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Neuromorphic CMOS imager for sparse vision data acquisition

Dissertation presented by
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ABSTRACT

The recent interest in modelling the human retina opens the doors to neuromorphic imagers. Neuromorphic engineering succeeds in achieving a biomimetic retina by providing an electrical model as close as possible to neuron architectures involved in the vision process: the event-based dynamic vision sensor (DVS) is designed for low-data and low-power image sensing acquisition. Its particularity resides in asynchronous pixels responding only to relative changes in light intensity. These sensors show a wide dynamic range, low power consumption and good time resolution. The visual neuromorphic field is thus not only promising for robotics, but also for real-time tracking.

Dynamic vision sensors seem suitable for detecting sparse data acquisition but raise one question: how to efficiently decrease the power consumption of an asynchronous pixel responding only to relative changes in light intensity? Inspired from a state-of-the-art image sensor, this study proposes a new DVS design in a mature 0.18 µm CMOS technology to tackle this challenge. Three different figures of merit are targeted: the dynamic range (to be maximized), the pixel area (to be minimized) and the power consumption (to be minimized). Moreover, compared to the state-of-the-art DVS working at 1.8 V or above, the main constraint added to this study is a supply voltage of 0.75 V to be compatible with the CAMEL image sensor from UCL. Pixel simulations show a detection in light changes of 10% with 3% of contrast matching. Moreover, the reported dynamic range is 140 dB. Finally, this new design provides a decrease of static power consumption from more than one order of magnitude (from 690 nW to 20.54 nW), at the expense of an increase in pixel latency of 42 µs.

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LIST OF ACRONYMS

AER	Address-Event Representation
APS	Active Pixel Sensor
ATIS	Asynchronous Time-based Image Sensor
BSI	Backside illumination
CIS	CMOS Image Sensor
CCD	Charge-Coupled Device
CMOS	Complementary Metal Oxide Semiconductor
DAVIS	Dynamic and Active pixel Vision Sensor
DPS	Dynamic Pixel Sensor
DR	Dynamic Range
DVS	Dynamic Vision Sensor
EHP	Electron-Hole Pair
FPN	Fixed-Pattern-Noise
MC	Monte-Carlo
MIMCAP	Metal-Insulator-Metal Capacitor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	n-channel MOSFET
OTA	Operational Transconductance Amplifier
PMOS	p-channel MOSFET
PWM	Pulse-Width-Modulation
SCA	Switched Capacitors Amplifier
SR	Slew rate
VGA	Video Graphics Array

Introduction

Since the early stages of evolution, we use our eyes to see our environment. They are even more important to prevent us from danger. For example, when a ball is thrown in our face, the brain can manage to avoid the collision thanks to the information received from our eyes. The visual system is therefore fundamental for survival.

Many researches have already investigated a way to model the human retina. Indeed, frame-based image sensors, that capture static light intensity, are widely deployed [1, 2]. However, they suffer from a high power consumption due to continuous data acquisition. Thus, a new sensor type has emerged: the neuromorphic image retina. It aims to give an electrical model as close as possible to neuron architectures involved in the biological vision process.

The first bio-inspired image sensor was designed in 1993 by M. Mahowald [3]. Even though its study was not adapted for any real task, it was an inspiration for many future neuromorphic works [4, 5, 6]. Hence, the event-driven dynamic vision sensor (DVS) was proposed [7]. The idea behind this new kind of sensor is to reduce redundant data by creating asynchronous pixels responding only to relative changes in light intensity. In this way, when a sparse data acquisition is detected, only the relevant data is processed. Keeping our example of the ball thrown in our face, this means that we only care now about the ball itself and not about the surrounding static environment. Works on DVS have already reported a wide dynamic range (120 dB), low power consumption (0.12 µW/pixel at low activity), low latency (only 3 µs) and a good temporal precision [5, 6]. The DVS features then get closer to the ones of human eyes. An event-driven dynamic vision sensor has already been implemented in a robot playing ping-pong [8] as well as in a pencil balancing robot [9]. The visual neuromorphic field is thus not only promising for robotics, but also for real-time tracking [10].

Therefore, this work aims to answer the following questions.

- How can the human eye be electrically emulated for event-driven sparse data acquisition?
- How to efficiently decrease the power consumption of an asynchronous pixel responding only to relative changes in light intensity?

Targets, contributions and outline

The purpose of this study is to understand the different DVS architectures proposed in the literature and to identify their strengths and weaknesses. Based on this, an asynchronous pixel architecture that responds only to relative changes in light intensity is proposed and implemented in a 0.18 µm CMOS technology, targeting the following three figures of merit:

- dynamic range (to be maximized),
- pixel area (to be minimized),
- power consumption (to be minimized).

Moreover, compared to state-of-the-art DVS architectures working at 1.8 V or above, the main constraint added to this study is a supply voltage of 0.75 V to be compatible with the CAMEL image sensor from UCL [1]. The main contributions from this work are:

- a complete state of the art of the different DVS architectures,
- a methodology providing guidelines to follow during the design of an asynchronous pixel for sparse vision data acquisition,
- a neuromorphic pixel designed in a 0.18 µm CMOS technology under 0.75 V supply voltage and its comparison with the literature that reveals a wider dynamic range and a lower power consumption.

These contributions are organized into five chapters:

- **Chapter 1:** The fundamentals as well as the state of the art are presented. The different concepts used during this Master Thesis are briefly reviewed. Then, contributions from prior researches are introduced and their main advantages and drawbacks are highlighted.
- **Chapter 2:** A neuromorphic pixel architecture is studied and essential guidelines to follow for its design are provided. Moreover, the equations behind its different circuit blocks are established.
- **Chapter 3:** The pixel is designed in a mature 0.18 µm CMOS technology with a supply voltage of 0.75 V. Simulations of each circuit block are given.
- **Chapter 4:** The pixel designed in Chapter 3 is fully validated and characterized in order to compare its performances with the state-of-the-art architectures.
- **Chapter 5:** Different trade-offs are discussed before giving some perspectives for future works.

Chapter 1

Fundamentals and state of the art

Contents

This first chapter aims to recall/explain some essential concepts required for a better understanding of this Master Thesis. Moreover, it gives an overview of the different architectures implementing a neuromorphic CMOS imager for sparse vision data acquisition. Firstly, the human retina architecture is presented in order to understand the challenges of a neuromorphic image sensor. Then, the photodiode principles of operation are analyzed and its important features are listed. Afterwards, the address-event representation (AER) used as an asynchronous communication protocol between neuromorphic chips is described. Finally, different state-of-the-art pixel architectures implemented for sparse vision data acquisition are presented from the oldest to the most recent one.

1.1 Human Retina

To develop a neuromorphic vision sensor, it is first essential to review the architecture and characteristics of the human retina. In this way, the different challenges to overcome are pointed out.

1.1.1 Architecture

The human retina is a thin sheet of neural tissue which recovers the orb of the eye. It is responsible for collecting the visual information and to send it to the brain in the form of spikes. A schema of the retina is presented in FIGURE 1.1.

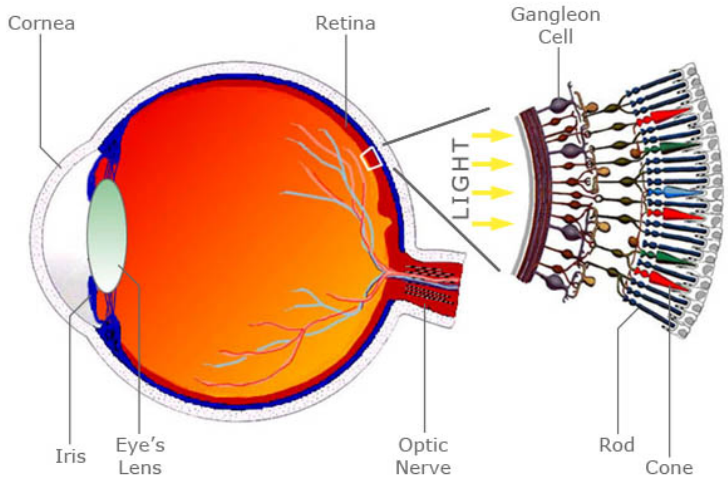


FIGURE 1.1 – Simplified schema of the human retina (from [11]).

In FIGURE 1.1, light comes from the left and goes to the back of the eye. It is sensed and transduced into an electrical signal by the photoreceptor cells (the cones for day vision and the rods for night vision) while the horizontal cells capture the background illuminance. Afterwards, the bipolar cells amplify the difference between the photoreceptor and the horizontal cells outputs. The signal is finally transferred to the ganglion cells that transform the electrical signal into an action potential before to send it to the brain [3].

1.1.2 Characteristics

As human eyes can be exposed to different illumination levels, the retina must send reliable information over a wide range of light intensities. Experiments on mudpuppy retinae confirmed this wide input range property of photoreceptors cells [12]. Theses experiments have also discovered that the transduction from the sensed light into a voltage is performed by a logarithmic relationship. Finally, according to a video realized by S. Liu, the human eye is composed of 10^8 photoreceptors and 10^6 ganglion cells spiking outputs. Moreover, it has a dynamic range of 180 dB and consumes only 3 mW [13]. Hence, reaching these same performances is a huge challenge for an artificial retina.

1.2 Photodiode

The creation of an artificial retina required a photodetector element to sense the surrounding light intensity. The principles of operation of this element as well as some of its figures of merit are presented in this division.

1.2.1 Principles of operation

An artificial retina is an image sensor composed of a two-dimensional array of pixels. Each of the pixel converts the incident light at its surface to an electrical signal thanks to a photodetector element. The photodetector is then a semiconductor that captures light particles (photons). The main principle of this element rests on the photoelectric effect. When the photodetector is lighted, the photons are either reflected or absorbed by the semiconductors. The absorbed light particles excite the electrons and if the energy is higher than the energy gap E_g, the electrons move from the valence band E_v into the conduction band E_c creating an electron-hole pairs (EHP) [14]. This phenomenon is represented in FIGURE 1.2.

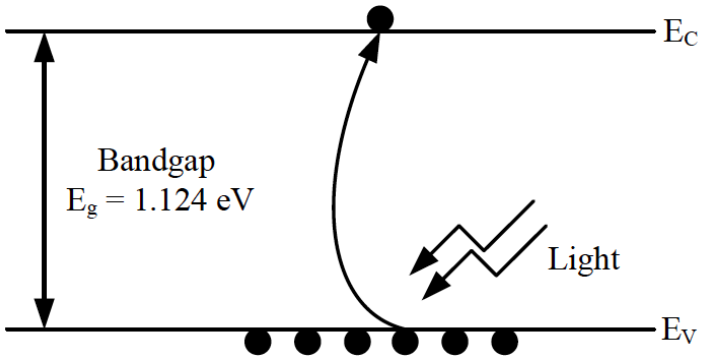
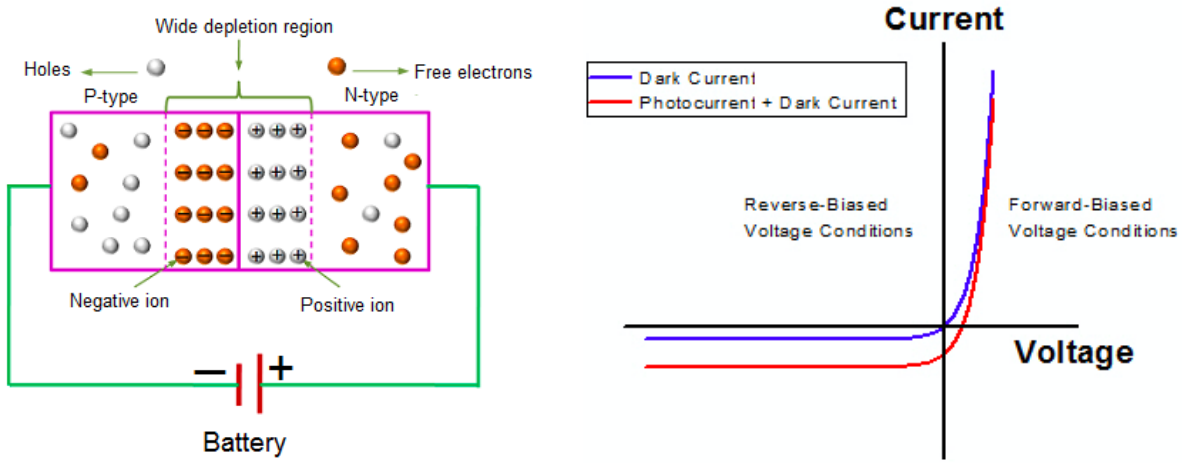


FIGURE 1.2 – Silicon energy bandgap (from [14]).

A well-known photodetector, that is used in this study to capture light information, is the photodiode. A photodiode is composed of a reverse biased p-n junction that generates a photocurrent. The p-n junction is obtained when a n-type semiconductor (characterized by an excess of electrons) and a p-type semiconductor (characterized by an excess of holes) are placed in contact. The electrons/holes diffuse from the n-type/p-type semiconductor to the p-type/n-type semiconductor due to the concentration gradient. The diffusion stops when the electric field of the carriers is equal to the concentration gradient, which is called the equilibrium. When this equilibrium is reached, the junction is formed. If the junction is reverse biased, this creates a depletion region between p-type region and n-type region [14, 15, 16]. A schema of the reverse biased pn-junction and its current-voltage characteristic curve are given respectively in FIGURE 1.3a and 1.3b.



(a) P-N junction in reverse biased (from [17]). (b) I-V characteristic of a p-n junction (from [18]).

FIGURE 1.3 – P-N junction.

Due to the electric field existing across the depletion region, when the photodiode is lighted, the photons absorbed in the depletion region create electron-hole pairs (EHP) that generate the photocurrent. Before giving the equation of the photocurrent, some parameters are defined [14, 15, 16, 19]:

- q is the electric charge ($q \simeq 1.6 \times 10^{-19} C$),
- k is the Boltzmann constant ($k \simeq 1.38 \times 10^{-23} JK^{-1}$),
- T is the absolute temperature,
- A is the total junction area,
- ϵ_s is the silicon permitivitty ($\epsilon_s = 11.9$),
- $N_{A,D}$ is the doping concentration of p-type and n-type semiconductors respectively,
- g_{op} is the light induced rate of EHP generation,
- n_i is the intrinsic carrier concentration of silicon ($n_i = 1.38 \times 10^{1}0 cm^{-3}$ at 300K),
- $m_{n,p}*$ is the effective mass of the electron and hole respectively,
- $\tau_{n,p}$ represents the recombination lifetime for electrons and holes respectively,
- $\mu_{n,p}$ is the electron mobility in the conduction band and hole mobility in the valence band respectively. It can be expressed by EQUATION 1.1,

$$\mu_{n,p} = \frac{q\tau_{n,p}}{m_{n,p}*} \tag{1.1}$$

- $D_{n,p}$, expressed by EQUATION 1.2, is the diffusion coefficient of electrons and holes respectively,

$$D_{n,p} = \mu_{n,p}\frac{kT}{q} \tag{1.2}$$

- $L_{n,p}$ is the electron and hole diffusion length respectively. It can be expressed by theEQUATION 1.3,

$$L_{n,p} = \sqrt{2D_{n,p}\tau_{n,p}} \tag{1.3}$$

- ϕ_0 is the internal potential expressed by EQUATION 1.4,

$$\phi_0 = \frac{kT}{q} ln(\frac{N_A N_D}{n_i^2}) \tag{1.4}$$

- W is the depletion region width. It depends on the doping concentration of p-type (N_A) and n-type (N_D) semiconductors used to create the p-n junction and on the voltage V applied across it. Its equation is given in EQUATION 1.5.

$$W = \sqrt{\frac{2\epsilon_s}{q}(\phi_0 - V)\frac{N_A + N_D}{N_A N_D}} \tag{1.5}$$

Hence, the current due to optically generated carriers I_{op} can be written as EQUATION 1.6.

$$I_{op} = q\ g_{op}\ A\ (W + L_n + L_p) \tag{1.6}$$

The generation of EHP depends on the light wavelength and on the penetration depth of the light particle into the material. The light intensity of a photon at depth x can be expressed as EQUATION 1.7.

$$I(x) = I_0\ exp(\alpha x) \tag{1.7}$$

with I_0 the light intensity at the surface of the semiconductor and α the coefficient of absorption.

1.2.2 Figures of merit

During this study, different figures of merit related to photodiodes are used to characterize neuromorphic pixels. The definition of each of them is reminded hereunder [19, 20].

Fill Factor The fill factor is the percentage of the area occupied by the photodiode in the pixel.

Responsivity In this study, the responsivity expressed the ratio of the photocurrent to the optical input power $[A/Wcm^{-2}]$.

Dark current The dark current is the current generated under dark conditions. It can also be defined as the leakage current of the photodiode and connected devices. The dark current is due to several sources as thermal generation in the depletion region, thermal generation due to defects on the surface of the diode, etc. If g_{th} is the thermal rate of EHP generation, photodiode leakage current can be expressed as EQUATION 1.8:

$$I_{dark} = q\ g_{th}\ A\ (W + L_n + L_p) \tag{1.8}$$

Dynamic range The dynamic range (DR) is defined as the ratio between the largest and lowest photocurrent detectable by the sensor.

Efficiency The external quantum efficiency defines the conversion from incident photons to electrons. It can be expressed as the product of optical efficiency and internal quantum efficiency. The first one represents the portion of absorbed photons in the semiconductor from the number of incident photons. The second one is the ratio between the number of induced charges and the number of incident photons. The photodiode efficiency depends also on the junction depth in the semiconductor. Actually, the EHP generated above the junction are much more likely to get collected that the ones generated under it as they start to spread deeper into the material, away from the junction. Hence, only a depth junction can generate EHP for long wavelength photons that penetrate deeper into the material. On the contrary, a junction relatively close to the surface captures only small wavelength photons. Finally, the collection efficiency depends also of the depletion region width as a wider one is more favorable to EHP generation.

Junction capacitance The junction capacitance C_j, that determines charge-to-voltage conversion, is defined by EQUATION 1.9.

$$C_j = \epsilon_s A/W \tag{1.9}$$

Hence, if the junction capacitance increases, the charge-to-voltage conversion decreases and inversely.

1.3 Address-Event Representation

The Address-Event Representation (AER) is an asynchronous chip-to-chip and/or intra-chip communication protocol that proposes a way to transmit spikes based signals between neuromorphic systems. Although the AER communication protocol is not developed in this Master Thesis, it is interesting to understand its principles of operation. Actually, in a future work, it could be implemented to this study. Hence, motivations to use such a protocol are pointed out in this section. Moreover, a brief explanation of its control sequences is given.

The AER protocol was first proposed in 1991 in a Ph.D Thesis of California Institute of Technology [21]. Since then it was used in many neuromorphic chips [5, 6]. This chip-to-chip communication protocol is inspired by biology. More specifically, it is inspired from neural networks in human brain where axons are replaced by digital circuits. The AER model for a unidirectional communication is schematized in FIGURE 1.4. Each neuron is represented by a unique binary address. Whenever a neuron of the transmitter chip spikes, the digital bus transmits its address to the receiver chip. Multiple neurons share then the same high-speed bus. When the receiver receives an address, it interprets it as an action potential that occurs on the corresponding neuron. Image sensors using the AER generate then an output in the form of address-events [3, 22].

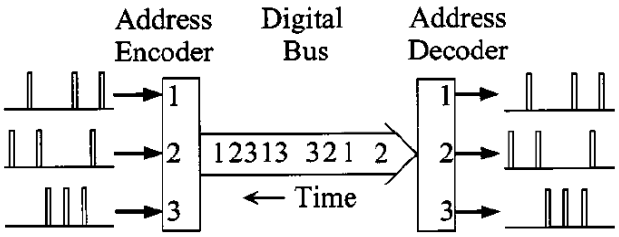


FIGURE 1.4 – General-purpose AER protocol for the transmission of data from an array of senders to an array of receivers (from [22]).

The control sequence of the data communication from a sender to a receiver is shown in FIGURE 1.5 and described hereunder. The request binary signal can only be driven by the sender and is exclusively sensed by the receiver and inversely for the acknowledge binary signal. The number of wires as well as the number of states of each wire are application dependent [23].

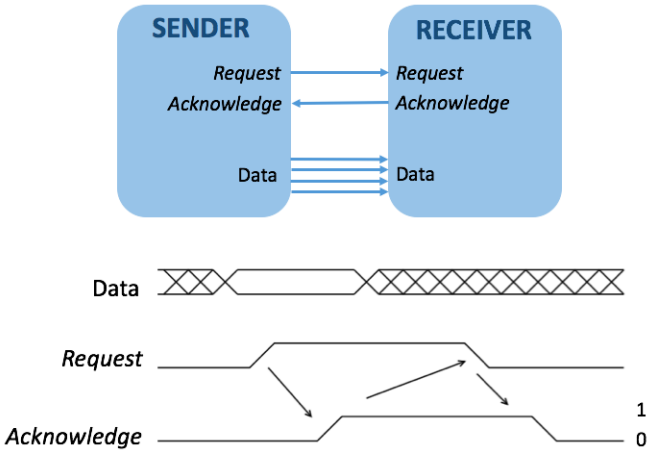


FIGURE 1.5 – Control sequence of the AER data communication (from [23]).

- In the inactive state, the sender drives the request signal to logic 0, the receiver drives the acknowledge signal to logic 0 and the data wires indicate data invalidity.
- When the sender wants to send a data to the receiver, it first drives a valid data on the data wires and then rises the request logic signal to 1. The receiver responds by sensing the valid data, which can take a relatively long time, and then rises the acknowledge logic signal to 1. This removes the requirement of the sender to put a valid data on the data wires.
- When the sender sensed an acknowledge signal to 1, it drives the request signal to logic 0 in a certain amount of time.
- When the receiver sensed that the request signal is at logic 0, it drives the acknowledge signal to logic 0 in a certain amount of time.
- Once the sender sensed that the acknowledge signal is at logic 0, it is free to start a new data communication.

1.4 Previous neuromorphic CMOS image sensors

The story begins in 1993 when M. Mahowald, during its doctoral dissertation and under the guidance of C. Mead, constructed an analog system of the biological structures involved in vision. In 1994, he built the first AER vision sensor in a modified version of its Ph. D., spending from neurons to microcircuits [3]. Actually, during its researches, he had discovered that neural circuit can be better modeled by electronic circuits in CMOS technology than by conventional sequential computer languages. Thanks to the similarities between the biological system and Mahowald's analog system, comparisons between them become feasible. The analog circuit he proposed is composed of a phototransducting element, a resistive system and a differential amplifier. The function of these three elements is summarized hereunder.

- The phototransducting element generates a logarithmic relation between the sensed light intensity and the output current.
- The resistive system models the retina horizontal cells by spatially and temporally averaging the output of the phototransducting element.
- The differential amplifier models the retina bipolar cells outputs by making the difference between the phototransductor outputs and the horizontal cells signals.

Unfortunately, the system realized by M. Mahowald was not adapted for any real task as the CMOS technology was not mature enough to reach the quality of charge-coupled device (CCD) imagers. Moreover, its pixel area was too large to provide high-resolution while meeting a reasonable cost. However, it was the first multichip analog neuromorphic system that interacts directly with the environment. Hence, it had opened the door to the neuromorphic CMOS imager field.

In 2004, Zaghoul and Boahen proposed a pixel design which captures the key features of biological retinas [4, 24]. They have drawn inspiration from neural circuits to build their model, especially from the four main ganglion cell types found in the retina. Their chip realizes luminance adaptation, bandpass spatio-temporal filtering, temporal adaptation and contrast gain control. Moreover, as their goals were more to provide a model and a design based on the retina key features than create a practical device, the performances as energy efficiency and deviation from pixel-to-pixel were not optimized.

Two more practical vision sensor architectures came out in 2002 and 2005: the asynchronous architecture developed by Kramer [25] and the synchronous architecture proposed by Mallik *et al.* [26] respectively. Since the Krame's work has been modified by different studies to reach better performances [5, 6, 27]. The two kinds of architectures are described in more details hereunder, starting with the Mallik *et al.* synchronous architecture.

1.4.1 Synchronous architectures

Mallik *et al.* developed a synchronous temporal change threshold detection imager in 2005 [26]. To achieve this purpose, they modified the traditional CMOS active pixel sensor (APS) to detect a change in illumination. The pixel architecture is represented in FIGURE 1.6.

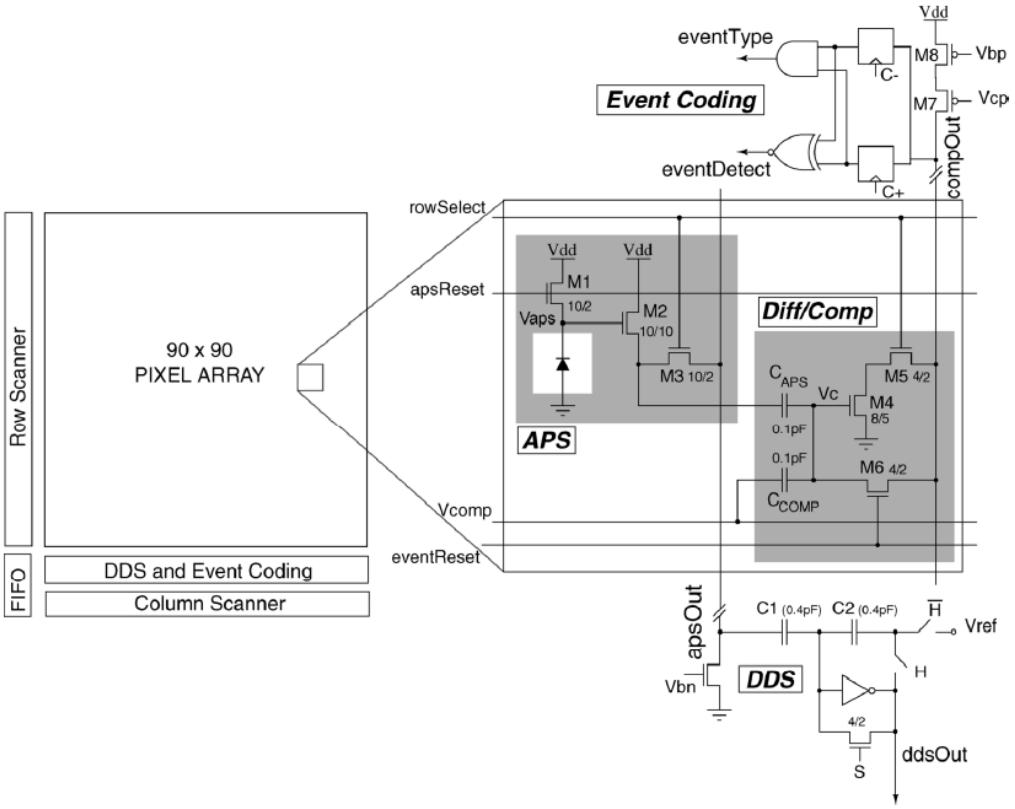
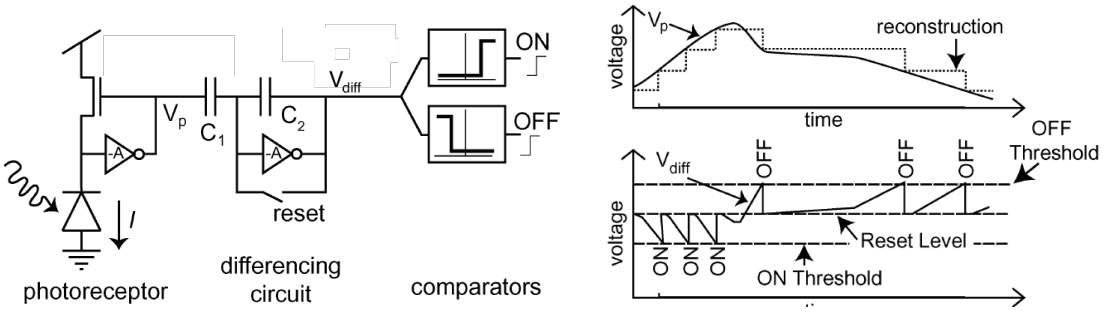


FIGURE 1.6 – The Mallik's pixel architecture (from [28]).

Hence, the pixel developed, and modified in 2007 [28], integrates a three-transistors APS with a two-capacitors and three-transistors comparator in a mature 0.5 µm CMOS technology. The comparator can be use either to detect scene changes or to perform, without any modifications, a pixel level analog-to-digital conversion. When using as a scene change detector, the comparator raises a digital flag each time the change between two frames of the analog APS output voltage reaches a variable threshold. As intensity change is detected by comparison of the current frame against the previous one, the event generation with this kind of architecture is synchronous. Moreover, although it uses a basic APS, the resulting dynamic range is poor and it results in absolute, rather than relative, illumination-change threshold. This architecture is therefore not really adapted for this Master Thesis as the asynchronous retina behavior is not emulated by the ATIS.

1.4.2 Asynchronous architectures

In 2002, Kramer developed a vision sensor in a 0.35 µm CMOS technology [25]. This sensor adapts itself to background illuminance and responds to local positive (ON) and negative (OFF) contrast changes. Two years later, P. Lichtsteiner *et al.* proposed an improved version of this imager by using a brighter pixel circuit and layout principles [29]. This modified sensor shows a wider dynamic range and responds much more symmetrical to ON and OFF events. However, the device presents a mismatch in transistors making it difficult to use at low contrast threshold. In 2008, a 120 dB and 15 µs latency asynchronous temporal contrast vision sensor was introduced by the same research group to overcome the previous issues [7]. The pixel is designed to achieve low mismatch, wide dynamic range, and low latency in a reasonable pixel area. The abstracted pixel and its principles of operation are illustrated in FIGURE 1.7a and FIGURE 1.7b respectively.



(a) Abstracted pixel schematic.

(b) Principle of operation.

FIGURE 1.7 – Pixel schematic and principles of operation of a 120 dB and 15 µs latency asynchronous temporal contrast vision sensor [7].

To preserve the three key properties of biological vision, this architecture combines a photoreceptor with a differential circuit and two comparators. The logarithmic photoreceptor circuit modeled the retina rods and cones by producing an electric signal V_p from the sensed light. The bipolar cells are replaced with a differential circuit amplifying V_p change between two reset signals, with the amplification gain determined by the capacitor ratio C_1/C_2. Finally, the ganglion cells are modeled with two comparators. Each time the output voltage of the differential circuit (V_{diff}) reaches one of the two comparators thresholds, the pixel creates an event leading to a reset of the differential circuit. Each pixel, independently from each other, produces therefore local sparse events in a continuous time. To be compatible with the AER protocol, these events appear at the pixel output as asynchronous digital addresses.

From this work, the dynamic vision sensor (DVS) is born. Since different vision sensors have been developed. In 2011, C. Posh *et al.* proposed an asynchronous time-based image sensor (ATIS) [6]. Barranco *et al.* came out with two asynchronous frame-free dynamic vision sensors in 2011 [30] and 2013 [27]. A dynamic and active pixel vision sensor (DAVIS) [5] and its color version (cDAVIS) [31] were introduced respectively in 2014 and 2016 by the Institute of Neuroinformatics at the University of Zurich and ETH Zurich. Finally, the Samsung group has recently proposed a VGA dynamic vision sensor. The different architectures are presented hereunder in chronological order.

The asynchronous time-based image sensor

The asynchronous time-based image sensor (ATIS) schematized in FIGURE 1.8 is the first visual sensor to combine the "where" and "what" systems [6]. The imager integrates an array of pixels, each of them containing an event-based change detector and a pulse-width-modulation (PWM) exposure measurement circuit. The event-based change detection system is based on the dynamic vision sensor developed previously and allows to model the biological "where" system when an object motion is detected. The PWM exposure measurement system is used to provide details of visual information, modeling then the "what" system.

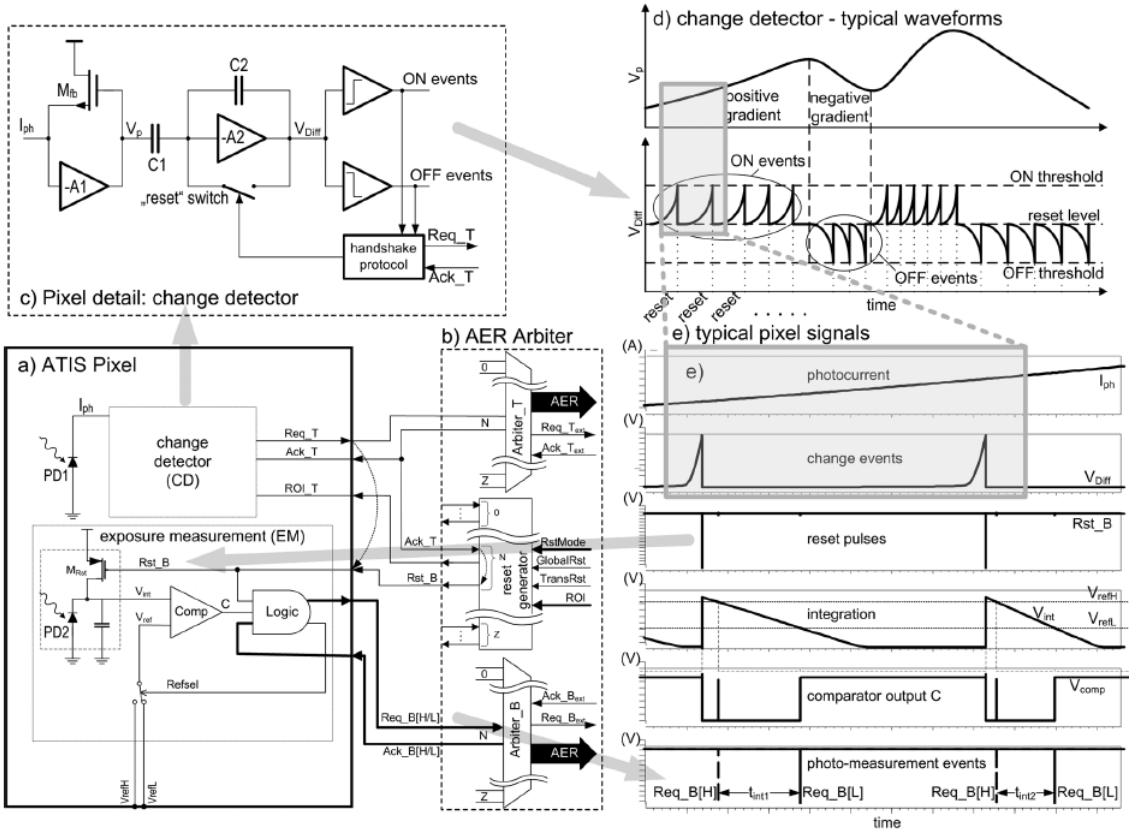


FIGURE 1.8 – Schematic view of the ATIS architecture (from [6]).

The exposure measurement system of the ATIS pixel is initialized only when the change detector of the same pixel detects a change in light intensity and produces the corresponding event. Therefore, the sensor does not generate redundant data when no events are detected. The visual information (temporal contrast and grayscale data encoded in inter-event intervals) is communicated to the output channel in the form of an asynchronous AER protocol.

Benefits from this kind of architecture is a reduction in bandwidth, memory and power requirements for data transmission. However, its drawback is that each pixel used two photodiodes, one in the change exposure measurement system and one in the change detector.

A 3.6 ms latency asynchronous frame-free event-driven DVS

In 2011, Barranco *et al.* proposed a modified version of the dynamic vision sensor by adding a compact preamplification stage allowing to improve the minimum detectable contrast over previous design [30]. Each pixel still detects temporal contrast but a minimum change in light intensity of 10% can now be detected while at the same time reducing the pixel area by 1/3. Moreover, by using an alternative photo-sensing stage, the sensor latency is reduced to 3.6 µs. However, the price to pay for these improvements is a significant increase in the power consumption and a slight increase in the fixed pattern noise (FPN). In 2013, they succeed in improving the contrast sensitivity down to 1.5% with a power consumption of 4 mW [27]. Moreover, the FPN is reduced to 0.9% and the overall area is further decreased while maintaining a good dynamic range (DR) and a latency of 3 µs. Decreasing the contrast sensitivity improves the quality of the sensed scene as the sensor captures finer details as contours and textures. Although the price to pay for this improvement is the increase of the output events, it opens the doors to new applications such as high speed texture based recognition.

The dynamic and active pixel vision sensor

The asynchronous time-based image sensor (ATIS) contains motion artifacts at high-speed due to the use of its two photodiodes. To overcome this issue, a dynamic and active pixel vision sensor (DAVIS) was proposed by Brandli *et al.* in 2014 [5]. The pixel architecture developed in the DAVIS is represented in Figure 1.9. It integrates both a basic active pixel sensor (APS) and a modified version of the DVS developed by Lichtsteiner [7]. More interesting, the APS and the DVS share the same photodiode. Therefore, the DAVIS can produce concurrently asynchronous events (with the DVS part of the pixel) and synchronous absolute light information (with the APS part of the pixel).

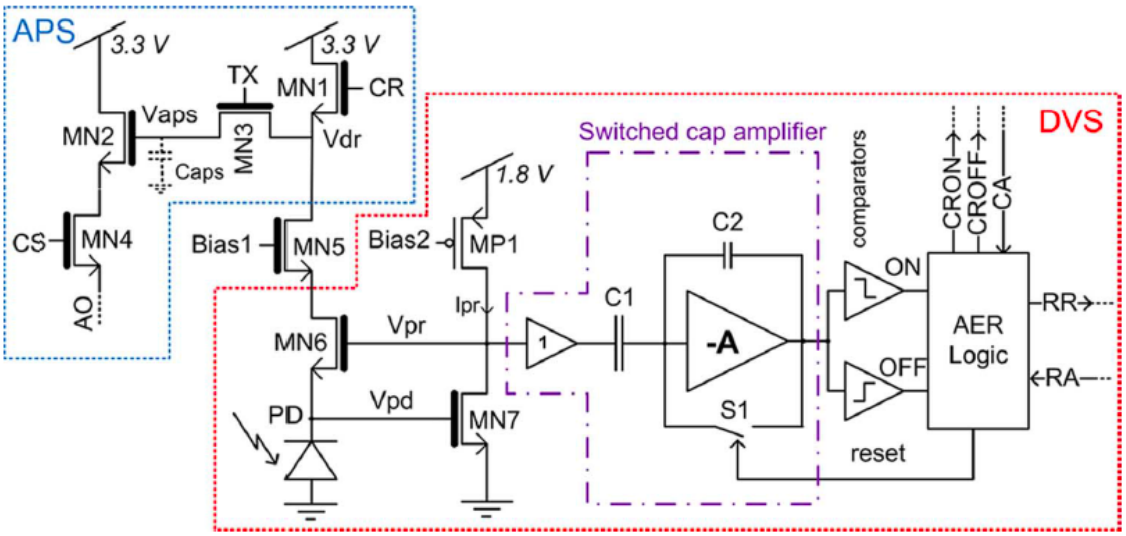


Figure 1.9 – DAVIS pixel schematic (from [5]).

The DVS part of the pixel is composed of, from left to right, a photoreceptor circuit, a buffer, a switched capacitor amplifier circuit, two comparators and an AER logic. The different elements are explained hereunder.

- The photoreceptor circuit performs the logarithmic conversion between the photocurrent and its output voltage V_{pr}.
- The buffer allows to isolate the photoreceptor circuit from the reset of the switched capacitor amplifier.
- The switched capacitor amplifier (SCA) circuit amplifies the change in V_{pr} between two reset signals.
- The two comparators compare the amplified change in V_{pr} with an upper and a lower threshold. If the change reaches one of the two thresholds, an OFF or ON event is respectively produced.
- The AER logic resets the pixel when an event is produced and ask the access to the bus to send it to the rest of the chip.

This vision sensor is developed in a 0.18 µm CMOS technology and reaches a contrast sensitivity of 11%, a dynamic range of 130 dB and a minimum pixel latency of 3 µs.

The colored dynamic and active pixel vision sensor

In 2016, a colored version of the DAVIS (cDAVIS) was proposed [31]. Each pixel of the cDAVIS combines monochrome event-generating DVS pixels and 3 APS pixels patterned with an RGBW color filter array. Therefore, the colored vision sensor is able to concurrently produce synchronous VGA resolution RGBW-coded frames and asynchronous monochrome QVA resolution temporal contrast events. Hence, with a slightly modified DAVIS pixel, the cDAVIS is able to capture the detail color while still tracking movements.

The Samsung's pixel

Recently, Samsung developed a VGA dynamic vision sensor [32]. The Samsung's pixel tries to reach thinner pixels as the DAVIS pixel size of 18.5 µm x 18.5 µm was too large for economical mass production. The Samsung's group succeeded in providing a 9 µm x 9 µm pixel by implementing the DVS in a backside illuminated (BSI) sensor. This kind of sensor increases the pixel responsivity thanks to its flip of the metal structure upside-down [33]. Therefore, the light particles are not anymore blocked by routing layers. With this new design, capacitors of the SCA circuit can overlap the photodiode improving therefore the pixel area. The Samsung's group also succeeded in reaching a data rate of 300 Meps (mega event per second) by grouping several neighboring pixels and dealt with them like a single one, with ON and OFF events of the same pixels group processed in parallel.

1.4.3 Summary

The features of the different neuromorphic architectures designed for sparse vision data acquisition are summarized in TABLE 1.1. After a discussion of some figures of merit, an image sensor is chosen to be the start point of this study.

Technology: Although charge-coupled devices (CCD) provide higher pixel sensitivity and lower noise images, all the state-of-the-art architectures were designed in CMOS technology in order to integrate analog and digital processing down to the pixel level. Moreover, as CCD required a special manufacturing process, they are more expensive than CMOS imagers [14, 20].

Fill Factor and DR: Recent studies as the DAVIS and the ATIS showed an increase of the fill factor and of the DR compared to their predecessors. The Samsung's pixel fill factor was not mentioned but is intended to be high as it uses a BSI photodiode.

Power consumption: The power consumption reached by the Barranco's work in 2011 is the higher one due to its preamplification stages. However, the definitions of a high and a low activity are not really standardized across the different studies. Barranco defined its low activity as moderate output event rates (below 1 Meps), the ATIS as no DVS activity, the DAVIS did not provide any scale and Samsung defined it as an output event rate of 100 Keps. A high activity was defined by Barranco as an output event rate above 1 Meps, by Samsung at 300 Meps and was not defined by the DAVIS and the ATIS. Older works did not give any of the two definitions. Hence, comparison in power consumption between the different sensors is not easy. A way to facilitate this comparison would be to have the DC power of each architecture as well as its required energy to produce an event.

Contrast sensitivity: Minimum contrast sensitivity is application dependent. Actually, a low contrast sensitivity sensor as the Barranco's imager in 2013 provides a more detailed information but at the price of a higher event rate. Hence, there is no good or poor contrast sensitivity.

FPN: The fixed pattern noise (FPN) represents the pixel to pixel variation. It was defined by Lichsteiner in its first DVS. According to it, FPN is calculated as the standard deviation of measured contrast threshold expressed in [%] of illumination change. A fixed pattern noise of 2.1 % was reported in its paper. The most recent works kept its definition. The Barranco's imager in 2011 showed an increased of the FPN due to its minimum latency improvement. In 2013, the sensor reached a lower FPN while still decreasing the minimum latency. The ATIS's pixel succeeded to reach a FPN below 0.25% thanks to the implementation of a correlated double sampling method. Finally, compared to the ATIS, the DAVIS's pixel showed an increase of the FPN (3.5%).

Minimum latency: The minimum latency is determined by the time taking by the first event to occur when the pixel is excited with a step photocurrent change of 30% at 1 klx. Excepted for the ATIS, each time a new architecture is proposed, it presents a decrease of this feature.

As the Zaghloul's architecture aimed more to provide a pixel based on the retina key features than create a practical design, its poor dynamic range and high power consumption make it not suitable for this study. Then, as mentioned before, the Mallik *et al.* pixel is also not appropriate for this work as its synchronous pixel does not reflect the asynchronous principles of operation of the human retina. Concerning the asynchronous pixels constructed in a mature 0.18 µm or 0.35 µm CMOS technology, the DAVIS is the one reaching the larger dynamic range, the lower minimum latency and the smaller pixel area while consuming only 0.32 µW/pixel at high activity. Moreover, it uses only 1 photodiode making it more suitable for high-speed applications than the ATIS. The Samsung's dynamic vision sensor succeeded to further decreases the pixel area to 9x9 μm^2 with a BSI sensor designed in 90 nm CMOS technology. As a 0.18 µm CMOS technology is preferred to integrate our work to the DVS developed in UCL, this study starts from the DAVIS to develop its own pixel architecture. More precisely, it starts from the DVS part of the DAVIS as this work aims to provide only a pixel detecting changes in light intensity in order to decrease data-processing requirements. Asynchronous absolute light information could be detected in a future work by integrating our pixel to the DVS from UCL.

Table 1.1 – Summary of state-of-the-art architectures.

	Samsung [32]	DAVIS [5]	ATIS [6]	Barranco 2013 [27]	Barranco 2011 [30]	Lichsteiner [7]	Mallik [26]	Zaghloul [24]
Functionality	DVS	DVS + APS	DVS + Exposure measurements	DVS	DVS	Asynchronous temporal contrast	APS imager + temporal change detection	Asyn. spatial and temporal contrast
CMOS Technology	90 nm CIS 1P5M BSI	0.18 µm CIS 1P6M MIM	0.18 µm CIS 1P6M MIM	0.35 µm CIS 2P4M	0.35 µm CIS 2P4M	0.35 µm CIS 2P4M	0.5 µm CIS 2P3M	0.35 µm CIS 2P4M
Chip size mm^2	8 x 5.8	5 x 5	9.9 x 8.2	4.9 x 4.9	5.5 x 5.6	6 x 6.3	3 x 3	3.5 x 3.5
Array size	640 x 480	240 x 180	304 x 240	128 x 128	128 x 128	128 x 128	90 x 90	96 x 60
Pixel size um^2	9 x 9	18.5 x 18.5	30 x 30	30 x 31	35 x 35	40 x 40	25 x 25	34 x 40
Fill factor	N.A.	22%	30%	10.5%	8.7%	8.1%	17%	14%
Pixel complexity	N.A.	47 T. 1 photodiode	77 T. 2 photodiodes	N.A.	N.A.	26T.	6T.	38T.
Supply voltage	2.8V analog 1.2V digital	1.8V/3.3V	3.3V analog 1.8V digital	3.3V	3.3V	3.3V	5V	3.3V
Power high activity low activity	50 mW 27 mW	14 mW 5 mW	175 mW 50 mW	4 mW	231 mW 132 mW	24 mW	30 mW	62.5 mW
Power/pixel high activity low activity	0.16 μW 0.088 μW	0.32 μW 0.12 μW	2.4 μW 0.69 μW	0.24 μW	14.1 μW 8.06 μW	1.46 μW	3.7 μW	10.85 μW
DR	N.A.	130dB DVS 51dB APS	125dB	120dB	100dB	120 dB	51dB	50dB
Min. contrast sensitivity	9%	11%	30% @ 1klux	1.5%	10%	15%	2.1%	N.A.
FPN	N.A.	0.5% APS 3.5% DVS	<0.25% intensity	0.9% DVS	4%	2.1%	0.5%	N.A.
Min. latency	N.A.	3us @ 1klux	<4us @ 1klux	3.2us @ 2klux	3.6us @ 25klux	15us @ 1klux	N.A.	10Meps

Chapter 2

Pixel architecture and specifications

Contents

This second chapter aims to describe the pixel architecture chosen in this study to implement a neuromorphic CMOS imager. Firstly, the pixel architecture is presented and its similarities and differences with DAVIS pixel are highlighted. Then, the pixel principles of operation are explained. Finally, based on the pixel study, some pixel design guidelines are given. This chapter is intended to be independent of any technology as its main goal is to provide guidelines for the pixel design. Hence, exporting the pixel architecture in any technology is facilitated.

2.1 Pixel architecture

The pixel architecture studied in this Master Thesis is a modified version of the state-of-the-art architecture DAVIS. It is represented in FIGURE 2.1.

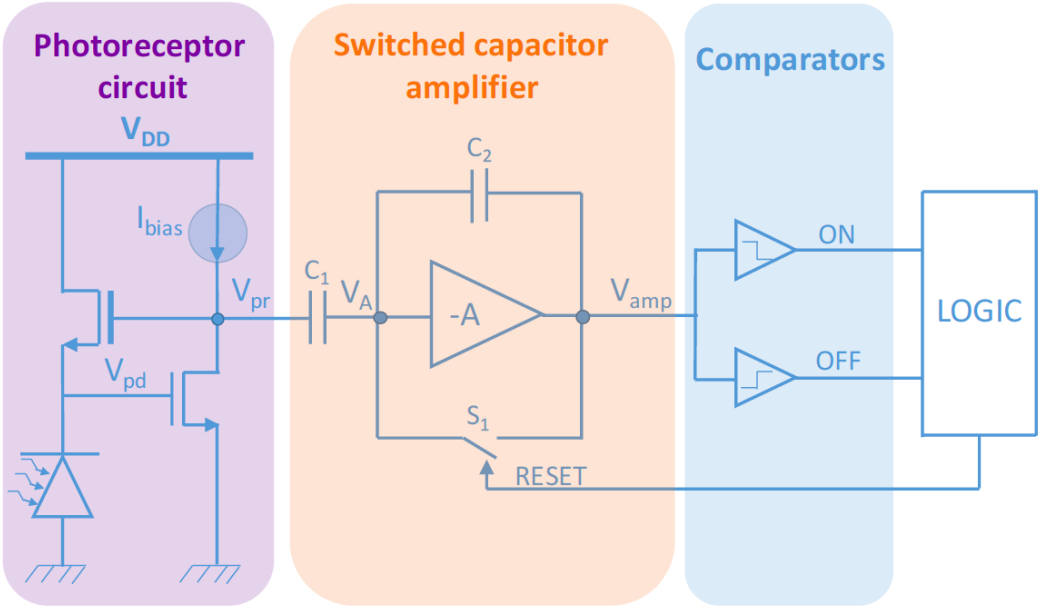


FIGURE 2.1 – Schema of the pixel architecture studied in this Master Thesis.

Therefore, the architecture is composed of four circuits:

- **Photoreceptor circuit:** it is responsible for the logarithmic transduction from the sensed light to its output voltage V_{pr}. The bias voltage V_{pd} allows to keep the photodiode at virtual ground.
- **Switched capacitor amplifier:** it amplifies the change in photocurrent intensity since the last reset. Its output is noted V_{amp}.
- **Comparators:** it compares the output of the switched capacitor amplifier with two thresholds. If the upper threshold is reached, the corresponding comparator produces an OFF event. On the other side, if the lower threshold is reached, the corresponding comparator produces an ON event.
- **Logic:** when an event is produced, the logic circuit provides the signal needed to reset the switched capacitor amplifier circuit.

Compared to the DAVIS pixel, this study does not contain any buffer circuit as it is not required by the architecture. The addition of a buffer increases indeed the pixel area and decrease its performances as it is discussed in SECTION 3.3. Then, as the subject of this study is focused on the neuromorphic pixel either than on the sensor itself, the AER logic is replaced with a simple logic providing the reset signal. The AER logic can still be easily added later with additional eleven transistors and one capacitor [7]. Another significant difference resides in the lack of an active pixel sensor part. Actually, this study is focused only on relative changes in light intensity. However, a possible solution to synchronously

produce absolute light information is to integrate the dynamic pixel sensor (DPS) from UCL (see ANNEXE A.1) to the DVS developed in this Master Thesis. Finally, each ideal bloc presented in the schematic view is realized apart from the ones used in the DAVIS, the purpose being to target three figures of merit: a low power consumption, a high dynamic range and a low pixel area. Hence, this work is only inspired by the schematic architecture of the DAVIS and not from its implementation.

To understand more deeply the pixel behavior, its principles of operation are analyzed in the next section. Afterwards, the four pixel circuits are studied and some of their specifications and architectural choices are introduced. These specifications are intended to be independent of any technology, the main purpose being to give some guidelines to respect during the pixel design. Obviously, the pixel area minimization by using as much as possible small transistor size is a guideline available for all circuit blocks.

2.2 Principles of operation

The ideal pixel behavior is represented in FIGURE 2.2. In the upper graph, the photoreceptor circuit output as well as the photodiode bias voltage are represented. Depending on the sensed light intensity, the voltage V_{pr} has a logarithmic variation. The bias voltage V_{pd} stays constant over time. In the lower graph, the output voltage of the switched amplifier capacitor circuit as well as the reset signal and the two levels of thresholds are drawn. When the voltage V_{pr} is rising, the output voltage V_{amp} decreases due to the negative gain of the switched capacitor amplifier. The SCA output voltage follows then the inverse variation of V_{pr}. When it reaches a threshold, the logic circuit performs a reset of V_{amp} to $V_{DD}/2$.

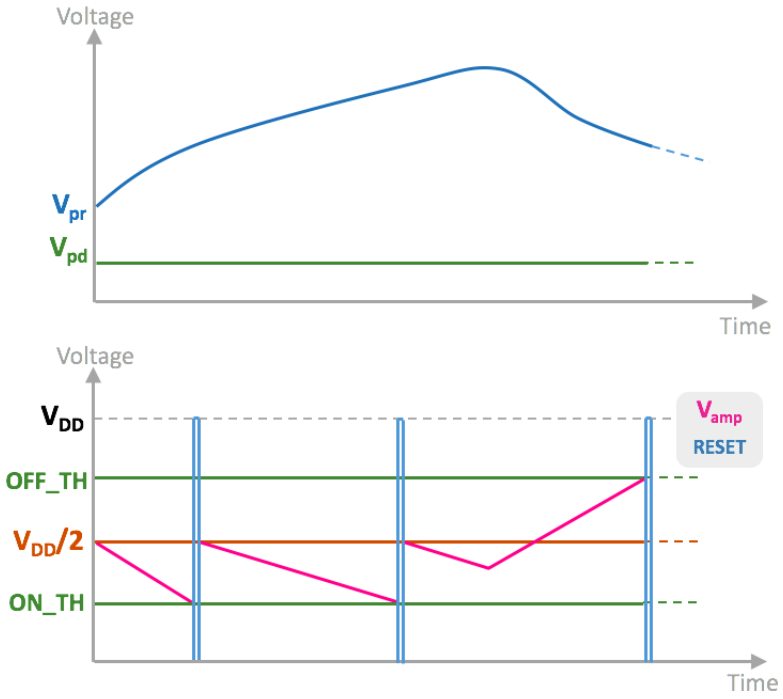


FIGURE 2.2 – Pixel principles of operation.

2.3 Photoreceptor circuit

The photoreceptor circuit, responsible for the transduction from the absorbed light to an electrical signal, is the first circuit block of the pixel. Firstly, the photoreceptor circuit is composed of a photodiode that sensed the photons and converts them to a photocurrent. The choice of this photodiode is important as it defines the pixel responsivity. Then, the transistor located above the photodiode performs the logarithmic conversion between the sensed light and its gate voltage V_{pr}. This transistor is called the *photoreceptor transistor* for the rest of this study. Finally, a bias source and its transistor (called the *bias transistor*) allow to keep the photodiode at a virtual ground. Guidelines to choose these different elements are given in the next sections, starting with the photodiode.

2.3.1 Photodiode

Performance parameters of a CMOS compatible photodiode vary according to the photodiode size, geometry and type. The three available CMOS compatible types of photodiode are the n^+/p-sub, the n-well/p-sub and the p^+/n-well/p-sub types. The cross section of each of them is represented in FIGURE 2.3.

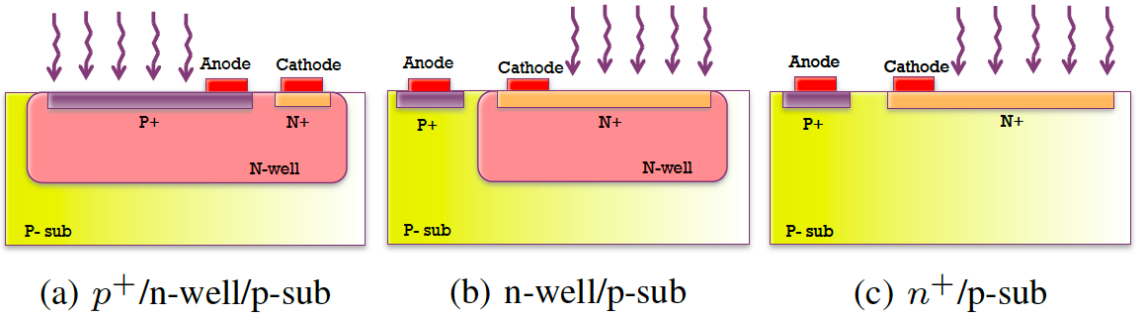


FIGURE 2.3 – Cross section of the photodiode types (from [34]).

The photodiode type choice is important as it determines different figures of merit of the pixel as its responsivity and its fill factor. In order to select the most adapted one, the three types are presented and compared hereunder. Moreover, their different figures of merit are discussed [19, 34].

The n^+/p-sub type photodiode: The n^+/p-sub type photodiode is composed of a highly doped n-region in a p-substrate. The n-region is created by ion implantation which leads to a junction relatively close to the surface of the semiconductor. Hence, according to SECTION 1.2.2, the collection efficiency is reduced. The photodiode also suffers from a narrow depletion region due to the high doping concentration of n^+. Consequently, the collection efficiency is further reduced and its junction capacitance is large. The responsivity of this photodiode type is then not sufficient for this study. Moreover, due to its large junction capacitance, the charge-to-voltage conversion is low.

The n-well/p-sub type photodiode: The n-well/p-sub type photodiode is composed of a highly doped n-region in a n-well. The low doping concentration of the n-well creates a p-n junction in the p-substrate. Due to this low doping concentration, the junction depletion is wider than the one achieved in the n^+/p-sub type photodiode. This should lead to a higher collection efficiency and a lower junction capacitance. The charge-to-voltage conversion is then improved. As the n-well is located deeper than the n^+ ion implementation, its corresponding junction is also localized deeper, increasing further the collection efficiency as the photodiode is more efficient at capturing long wavelength photons.

The p^+/n-well/p-sub type photodiode: The p^+/n-well/p-sub type photodiode is composed of a highly doped p-region and n-region in a n-well. According to the literature, this photodiode is the one reaching the highest collection efficiency for CMOS technologies 0.5 µm [19] and 0.18 µm [34]. Actually, the photodiode is composed of two junctions, the p^+ to n-well junction and the n-well to p-sub junction. Therefore, the resulting depletion region is higher than in the two other photodiode types, increasing then the collection efficiency. However, the two junction capacitances of the p^+/n-well/p-sub type photodiode are added together in parallel. The resulting junction capacitance is then higher, decreasing the charge-to-voltage conversion.

To detect changes in light intensity, the photoreceptor circuit needs the best collection efficiency as possible. Therefore, the p^+/n-well/p-sub type photodiode is a good candidate for this study. Moreover, as previously explained, this work should be compatible with the CAMEL sensor from UCL [1]. As this imager uses a p^+/n-well/p-sub type photodiode, the choice of this photodiode is further encouraged. The choice of photodiode size is application dependent. A larger photodiode diffusion area produces a larger photocurrent, enhancing the detection of low illuminances. However the price to pay is an increase of the pixel area.

Before giving guidelines about the design of the rest of the photoreceptor circuit, the dark current and the range of light intensity are discussed.

Dark current

The main source of dark current comes from the interface state at the surface of the n-well to p-sub junction. Actually, according to EQUATION 1.8, the dark current is proportional to the thermal rate of electron-hole pairs (EHP). This term is maximized when the number of electrons and holes are equal. Hence, the high free charge carrier concentration of the p^+ material decreases the thermal rate of the electron-hole pairs generation in the p^+ to n-well junction. Therefore, the low depletion region of the p^+ to n-well junction produces only few electron-hole pairs in dark conditions. For the n-well to p-sub junction, the depletion region is wider resulting to more EHP generations. Moreover, as this deeper junction collects all the electron-hole pairs generated above it, its dark current is further increased. However, compared to the n-well/p-sub type photodiode, the p^+ protective layer reduces the number of free interface states and leads to a reduction in the dark current [15, 19].

Range of light intensity

This section aims to fix a range of photocurrent that should be detected by the pixel. In FIGURE 2.4, the different scales related to light intensity are represented.

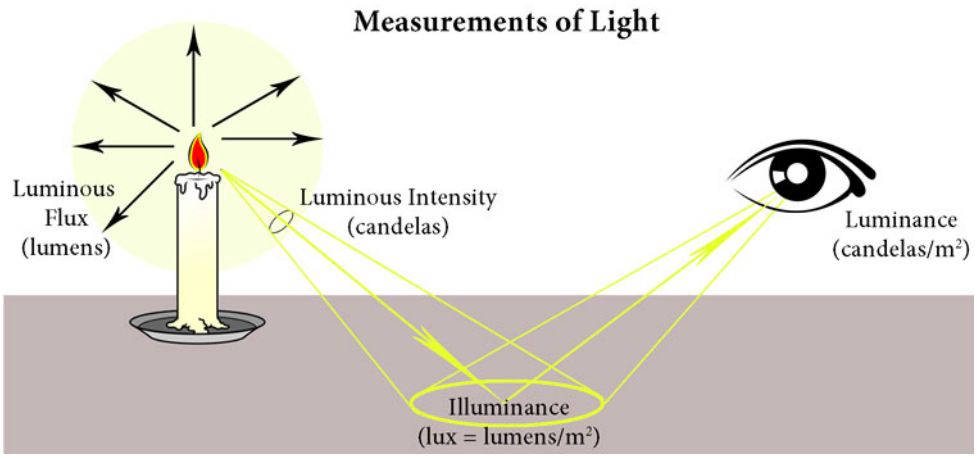


FIGURE 2.4 – Schema of the different light scales (from [35]).

These terms are defined in [35, 36, 37] and reported hereunder.

- The **luminous intensity** measures the amount of light produced by a source within a solid angle of one steradian (sr). Its unit of measurement is the candela (cd). One candela is defined as the luminous intensity of a point source emitting a monochromatic radiation of frequency 540 THz and with a radiant intensity in its radiating direction of $\frac{1}{683}$ watt per steradian: 1 cd $=$ $\frac{1}{683}$ W/sr
- The **luminous flux** measures the amount of light emitted in all directions. It represents then the total quantity of visible light emitted by a source. As it is a measurement of the light source, it is independent of the surface type. Its unit of measurement is the lumen (lm): 1 lm = 1 cd $\times$ 1 sr = 1 cdsr
- The **illuminance** is the total luminous flux incident on a surface per unit of area. Its unit of measurement is the lux: 1 lx = 1 lm/m^2 = $\frac{1}{683}$ W/m^2.
- The **luminous emittance** is the luminous flux per unit of area emitted from a surface.
- The **luminance** is the intensity of a light reflected from an object or a surface in a direction per unit of area. It is then the only scale sensed by the human eye. As represented in FIGURE 2.5, if the human eye looks at the surface S with an angle of view α, the apparent surface S_{app} is: $S_{app} = S \times sin(\alpha)$. Therefore, luminance does not depend from the viewing distance. Its unity of measurement is the candela per meter square (cd/m^2).

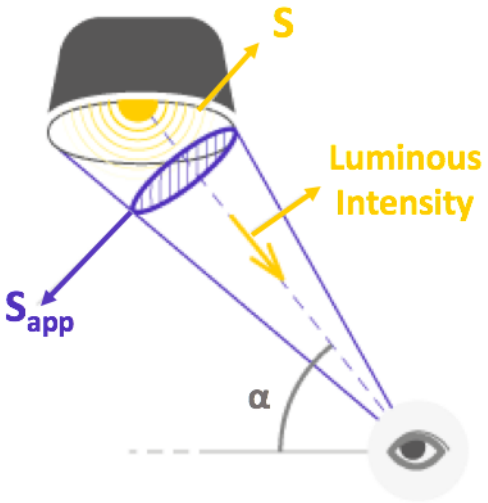


FIGURE 2.5 – Conversion from surface to apparent surface (adapted from [36]).

The illuminance and the luminous emittance can be related by EQUATION 2.1:

$$M_v = E_V R \tag{2.1}$$

with M_v the surface luminous emittance, E_v the received illuminance and R the surface reflectance. Moreover, the luminous emittance and the luminance can be converted by EQUATION 2.2 :

$$M_v = \int_{\Omega_\Sigma} L_v cos(\theta_\Sigma) d\Omega_\Sigma \tag{2.2}$$

with Ω_Σ the solid angle (sr) containing the specified direction, L_v the luminance and θ_Σ the angle between the normal to the surface and the specified direction [37].

As the luminance depends on the surface reflectance, the range of light intensities is given in terms of illuminance. Some standardized illuminance values as well as the minimum illuminance detected in the DAVIS are summarized in TABLE 2.1. The maximal illuminance is then fixed at $100,000$ lx, corresponding to full sunshine. To reach at least the same performances as the DAVIS, the minimum illuminance is fixed at 0.01 lx. When the photodiode responsivity and size are known, the luminous flux per unit of area can be easily expressed as photocurrent.

TABLE 2.1 – Norm of some illuminance intensities [38].

	Illuminance
In full sunshine	$100,000$ lx
In an office	500 lx
In an illuminated street	50 lx
The DAVIS minimum illuminance	0.01 lx

2.3.2 Photoreceptor transistor

The photoreceptor transistor achieves the conversion from photocurrent to its gate voltage. To sense low currents, the photoreceptor transistor should work in weak inversion. Therefore, the transduction from current to voltage can be modeled as in EQUATION 2.3 [39]:

$$\begin{aligned} I_D &= I_0 \frac{W}{L} exp(\frac{V_{pr} - nV_{pd}}{nU_T}) \\ \Leftrightarrow V_{pr} &= ln(\frac{I_D}{I_0}\frac{L}{W})nU_T + nV_{pd} \end{aligned} \tag{2.3}$$

with I_D the transistor drain current and I_0 the characteristic current representing the leakage current through the transistor. W and L are the photoreceptor transistor width and length respectively. The subthreshold slope factor n (around 1-1.5) represents the effect of the gate voltage on the drain current and $U_T = kT/q$ is the thermal voltage.

The transistor size should be chosen in order to maximize the pixel dynamic range. In the DAVIS, a dynamic range of 130 dB is reported, with a minimum illuminance of 0.01 lx [5]. To sense low light intensities, corresponding to a low drain current, the analysis of EQUATION 2.3 shows that a large and a low values of transistor length and width are respectively required. If the complete relationship between the sensed current and the gate voltage V_{pr} is considered, EQUATION 2.4 can be written [40]:

$$I_D = 2n\mu C_{ox}\frac{W}{L}U_T^2 e^{\frac{-V_{T0}}{nU_T}} e^{\frac{V_{pr}}{nU_T}} (e^{\frac{-V_{pd}}{U_T}} - e^{\frac{-V_{DD}}{U_T}}) \tag{2.4}$$

With C_{ox} the oxide gate capacitance, μ the mobility and V_{T0} the threshold voltage of the transistor. In this way, to decrease further the minimum sensed light, a transistor with a larger threshold voltage should be used.

2.3.3 Bias point

The last element composing the photoreceptor circuit is the bias transistor. It is used to keep the photodiode at the same bias point, noted V_{pr}. To hold the photoreceptor transistor in an active region, this bias voltage must be lower than the output voltage V_{pr}. A too large value of the bias voltage decreases then the pixel dynamic range as the V_{pr} minimum value is saturated by the bias voltage. However, a too low value of V_{pd} can generate issues, as zero bias voltage, during the Monte-Carlo simulation. A current mirror with a reference voltage, shared by all pixels in the array, is used to maintain it. In this way, the correct value of V_{pd} is insured in each Process-Temperature corners. Finally, the bias transistor size determines the bias current I_{bias}. This current has an effect on the transduction slew rate. The slew rate can be expressed as in EQUATION 2.5:

$$SR = I_{bias}/C_1 \tag{2.5}$$

with C_1 the first capacitor of the switched capacitor amplifier circuit. Therefore, to increase the slew rate, a low capacitance and a large current I_{bias} should be used. However, a too large value of I_{bias} increases also the pixel power consumption.

2.4 Switched capacitor amplifier

The switched capacitor amplifier (SCA) circuit is the second circuit block of the pixel. It takes as input the output voltage V_{pr} of the photoreceptor circuit and its output is noted V_{amp}. This circuit aims to amplify the changes in intensity between two reset signals. To achieve this goal, it is composed of two capacitors, one amplifier and one switch. As it is demonstrated hereunder, the amplify gain is determined by the ratio of the two capacitors C_1/C_2. When an event is produced, the switch allows to reset the switched capacitor amplifier circuit. The actual value of V_{pr} is then saved on the capacitance C_1 and the output V_{amp} is short-circuited with the negative input of the amplifier. A reset of V_{amp} at $V_{DD}/2$ is then realized each time an event is produced. The switched capacitor amplifier circuit is represented in FIGURE 2.6.

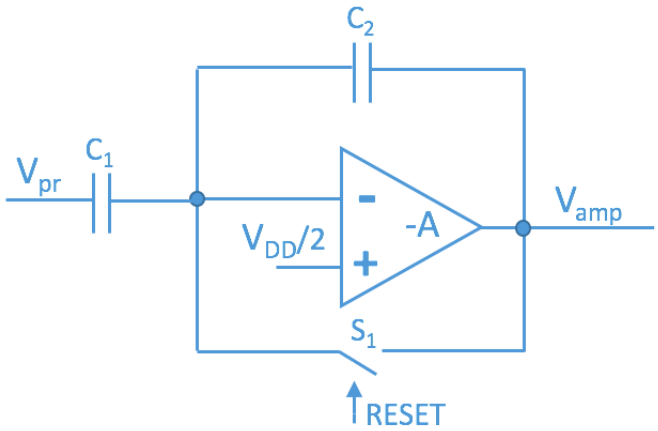
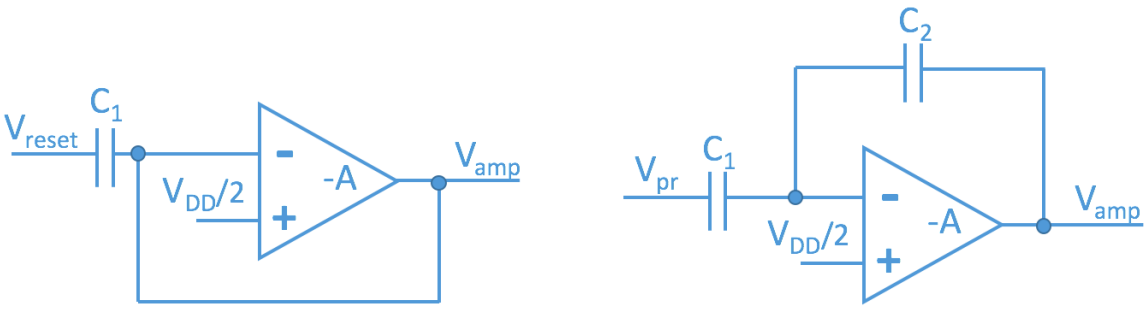


FIGURE 2.6 – Schema of the switched capacitor amplifier.

The relation of the circuit output V_{amp} can be determined by considering two states : the reset state (switch closed) when an event is produced and the switch opened state when the change in light intensity is amplified. These two states are drawn in FIGURE 2.7.



(a) Switch closed.

(b) Switch opened.

FIGURE 2.7 – Switched capacitor amplifier circuit with switch closed and opened respectively.

If the amplifier is considered as ideal, the charge on capacitor C_1 in reset state can be written as EQUATION 2.6:

$$Q_1 = (V_{reset} - \frac{V_{DD}}{2})\ C_1 \tag{2.6}$$

with V_{reset} the V_{pr} value at reset time.

Two cases can be considered when the switch S_1 is open:

- The light intensity increases leading to an increase of voltage V_{pr} and a decrease of voltage V_{amp} due to the negative gain of the amplifier:

$$\begin{aligned} Q_1^{'} &= (V_{pr} - \frac{V_{DD}}{2})\ C_1 \\ Q_2^{'} &= (\frac{V_{DD}}{2} - V_{amp})\ C_2 \\ Q_1 &= Q_1^{'} - Q_2^{'} \\ V_{reset}\ C_1 - \frac{V_{DD}}{2}\ C_1 &= V_{pr}\ C_1 - \frac{V_{DD}}{2}\ C_1 - \frac{V_{DD}}{2}\ C_2 + V_{amp}\ C_2 \\ C_1\ (V_{reset} - V_{pr}) &= C_2\ (V_{amp} - \frac{V_{DD}}{2}) \end{aligned} \tag{2.7}$$

- The light intensity decreases leading to a decrease of voltage V_{pr} and an increase of voltage V_{amp} due to the negative gain of the amplifier:

$$\begin{aligned} Q_1^{'} &= (V_{pr} - \frac{V_{DD}}{2})\ C_1 \\ Q_2^{'} &= (V_{amp} - \frac{V_{DD}}{2})\ \ C_2 \\ Q_1 &= Q_1^{'} + Q_2^{'} \\ V_{reset}\ C_1 - \frac{V_{DD}}{2}\ C_1 &= V_{pr}\ C_1 - \frac{V_{DD}}{2})\ C_1 + V_{amp}\ C_2 - \frac{V_{DD}}{2}\ C_2 \\ C_1\ (V_{reset} - V_{pr}) &= C_2\ (V_{amp} - \frac{V_{DD}}{2}) \end{aligned} \tag{2.8}$$

From EQUATIONS 2.7 and 2.8, the output voltage V_{amp} can be written as EQUATION 2.9:

$$V_{amp} = \frac{V_{DD}}{2} + \frac{C_1}{C_2}\ (V_{reset} - V_{pr}) \tag{2.9}$$

The SCA circuit amplifies therefore by C_1/C_2 the change of V_{pr} from the last reset. This change is then added to $V_{DD}/2$.

Now that the output of the SCA block is determined, guidelines on the sizing of the different elements composing the circuit are given, starting with the capacitors.

2.4.1 Capacitors

The SCA block is composed of two capacitors that should be chosen in order to minimize the pixel area. Moreover, the ratio between the two capacitors is fundamental as it fixes the amplification gain. A too large gain also amplifies noise leading to false events. However, a too low gain does not amplify enough the change in intensity and the comparators can then not detect events. Finally, the ratio should also be chosen for layout facilities [39]. Putting all together, a ratio of 15 between the two capacitors should be adapted for a DVS pixel. Its corresponding layout is schematized in FIGURE 2.8.

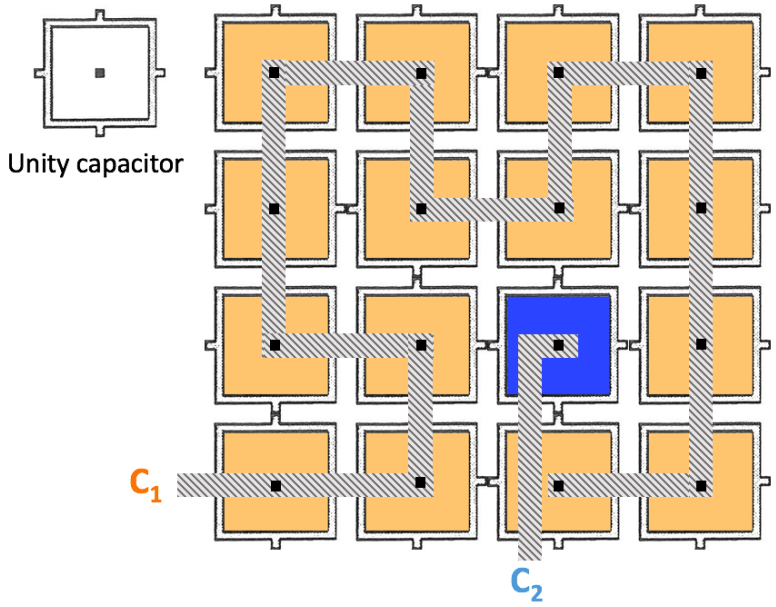


FIGURE 2.8 – Capacitor layout for matching issues.

The use of a unity capacitor allows to improve the matching between the two capacitors. The capacitor C_1 is constructed with 1 capacitor unit and the capacitor C_2 with 15 capacitor units. With this common centroid structure, the ratio between the two capacitors is then well controlled. Moreover, capacitor units are placed in the layout in order to obtain the most symmetrical shape. In this way, the surrounding effects act on the capacitor units more symmetrically. The use of 16 capacitor units allows to construct a squared layout. The gain of 15 is then a good ratio for a symmetrical layout. Moreover, capacitor C_1 is placed in a central position as it is composed of only one unit. Hence, its surrounding effects (as the effect of oxide thickness) are reduced. The capacitor C_2 is composed of 15 units, allowing a mean of each non-ideal effect.

With this configuration, the matching between the two capacitors is then maximized. However, to ensure the same environment to each capacitor unit, dummies can be added all around the squared shape. The price to pay to this homogeneous etching improvement is a non-negligible pixel area increase. As this feature is one of the three figures of merit targeted in this study, dummies are not added in the capacitors layout [39].

2.4.2 Amplifier

The SCA circuit is composed of one amplifier. Firstly, the amplifier should have a large slew rate (SR) in order to quickly reset its output when an event is detected. Actually, the output voltage V_{amp} should be at $V_{DD}/2$ before the end of the reset. Therefore, the slew rate is an important parameter to take care in the design. Then, the gain of the amplifier is also important as it defines the V_{amp} offset. If the gain is too low, the amplifier negative input is not at $V_{DD}/2$. Therefore, after a reset, the voltage V_{amp} does not start at $V_{DD}/2$. The architecture of the amplifier used in the SCA is a single-stage CMOS operational transconductance amplifier [41]. The schema of such an amplifier is represented in FIGURE 2.9.

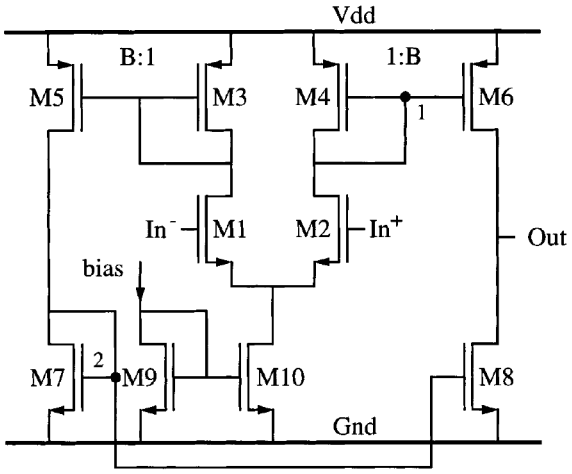


FIGURE 2.9 – Single stage OTA architecture (from [41]).

Its DC open-loop gain, bandwidth gain and slew rate are given by EQUATIONS 2.10, 2.11 and 2.12 respectively [41].

$$A_{v0} = \frac{Bg_{m1}}{g_{d6} + g_{d8}} = V_{ea}(g_m/I_D)_1 \tag{2.10}$$

with $V_{ea} = V_{ea6}V_{ea8}/(V_{ea6} + V_{ea8})$

$$GBW = B(g_m/I_D)_1 \frac{I_{D1}}{2\pi C_L} \tag{2.11}$$

with C_L the load capacitance which is here dominated by C_2.

$$SR = \frac{2I_{D1}B}{C_L} \tag{2.12}$$

In this way, to maximize the SR, the load capacitance should be minimized. Moreover, if the bias current or/and the parameter B of the amplifier increase, the slew rate increases by the same ratio. However, increasing the bias current and/or B also increases the total power consumption. A trade-off exists then between the slew rate and the power consumption. The design flow of such an amplifier is presented in ANNEXE B. For the complete OTA study see [39].

2.4.3 Switch

The switch is the last element composing the SCA circuit. A way to implement it is to use a NMOS transistor designed to minimize the charges injection. The phenomena of charges injection during the reset signal is illustrated in FIGURE 2.10.

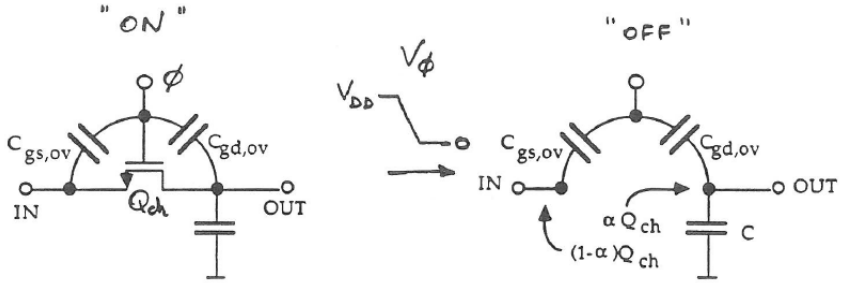


FIGURE 2.10 – Charges injection (from [39]).

When the switch is OFF, the capacitance $C_{gd,ov}$ discharges its accumulated charges in the load capacitance C according to EQUATION 2.13.

$$\Delta Q_{gd,ov} = -C_{gd,ov} V_{DD} \tag{2.13}$$

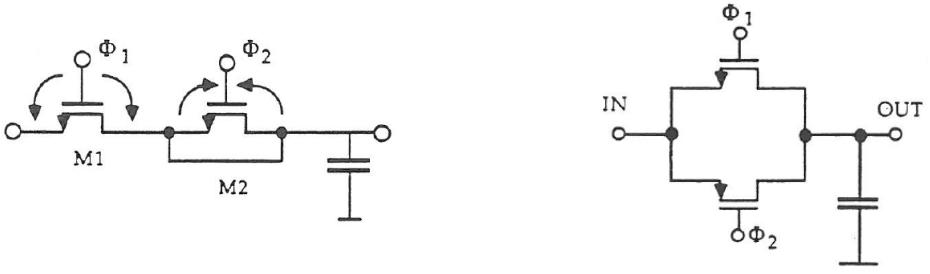
An error on the output voltage is then produced. Moreover, the accumulated charges in the channel are redistributed towards both ends depending on the relative impedance seen. The channel charges can be expressed as EQUATION 2.14.

$$Q_{ch} = C_{ox} W L (V_{DD} - V_{T0} - n V_{IN}) \tag{2.14}$$

Hence, the charges injected in the circuit can be expressed as EQUATION 2.15 [39, 42].

$$Q_{inj} = \alpha Q_{ch} + \Delta Q_{gd,ov} \tag{2.15}$$

To minimize the charges injection, a small transistor size should therefore be used. The addition of a dummy switch or a complementary switch further minimize the charges injection phenomena. These two improvements are respectively represented in FIGURE 2.11a and 2.11b and described hereunder.



(a) Dummy switch.

(b) Complimentary switch.

FIGURE 2.11 – Charges injection cancellation with Φ_1 and Φ_2 two clocks from opposite sign (from [39]).

Dummy switch: The dummy switch M2 in FIGURE 2.11a is used to attract the injected charges from switch M1. The switch M1 has only one internal capacitance on the pre-output voltage (the node between M1 and M2). The dummy switch M2 has two internal capacitances on the same node (as the drain and the source are connected with each other). Therefore, to cancel the charges injection, size of M1 should be twice the size of M2. Moreover, the success of charges injection cancellation with a dummy switch is restricted as V_{IN} and the pre-output voltage are not at the same voltage leading to different charges injections in M1 and M2.

Complementary switch: The complementary switches in FIGURE 2.11b work as follows: when the NMOS transistor receives a positive clock pulse, the PMOS receives a negative one. If the overlap capacitances between PMOS and NMOS match, the effects of charges injection are canceled. The use of complementary switches is then effective only when all parameters and voltages are symmetrical. In the SCA circuit, V_{IN} corresponds to $V_{DD}/2$ and V_{OUT} to V_{amp}. As V_{amp} differs from $V_{DD}/2$ of "$V_{DD}/2-$Threshold" or "$V_{DD}/2+$Threshold", the voltages can be considered sufficiently symmetrical.

The complementary switch is the option that is retained in this work as it gives the best performances (see SECTION 3.4.3).

2.5 Comparators

To detect a change in light intensity and to produce the corresponding event, two comparators are used. These comparators are independent from each other and are realized with the same design of the SCA operational amplifier. However, as the specifications for the comparators are different from the ones in the switched capacitor amplifier circuit, their design differs.

Firstly, the slew rate of comparators is less important than in the SCA circuit. Actually, if ON and OFF events are produced with a relatively small delay, the impact on the minimum contrast sensitivity can be considered negligible due to the gain introduced by the SCA block. In this way, it is possible to win power with well-design low-power comparators. Then, the comparator gain should be large enough to produce an event each time a threshold is reached. However, if the events are produced a little bit below the threshold or if the threshold is a little bit exceeded, the error on V_{pr} is also only impacted by a ratio of C_2/C_1 thanks to the SCA. Finally, if the error on thresholds is constant, a way to reach good comparator performances is to add a correction on the threshold with an offset.

2.6 Logic

When an event is produced, the logic circuit is used to reset the output voltage of the SCA circuit. In this way, the voltage V_{amp} is reset to $V_{DD}/2$. The logic is composed of 4 inverter gates. Two are used to produce a true digital ON event and the two others for the digital OFF event. Moreover, the logic contains an OR gate taking as input ON events and OFF events. The output of the OR gate is the reset signal. This signal should be long enough to allow the reset of V_{amp} to $V_{DD}/2$. However, if it is too long, the latency between two events is reduced. As the brain works in the sub-milliseconds latency, a reset signal of 100 μs is already a good biomimetic. The design of the four inverter gates fixes the duration of the reset signal. Finally, the logic circuit contains an inverter gate to produce the non-reset signal used in the complementary switch of the SCA block. The complete logic chain is schematized in FIGURE 2.12. The AER logic is added in the figure to show how it has to be connected with.

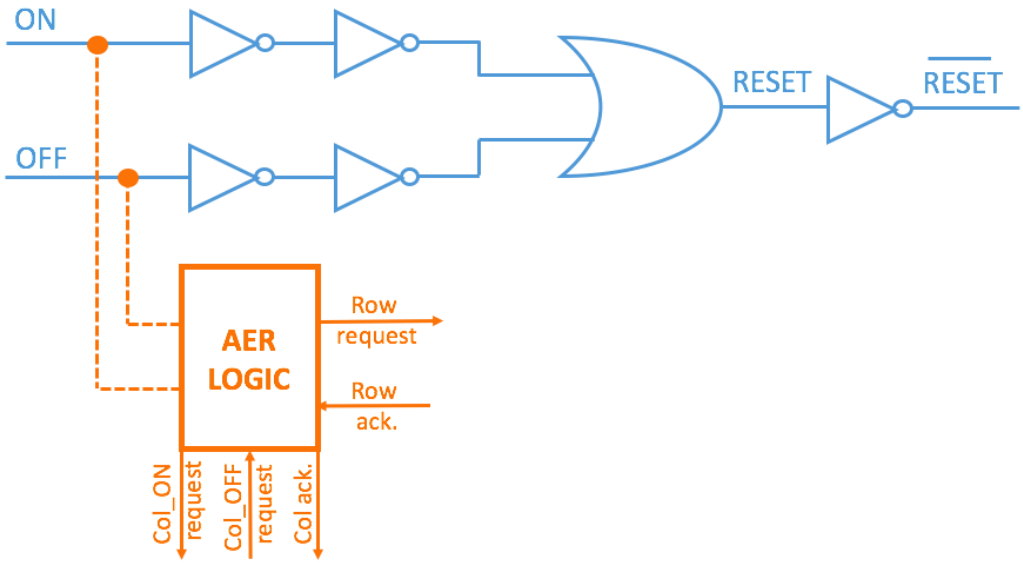


FIGURE 2.12 – Schema of the logic chain. In orange, the connections for a future implementation of the AER logic.

The principles of operation of the AER protocol used in the DAVIS are represented in FIGURE 2.13. The AER row/column logic, arbiter and address encoder are placed outside of the pixel array. When an event is generated by a pixel, it drives its row request line (shared by all pixels in a row). Among all active requesting rows, the AER row arbiter chooses one of them and acknowledge it with the row acknowledge signal. All pixels producing an ON/OFF event in the chosen row make an ON/OFF request to the AER column arbiter. An asynchronous AER handshake state machine transmits the row address to a receiver chip as well as the requesting columns, starting from the leftmost one.

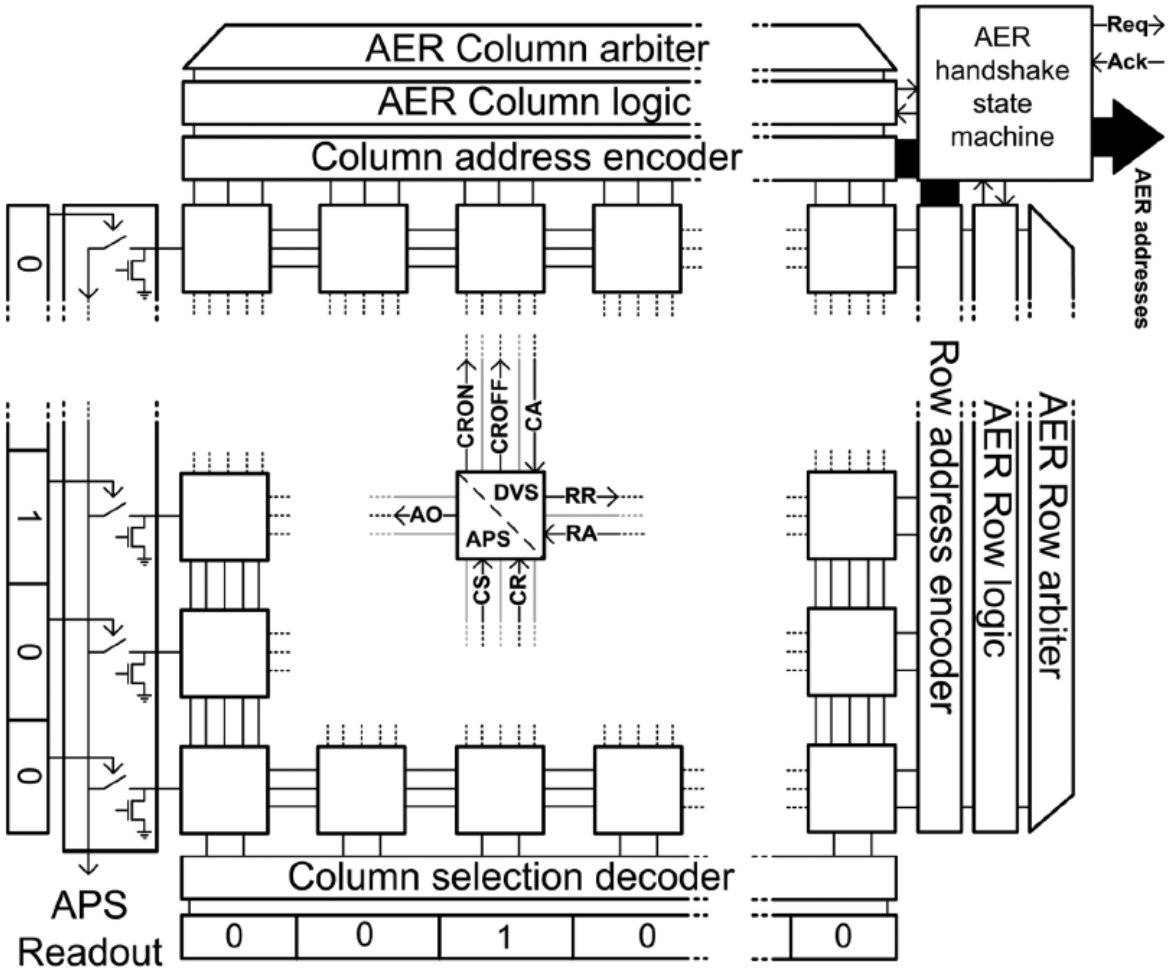


FIGURE 2.13 – Principles of operation of the AER protocol used in the DAVIS (from [5]).

Chapter 3

Pixel design

Contents

A design of the neuromorphic pixel in a 0.18 µm *CMOS technology is proposed in this chapter. Firstly, the technology is rapidly studied and its principal characteristics are pointed out. The photoreceptor circuit is then sized. Afterwards, a design of the switched capacitor amplifier circuit is proposed. Finally, the comparators are designed.*

The pixel implementation proposed in this study is realized in the same technology a the CAMEL: the 0.18 µm CMOS technology. Moreover, a same supply voltage is used, that is, 0.75 V. Therefore, this work is compatible with the imager from UCL [1]. Hence, a supply constraint is added to this study compared to the DAVIS.

3.1 Technology characteristics

Before the pixel design, it is important to study briefly the technology. Therefore, this section presents different characteristics of the core and IO transistors available in a 0.18 µm CMOS technology. As an imager sensor requests to play with low currents, transistors sizes are small. The length of the two transistors studied in this section is fixed at 800 nm and their width at 240 nm. Only NMOS transistors are described in this section but PMOS transistors can be studied similarly.

3.1.1 Core transistors

Supply voltage: The core transistor can be supplied until 1.8 V.

Length and width: The transistor length can be fixed from 180 nm to 50 µm and its width from 240 nm to 100 µm.

gm/ID characteristic curve: The gm/ID characteristic curve in various transistor gate voltages is represented in FIGURE 3.1. The gm/ID maximum value is reached at $V_{GS} = 0$ V and corresponds to 37 V^{-1}.

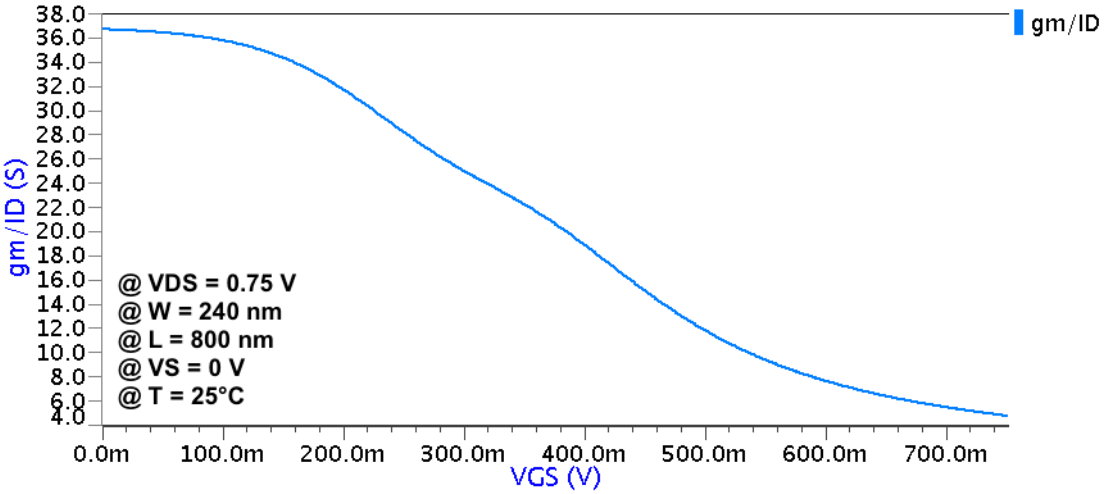


FIGURE 3.1 – gm/ID characteristic curve of NMOS core transistors.

Subthreshold slope factor *n*: The subthreshold slope factor (n) can be calculated with EQUATION 3.1 [43].

$$S = n\left(\frac{kT}{q}\right) ln(10) \tag{3.1}$$

with S the slope factor (or subthreshold swing) in volts per decade, k the Boltzmann constant and q the electronic charge. At room temperature and at unity subthreshold slope factor, the slope factor is equal to 60 mV per decade [43]. With FIGURE 3.2, the slope factor can be approximated as 68 mV per decade. The corresponding subthreshold slope factor is then $n = 1.13$.

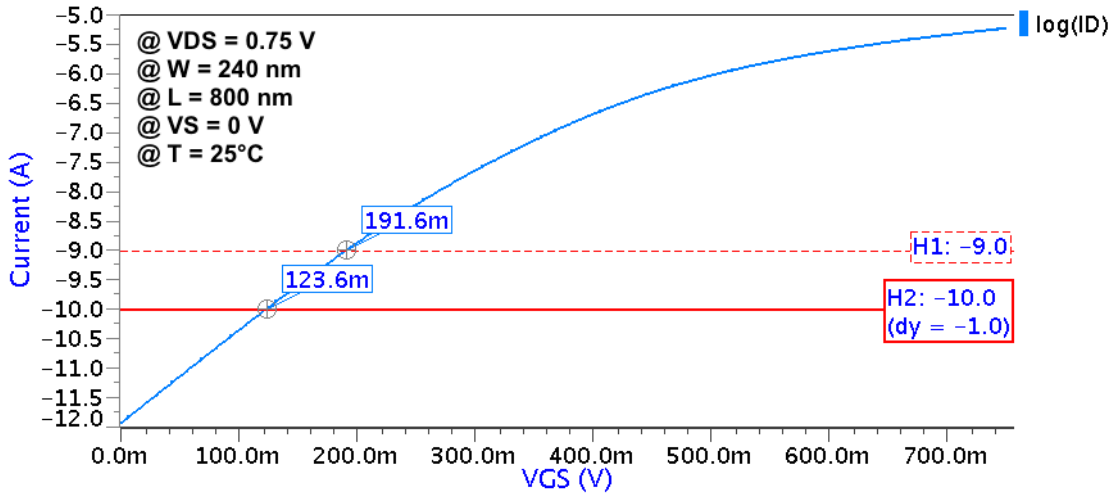


FIGURE 3.2 – Logarithm of NMOS core transistors drain current in various gate voltages.

3.1.2 IO transistors

Supply voltage: The maximum supply voltage of an IO transistor is 3.3 V. Actually, thanks to its thicker oxide layer, it can support a higher supply voltage than core transistors.

Length and width: The transistor length can be fixed from 340 nm to 5 µm and its width from 240 nm to 100 µm.

gm/ID characteristic curve and subthreshold slope factor: In the same way as the core transistor, the gm/ID characteristic curve as well as the logarithm of the drain current in various gate voltages are represented in FIGURE 3.3. The corresponding slope factor is 76 mV per decade. According to EQUATION 3.1, subthreshold slope factor of an IO transistor is then $n = 1.26$.

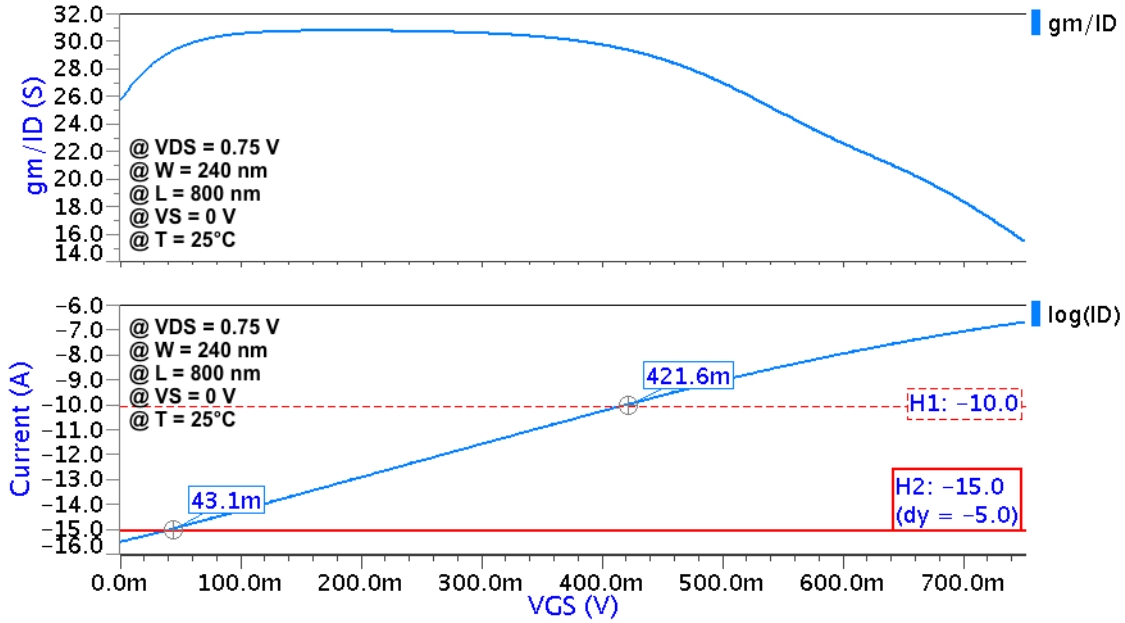


FIGURE 3.3 – gm/ID characteristic curve (top) and logarithm of the drain current (down) for a NMOS IO transistor in various gate voltages.

Summary

The different technology characteristics are summarized in TABLE 3.1.

TABLE 3.1 – Characteristic of core an IO transistors in a 0.18 μm^2 technology.

	NMOS core transistor	NMOS IO transistor
Maximum supply voltage	1.8 V	3.3 V
Minimum length	180 nm	340 nm
Maximum length	50 µm	50 µm
Minimum width	240 nm	240 nm
Maximum width	100 µm	100 µm
Maximum gm/ID value	37 V^{-1}	31 V^{-1}
Subthreshold slope factor n	1.13	1.26

3.2 Photoreceptor circuit

The photoreceptor circuit is designed and simulated in this section. As a reminder, this circuit takes care of the transduction from the sensed light signal into an electrical signal. It is recalled in FIGURE 3.4 with its different parts highlighted.

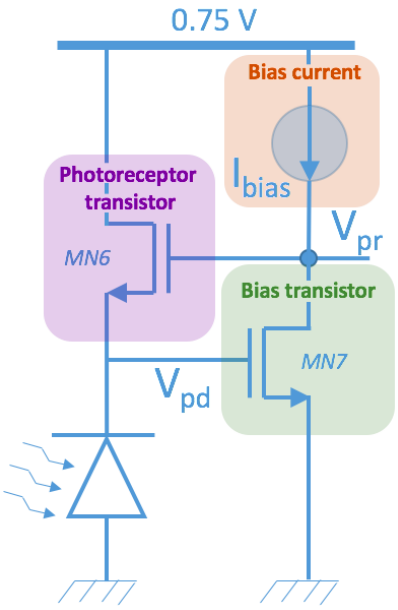


FIGURE 3.4 – Schema of the photoreceptor circuit responsible for the transduction from the photocurrent to the voltage V_{pr}.

To design this architecture, the p^+/n-well/p-sub type photodiode in a 0.18 µm CMOS technology is firstly studied in order to fix the photocurrent range detectable by the photoreceptor circuit. According to this range, the photoreceptor transistor and the photodiode are sized. The leakage currents of the circuit are then studied. Finally, the bias transistor as well as the bias current are sized in order to fix the bias point V_{pd}. During the design, the variations in process and temperature are studied and a Monte-Carlo simulation with 10,000 runs is realized to validate the different results.

3.2.1 Range of photocurrent

As discussed in SECTION 2.3.1, the most suitable photodiode type is the p^+/n-well/p-sub type as it achieves the highest responsivity. In the same section, the range of illuminance is fixed. As a reminder, the illuminance can be expressed as EQUATION 3.2:

$$1\ \mathrm{lx} = \frac{1}{683}\ \mathrm{W/m^2} \tag{3.2}$$

To design the photoreceptor circuit efficiently, it is fundamental to know the specifications on the photocurrent beforehand. To convert the level of illuminance into the corresponding photocurrent, EQUATION 3.2 is used as well as FIGURE 3.5. This graph gives the responsivity in $[Acm^{-2}/Wcm^{-2}]$ for a p^+/n-well/p-sub type photodiode in a 0.18 µm CMOS technology [34].

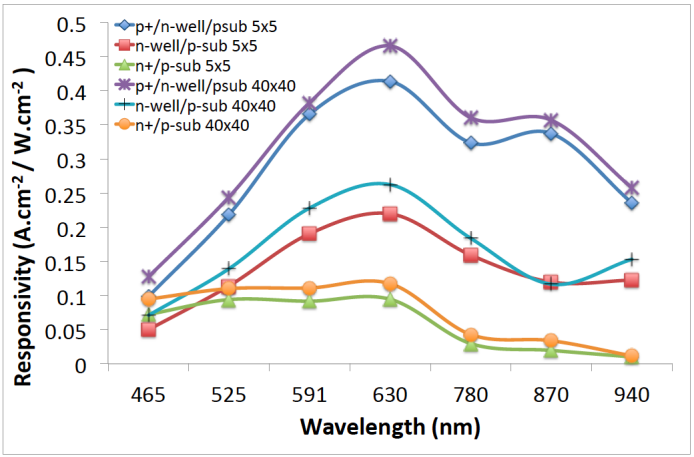


FIGURE 3.5 – Responsivity comparison of different photodiode types at different diffusion area (from [34]).

According to it, responsivity of a p^+/n-well/p-sub type photodiode for a wavelength of 555 nm is 0.3 $\text{Acm}^{-2}/\text{Wcm}^{-2}$. The conversion from an illuminance to a photocurrent per unit of area can then be realized using EQUATION 3.3.

$$1\ \text{lx} = \frac{0.3}{683} \times 10^{-12}\ \text{A}\mu\text{m}^{-2} \tag{3.3}$$

The different values of illuminance and their respective conversion to photocurrent per unit of area are summarized in TABLE 3.2. Hence, the photoreceptor transistor should detect a photocurrent (per unit of photodiode diffusion area) from 4.4 $\text{aA}\mu\text{m}^{-2}$ to 44 $\text{pA}\mu\text{m}^{-2}$. The photodiode area is chosen later as it depends on the photoreceptor transistor performances.

TABLE 3.2 – Norm of illuminance intensities and their corresponding photocurrent per unit of area [38].

	Illuminance	Photocurrent per unit of area
In full sunshine	100,000 lx	44 $\text{pA}\mu\text{m}^{-2}$
In an office	500 lx	220 $\text{fA}\mu\text{m}^{-2}$
In an illuminated street	50 lx	22 $\text{fA}\mu\text{m}^{-2}$
The DAVIS minimum illuminance	0.01 lx	4.4 $\text{aA}\mu\text{m}^{-2}$

3.2.2 Photoreceptor transistor

Now that the photocurrent range per unit of area is determined, the photoreceptor transistor is sized. As mentioned before, the photocurrent values sensed by the photodiode is low. Therefore, the photoreceptor transistor should be designed in weak inversion. Moreover, as this transistor achieves the transduction from the photocurrent to the voltage V_{pr}, it determines the pixel dynamic range. The range of V_{pr} should then be maximized. However, according to SECTION 2.3.3, to keep the photoreceptor transistor in active region, the output voltage V_{pr} should be included between the bias voltage and V_{DD}. A minimum value of V_{pd} maximizes then the pixel dynamic range but a too low value could be an issue during a Monte-Carlo simulation. Putting all together, a polarization voltage of 150 mV seems to be a good trade-off.

Design of an IO photoreceptor transistor

In a first attempt to design the photoreceptor transistor, a core transistor is used. To choose the most suitable photoreceptor transistor size, its drain current variation in various gate voltages V_{pr} is simulated in FIGURE 3.6 for different core transistor sizes. During the simulation, the width and length range is limited to 800 nm as the pixel area should be minimized.

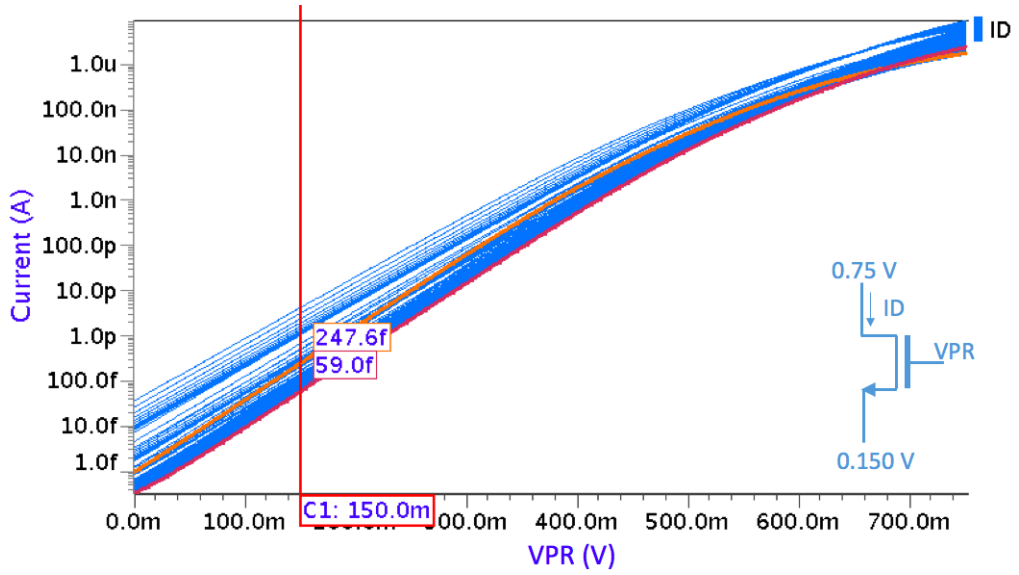


FIGURE 3.6 – Drain current variation in various gate voltages V_{pr} for different photoreceptor core transistor widths and lengths. Orange curve is obtained with W=240 nm and L=800 nm. Red curve is obtained with W=450 nm and L=550 nm.

From EQUATION 2.3, a minimum current is achieved with small transistor width, large transistor length and large threshold voltage. For a width of 240 nm and a length of 800 nm, the current is then intended to be minimized. However, the corresponding threshold voltage is 410 mV. For a width of 450 nm and a length of 550 nm, the threshold voltage increases to 490 mV. According to FIGURE 3.6, a transistor with width of 450 nm and length of 550 nm reaches the lowest current at V_{GS}= 0 V.

According to EQUATION 3.3, an illuminance of 0.01 lx corresponds to a photocurrent of 48 aA if a photodiode diffusion area of 11 µm^2 is considered (corresponding to the CAMEL photodiode area). However, the minimum drain current obtained in FIGURE 3.6 at V_{GS} = 0 V is 59 fA. Hence, the specification on the minimum photocurrent is not respected with this transistor design. A way to decrease this minimum drain current to 48 aA is to drastically increase the photodiode area and/or the photoreceptor transistor length. However, as pixel area is one of the three figures of merit, this huge increase is not conceivable in this study. According to EQUATION 2.4, another way to fix this issue is to use a transistor with higher threshold voltage. This is coherent with what is said in the DAVIS's paper [5]. Hence, in a second attempt to design the photoreceptor transistor, an IO transistor is used.

Design of an IO photoreceptor transistor

Similarly to the core transistor, the drain current variation in various gate voltages V_{pr} is simulated in FIGURE 3.6 for different core transistor sizes.

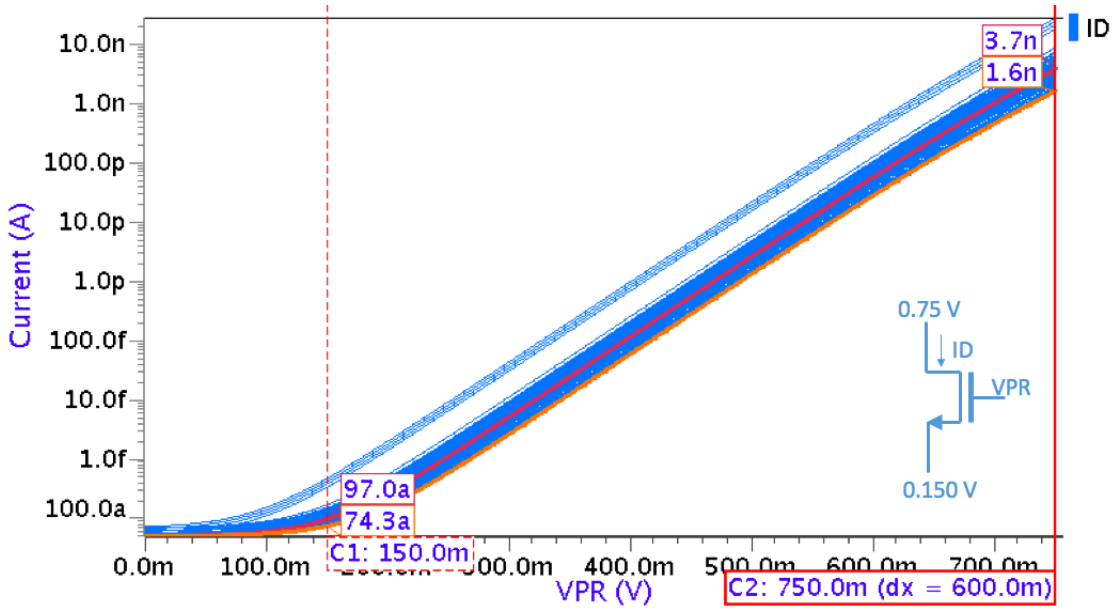


FIGURE 3.7 – Drain current variation in various gate voltages V_{pr} for different photoreceptor IO transistor widths and lengths. Red curve is obtained with W=240 nm and L=800 nm. Orange curve is obtained with W=240 nm and L=3 µm.

Red curve shows a drain current of 97 aA at V_{GS}= 0 V. This drain current can be further decreased to 74 aA if the transistor length increases to 3 µm. However, the price to pay for this improvement is a larger pixel area. A final way to decrease further this current is to decrease the bias voltage V_{pd}. However, as mentioned previously, some issues could append during the Monte-Carlo simulation. For this study, an IO photoreceptor transistor of 240 nm x 800 nm and a V_{pd} voltage of 150 mV are then considered as a good trade-off.

3.2.3 Photodiode area

If a photodiode diffusion area of 11 μm^2 is considered, from EQUATION 3.3, an illuminance of 0.01 lx corresponds to a photocurrent of 48 aA. However, this value is below the drain current obtained at V_{GS}= 0 V for an IO photoreceptor transistor of 240 nm x 800 nm. Hence, the photodiode diffusion area is increased to 25 μm^2, giving a photocurrent of 110 aA at 0.01 lx. This increase has a non-negligible negative impact on the pixel area. However, the impact on the fill factor is positive. As the DAVIS uses a photodiode diffusion area of 75 μm^2, the use of a photodiode area of 25 μm^2 seems suitable for this study. An illuminance of 100,000 lx corresponds then to a photocurrent of 1.1 nA. As the drain current of the photoreceptor circuit reached 3.7 nA at $V_{GS} = V_{DD}$, all the specifications on the photocurrent are respected.

A summary of the range of photocurrent created by a photodiode with diffusion area of 25 μm^2 in different illuminance is given in TABLE 3.3.

TABLE 3.3 – Norm of some illuminance intensities and their corresponding photocurrent for a photodiode area of 25 μm^2 [38].

	Illuminance	Photocurrent per unit of area	Photocurrent for a photodiode of 25 μm^2
In full sunshine	100,000 lx	44 pAμm^{-2}	1.1 nA
In an office	500 lx	220 fAμm^{-2}	5.5 pA
In a illuminated street	50 lx	22 fAμm^{-2}	550 fA
The DAVIS minimum illuminance	0.01 lx	4.4 aAμm^{-2}	110 aA

Saturation current: The range of photocurrent included between 110 aA and 1.1 nA is called the *saturation current* for the rest of this work.

Now that the photoreceptor transistor as well as the photodiode are sized, the bias point is fixed thanks to the bias transistor and the bias source. However, before going to their design, it is interesting to study the dark current of the photoreceptor circuit.

3.2.4 Dark current

In an APS imager, sources of dark current are the photodiode leakage, the reset leakage and the gate leakage. As no reset is performed on the photoreceptor circuit, the reset leakage is not part of the DVS dark current. However, the bulk current from the photoreceptor transistor is a source of dark current as it is not a useful signal. The DVS dark current is then composed of the photoreceptor transistor bulk leakage and the photodiode leakage. Those currents are added to the photocurrent generated by the photodiode to form the drain current of the photoreceptor transistor as it is schematized in FIGURE 3.8. As the output voltage V_{pr} follows a logarithmic relationship with the drain current, if the dark current is high, a low value of photocurrent is not sensed with the same sensitivity. Hence, a high dark current decreases the pixel sensitivity at low light intensities.

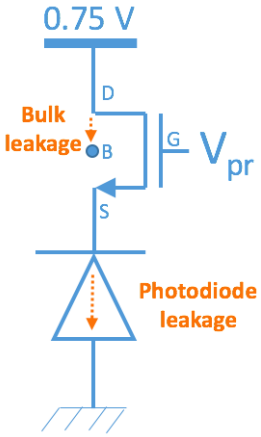


FIGURE 3.8 – Dark current of the photoreceptor circuit.

Bulk leakage

A current flows through the bulk of the photoreceptor transistor. Bulk currents of an IO and a core photoreceptor transistor are simulated in various temperatures in FIGURE 3.9. The graph shows that the bulk current generated by the IO transistor is lower than the one generated by the core transistor, especially in high temperatures. The use of an IO photoreceptor transistor is then, one more time, a better choice. The bulk current for this kind of transistor reaches 60 aA at 25°C. At 85°C, the bulk current increases to 150 fA reducing further the pixel sensitivity at low light intensities. As 150 fA corresponds already to an illuminance of 10 lx, this temperature is not suitable for the photoreceptor circuit. A maximum operating temperature of 50°C, giving a bulk current of 2.2 fA and corresponding to an illuminance of 0.2 lx, is then considered.

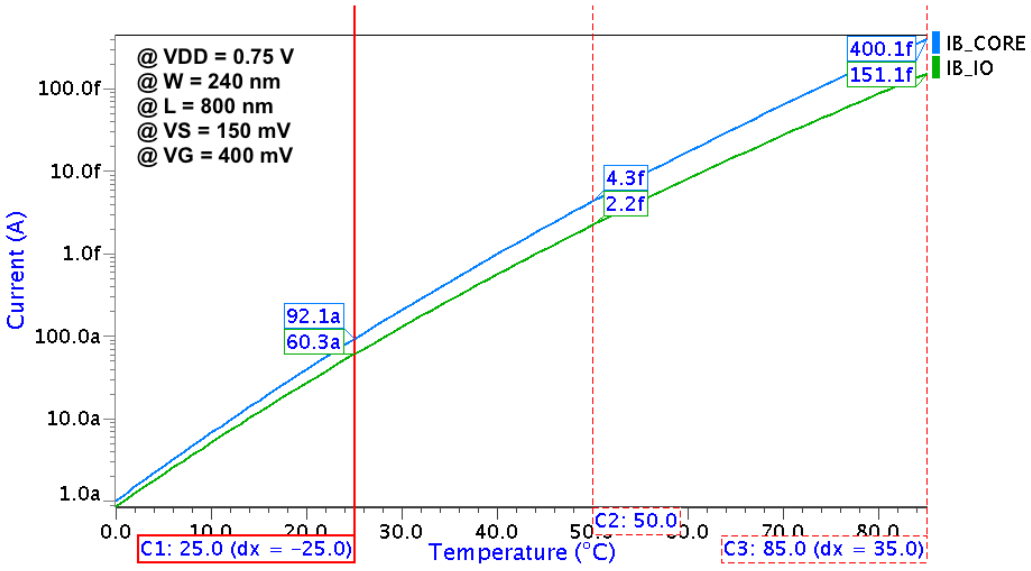


FIGURE 3.9 – Bulk current of an IO and a core photoreceptor transistor of 240 nm x 800 nm in various temperatures.

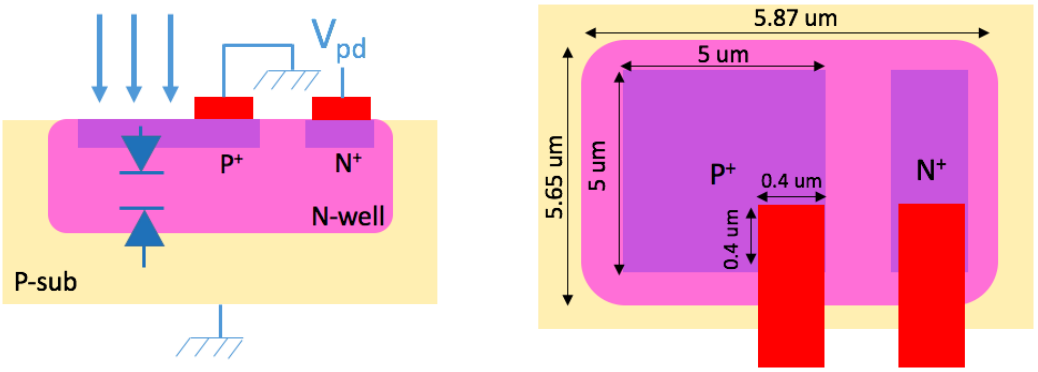
Photodiode leakage

The article of G. Köklü allows to get an idea of the dark current produced by the photodiode [34]. Actually, for a p^+/n-well/p-sub type photodiode with a 5x5 µm^2 diffusion area, they obtained a junction capacitance of 24.37 fF. Moreover, the corresponding dark signal was 75 mV/ sec. This dark signal was generated by keeping the photodiode under dark conditions and by calculating the slope of the voltage output. Although this measured dark signal was not only due to the dark current but also due to the reset noise and the photon shot noise [34], it gives a good idea of the level of dark signal. To calculate the corresponding dark current, EQUATION 3.4 can be used:

$$I = C \frac{dV}{dT} = 1.8 \text{ fA} \tag{3.4}$$

with C the junction capacitance, $\frac{dV}{dT}$ the dark signal and I the dark current.

The dark current can now be simulated for the photodiode used in the photoreceptor circuit. As the p^+/n-well/p-sub type photodiode is composed of two junctions (from p^+ to n-well and from n-well to p-sub), the two corresponding photodiode models are put in parallel (see ANNEXE C). Hence, photodiode schema in FIGURE 3.10 is reproduced. As metal contacts take only 0.16 µm^2, their area in the p^+ layer can be neglected.



(a) Side view. (b) Upper view.

FIGURE 3.10 – Side and upper views of the p^+/n-well/p-sub type photodiode with the metal layer represented in red.

Firstly, the simulation is realized with the initial value of the gmin parameter: gmin=10^{-12} S. However, as represented in FIGURE 3.11, this value does not give the true value of the dark current as it is too huge to furnish enough precisions. For a gmin value of 10^{-24} S, the simulation can be considered as accurate. This value is then used for this study. With gmin=10^{-24} S, a dark current of 160 aA is obtained at 25°C and with the photodiode polarized at 150 mV. However, this simulated dark current is overestimated as p^+ layer plays the role of a protective layer by reducing the number of free interface states, leading to a reduction in the dark current in the n-well/p-sub junction [19]. This effect is not taken into account during the simulation of the two photodiodes put in parallel.

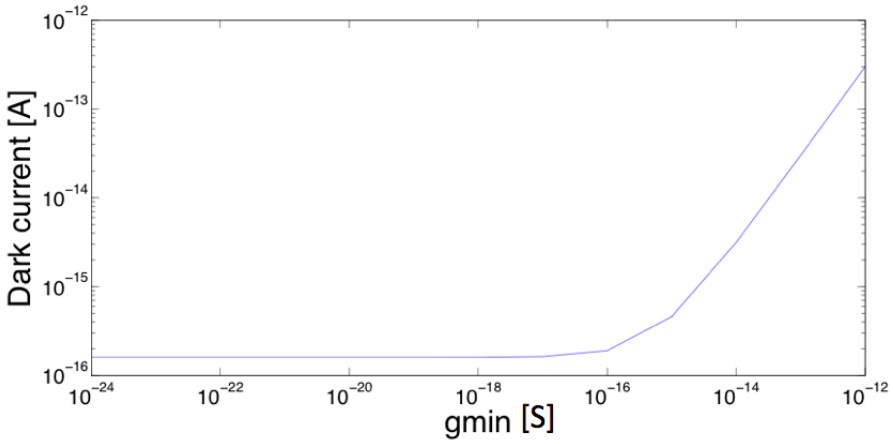


FIGURE 3.11 – Simulation of the photodiode leakage for a p^+/n-well/p-sub type photodiode with diffusion area of 25 µm^2 for different values of the gmin parameter.

The simulated value is then not really close to the one obtained before. According to the ATIS's founding paper, the dark current is 15 aA/µm^2, giving another value of dark current [6]. To obtain a precise photodiode dark current value, an experimental measurement is then preferred. However, this measure is not realized in this study.

Although this dark current is not accurate, it is simulated in various temperatures in FIGURE 3.12. As predicted in SECTION 2.3.1, the dark current of the n-well to p-sub junction is higher than the one of the p^+ to n-well junction. Moreover, the graph shows the increase of dark current by a factor of 2 every 7-8°C [15]. At high temperature, the dark current becomes non-negligible. A maximum operating temperature of 50°C is then further motivated.

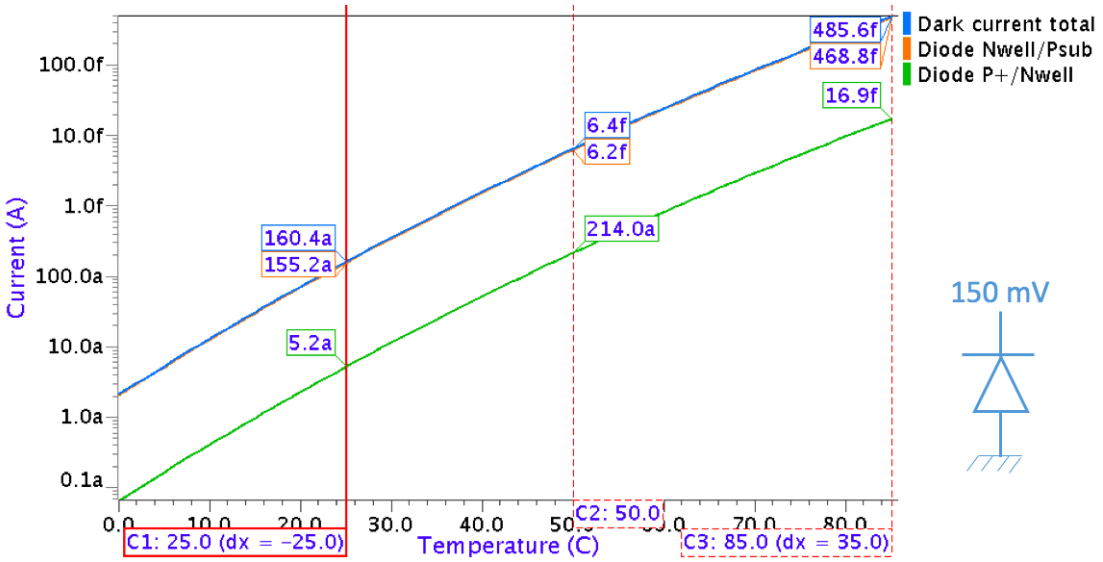


FIGURE 3.12 – Dark current simulation of a 25 µm^2 diffusion area p^+/n-well/p-sub type photodiode at different temperatures.

Finally, the photodiode leakage in various bias points is simulated in FIGURE 3.13. The leakage current stays then constant when the photodiode is polarized above 150 mV [15].

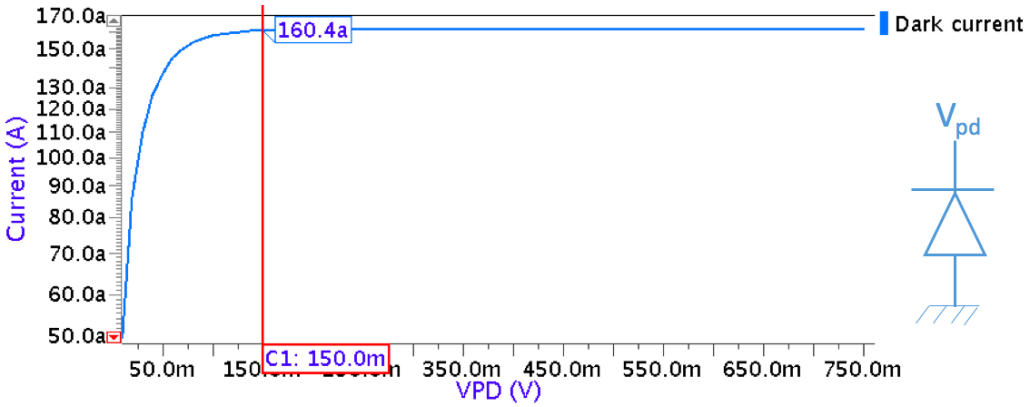


FIGURE 3.13 – Dark current simulation of a 25 µm^2 diffusion area p^+/n-well/p-sub type photodiode at different bias voltages.

3.2.5 Bias point

The bias transistor and the bias current source allow to keep the photodiode at virtual ground. As already discussed, the bias point value is fixed at 150 mV. Concerning the bias current source, a large one improves the photoreceptor circuit slew rate but increases the total power consumption. However, a low one is not recommended for the slew rate, although it decreases power consumption. Trade-off between power consumption and slew rate is discussed in SECTION 5.1.1. In a first attempt, the bias current source is chosen at 50 pA. The photoreceptor circuit is simulated in FIGURE 3.14 in various bias transistor sizes.

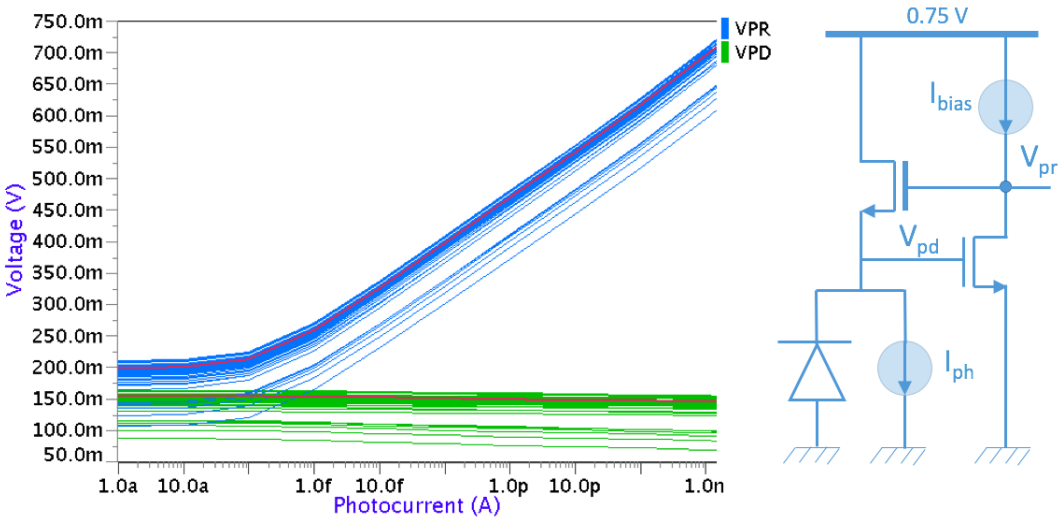


FIGURE 3.14 – V_{pd} (curves in green) and V_{pr} (curves in blue) voltages versus the photocurrent in various bias transistor sizes. In red, V_{pr} and V_{pd} curves obtained with a bias transistor of L=800 nm and W=400 nm.

A bias voltage of 150 mV is reached with a bias transistor of L=800 nm and W=400 nm. For each photocurrent I_{ph}, the voltage V_{pr} is above the voltage V_{pd}. Hence, the photoreceptor transistor is insured to work in active region for the whole saturation current range which is coherent with previous results. Indeed, as say before, the photoreceptor transistor can sense a drain current of 97 aA. As the photodiode leakage current is 160 aA and the bulk leakage current is 60 aA at 25°C, even a photocurrent of 1 aA can be detected by the photoreceptor circuit. The relation between the different currents can be expressed as EQUATION 3.5:

$$I_D = I_{bulk} + I_{dark} + I_{ph} \tag{3.5}$$

with I_{bulk} the bulk current in the photoreceptor transistor, I_{dark} the dark current of the photodiode and I_{ph} the photocurrent produced by the photodiode under light condition. However, due to the dark current, the sensitivity is low for a photocurrent under 100 aA. As the minimum saturation current is 110 aA, this sensitivity issue is not relevant at 25°C.

The ideal bias current source is now replaced with a current mirror. Hence, the bias current source is generated only one time for all pixels in the array. The characteristic curve of photoreceptor circuit is given in FIGURE 3.15 in various photocurrent values.

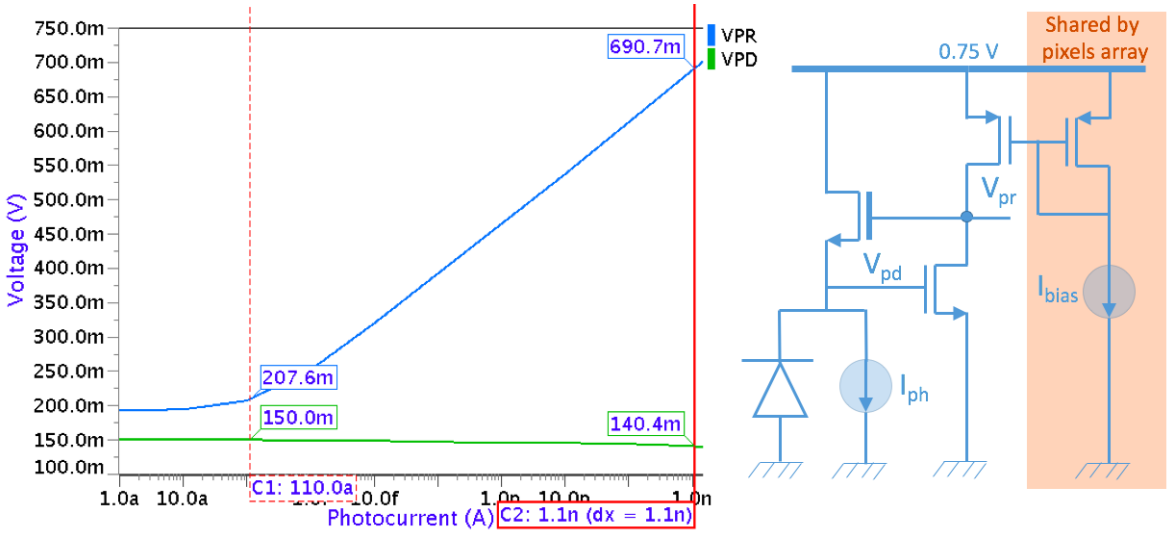


FIGURE 3.15 – Photoreceptor circuit characteristic curves.

Although the bias voltage is not totally constant, the sensitivity stays mostly steady for all the saturation current. The characteristic curves respond then to the different specifications.

Before extracting the different characteristics of the curve, the variations in Process and Temperature are simulated in corners. Moreover, the Monte-Carlo simulation with 10,000 runs is realized on the typical case and on the worst corners to fully validate the curve of transduction from photocurrent to voltage.

3.2.6 Process-Temperature corners simulations

To validate the characteristic curve of the photoreceptor circuit, variations of the global process are applied on the PMOS and NMOS transistors [44]. Global variations affect the speed of all devices realized on the same wafer. The different processes are:

- Fast NMOS - Fast PMOS (FN-FP)
- Slow NMOS - Slow PMOS (SN-SP)
- Fast NMOS - Slow PMOS (FN-SP)
- Slow NMOS - Fast PMOS (SN-FP)

Moreover, a variation on the temperature is realized. Although the industrial temperature range goes from -40°C to 80°C [44], the simulation varies in temperature from -40°C to 50°C. Indeed, in Section 3.2.4 a maximum operating temperature of 50°C is fixed in order to avoid a dark current larger than a photocurrent generated at 0.1 lx. The study of variation in Process-Temperature corners is given in Figure 3.16.

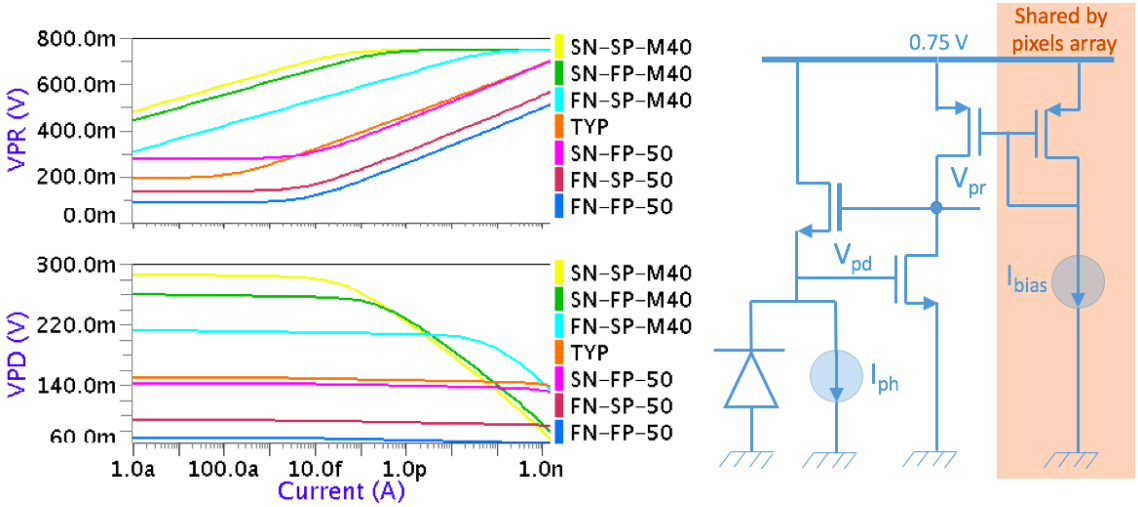


Figure 3.16 – Simulation of the variation in Process-Temperature corners of the photoreceptor circuit.

The simulation shows a variation of the V_{pd} voltage depending on its Process-Temperature corner. The photodiode is then not biased identically for each corner. In Slow NMOS - Slow PMOS and Slow NMOS - Fast PMOS corners at -40°C, the V_{pd} voltage increases to 290 mV and 260 mV respectively. Therefore, their V_{pr} characteristic curve saturates above a photocurrent of 100 fA due to the supply voltage constraint of 0.75 V.

A way to solve this issue is to modify the current mirror circuit architecture to integrate a reference voltage source. Hence, the current reference source I_{bias} is replaced by a voltage reference source V_{ref} fixed at 150 mV.

The study of variation in Process-Temperature corners is realized in FIGURE 3.17 with the integration of such a voltage reference source.

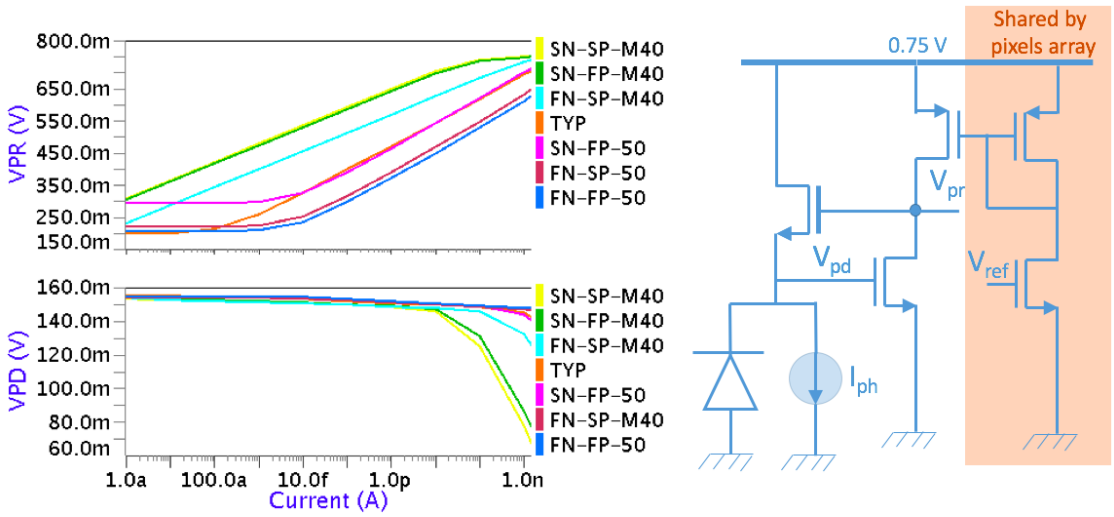


FIGURE 3.17 – Simulation of the variation in Process-Temperature corners of the photoreceptor circuit with a voltage reference source.

With this new current mirror architecture, the photodiode is biased at 150 mV for each variation in Process-Temperature corner. Although an offset on the slope of V_{pr} characteristic curves can be seen, it is not considered as an issue in this study. Actually, only the change in light intensity should be detected and not its absolute value. As V_{pr} characteristic curve slopes at 50°C are steeper than in typical conditions, the sensitivity at 50°C is improved. However, in all corners realized at 50°C, the sensitivity for a photocurrent lower that 10 fA is small. This effect is due to photoreceptor circuit dark current, already explained in SECTION 3.2.4. At -40°C, the sensitivity is decreased as the characteristic curves have a less sleep slope. Moreover, for high photocurrent values (above 100 pA), V_{pr} characteristic curves of Slow NMOS - Slow PMOS and Slow NMOS - Fast PMOS corners at -40°C still show saturation. Hence, using a supply voltage of 0.75 V decreases the total pixel power consumption but the price to pay is saturation, at -40°C, of the photoreceptor characteristic curve above $10,000$ lx.

A possible way to resolve the saturation issue is to decrease the bias voltage V_{pd}. Hence, characteristic curves are shifted downwards solving then the saturation at V_{DD} for a photocurrent above 100 pA. For example, the same Process-Temperature corner simulations are realized in FIGURE 3.18 but this time with a bias voltage of 100 mV. The characteristic curves are all shifted downwards and the saturation at 0.75 V is an issue only above a photocurrent of 1.1 nA. As a photocurrent of 1.1 nA corresponds to the maximum saturation current at full sunshine, saturation is not an issue anymore.

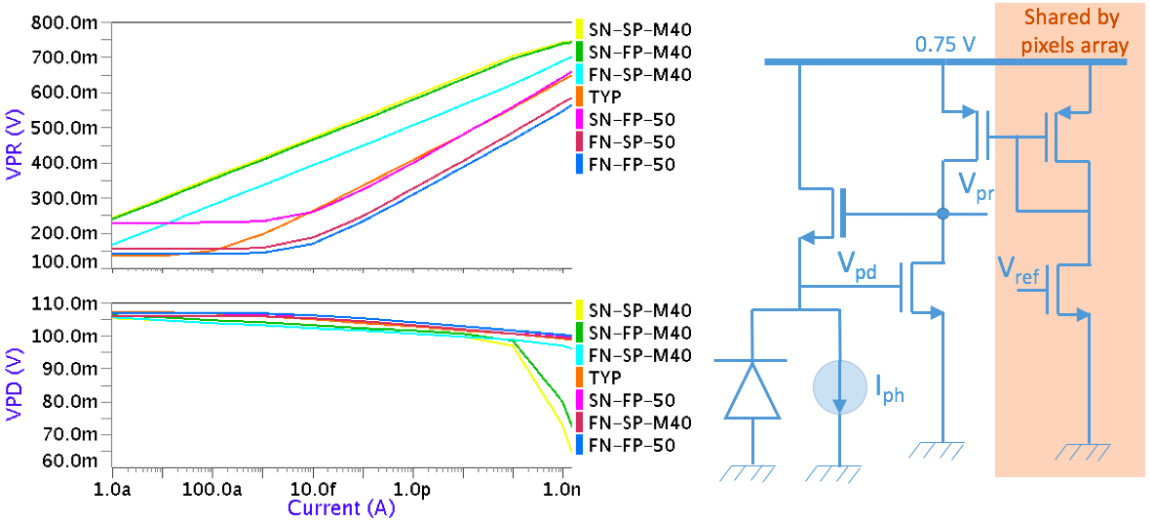


FIGURE 3.18 – Simulation of variation in Process-Temperature corners of the photoreceptor circuit with a voltage reference source at 100 mV.

However, decreasing the bias voltage V_{pd} to 100 mV is not advised for a MC simulation that simulates the process variation. Moreover, a variation on the supply voltage can lead to a problem if a V_{pd} value of 100 mV is used. Hence, a V_{pd} value of 150 mV is kept although the saturation issue at -40°C. A pixel working at -40°C can then detect change in contrast under a light absolute value of 10, 000 lx. Above this value, the pixel does not produce any event.

3.2.7 Monte-Carlo simulation

To validate the photoreceptor circuit in process variation, a Monte-Carlo simulation with 10,000 runs in typical conditions is realized in FIGURE 3.19.

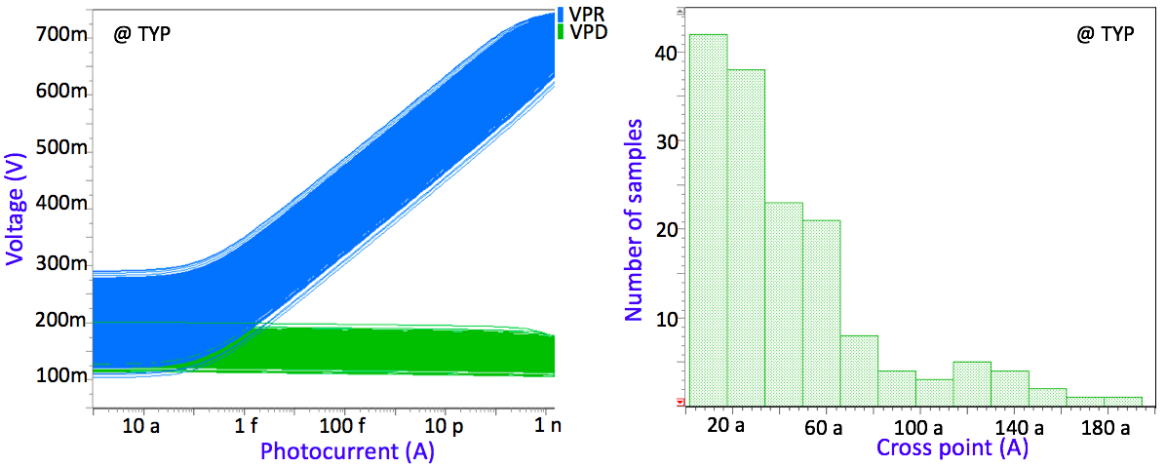


FIGURE 3.19 – Characteristic curves and histogram of the photoreceptor circuit simulated with a Monte-Carlo simulation with 10,000 runs.

The MC simulation shows a variation in the offset of V_{pr} curves in various photocurrent values. However, as explained before, this offset is not an issue in this study as only the change in intensity is detected. Moreover, it shows a constant slope for each V_{pr} curve. Hence, the same sensibility is guaranteed for all runs. The simulation shows also a variation on the biasing point V_{pd}. It varies from 50 mV around its typical value of 150 mV. Hopefully this effect has no impact on the V_{pr} curve. Finally, a histogram of the cross point between V_{pd} and V_{pr} is plotted. Only 150 over 10,000 runs give a cross point between the two voltages for a photocurrent range from 1 nA to 1.1 nA. Moreover, only 20 of them (0.2% of 10,000 runs) shows a cross point above the minimum saturation current of 110 aA. Hence, the minimum saturation current is guaranteed to be sensed in 99.8% in typical conditions.

To study the saturation issue in process variations, a Monte-Carlo simulation with 10,000 runs is realized on the Slow NMOS - Slow PMOS corner at -40°C. The result of the simulation is represented in FIGURE 3.20.

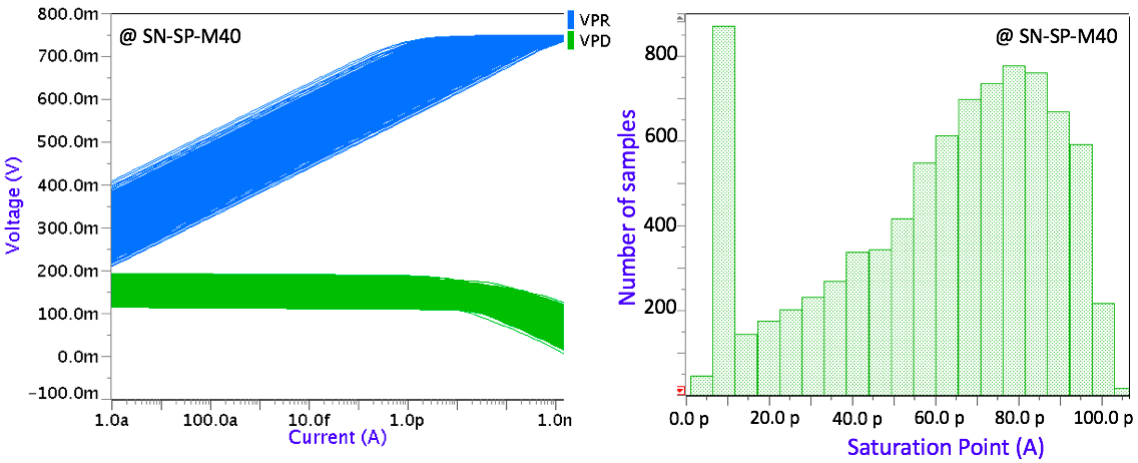


FIGURE 3.20 – Characteristic curves and histogram of the photoreceptor circuit simulated with a Monte-Carlo simulation with 10,000 runs for a Slow NMOS - Slow PMOS process at -40°C.

The histogram in FIGURE 3.20 shows the saturation point at which the characteristic curve V_{pr} begins to saturate. A saturation current between 6 pA and 12 pA is reached for 870 (8.7%) runs. This saturation current corresponds to an illuminance of $1,000$ lx. Hence, 8.7% of the pixels in the array are not able to detect an illuminance above $1,000$ lx if the process is realized in Slow NMOS, Slow PMOS and at -40°C. Moreover, 0.5% of the pixels in the array are not able to detect a photocurrent above 600 fA, corresponding to 50 lx.

Now that the photoreceptor circuit is fully validated in Process-Temperature corners and in Monte-Carlo simulation for the typical and the worst cases, the characteristic curve can be studied to extract the pixel contrast sensitivity.

3.2.8 Contrast sensitivity

The pixel contrast sensitivity can be extracted from FIGURE 3.21. According to the state of the art, a luminous contrast sensitivity of 10% is chosen. Therefore, an event should be generated each time the changes in light increase or decrease by 10%. As intensity change of 10% corresponds to a V_{pr} change of 3 mV, the V_{pr} voltage sensitivity is fixed at 3 mV.

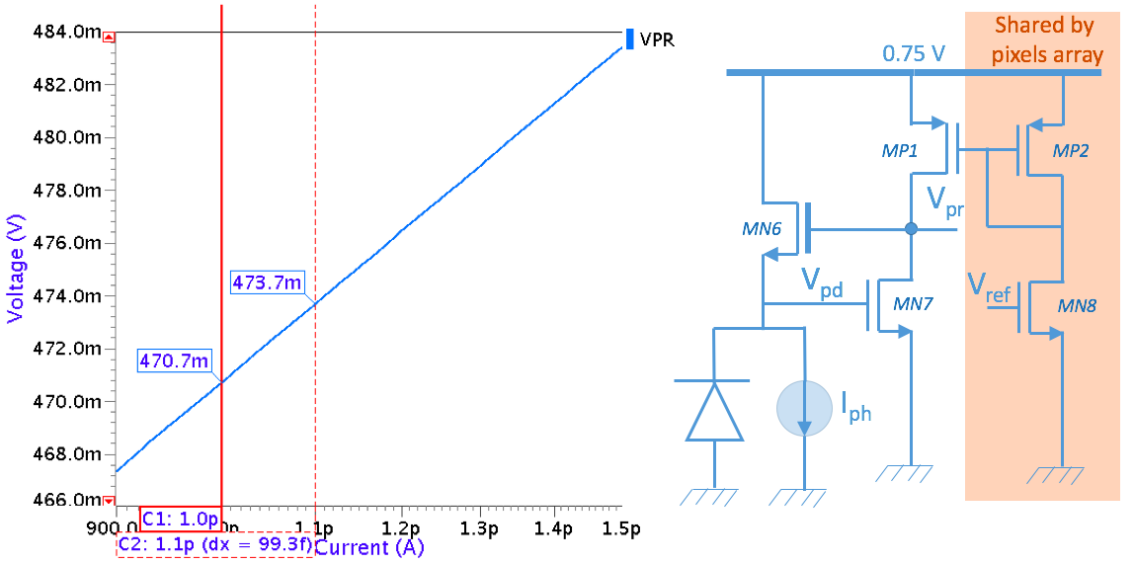


FIGURE 3.21 – Characteristic curve used to determine the sensitivity of the photoreceptor circuit.

3.2.9 Design summary

The final transistor sizing of the photoreceptor circuit is summarized in TABLE 3.4.

TABLE 3.4 – Summary of transistor size in the photoreceptor circuit.

	Width (W)	Length (L)	Transistor type
MN6	300 nm	800 nm	IO
MN7	300 nm	500 nm	Core
MN8	300 nm	500 nm	Core
MP1	500 nm	500 nm	Core
MP2	500 nm	500 nm	Core

3.3 Buffer

According to the DAVIS, the buffer circuit allows to isolate the output voltage of the photoreceptor circuit from the reset of the SCA circuit. However, as mentioned in SECTION 2.1, the buffer is not integrated in this work. The reason is explained in this section. First of all, it is considered that the buffer is part of this study. The problem of its design is then highlighted. Finally, the buffer is removed from the pixel schema and its consequences are outlined.

The schema of the pixel with the integration of the buffer is represented in FIGURE 3.22. The input of the buffer circuit is the voltage V_{pr} and its output is noted V_{buf}.

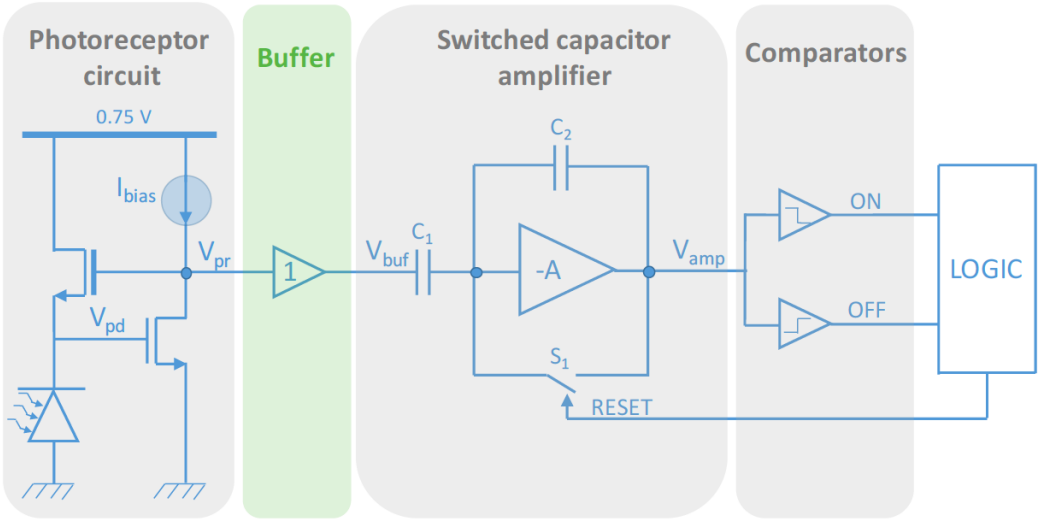


FIGURE 3.22 – Pixel schematic with the buffer highlighted.

A way to realize a buffer is to use a source follower transistor. To avoid the bulk to source effect leading to an error on the slope, the buffer transistor should have its bulk short-circuited at its source. For layout facilities, a PMOS source follower is then more appropriated to construct the buffer. To express the relation between V_{pr} and V_{buf} in such a configuration, the equation of its drain current is considered:

$$I_D \propto \frac{W}{L}(V_{buf} - V_{pr} - V_{th})^2$$

Therefore, for a constant drain current, if V_{pr} increases, V_{buf} increases of the same among. The difference between V_{pr} and V_{buf} is then an offset depending of the drain current, the size of the transistor ant its threshold voltage. As the purpose of the neuromorphic pixel is to capture movement and not the background of the scene, the offset on V_{pr} and V_{buf} voltages is not relevant. The buffer can then be realized with a source follower transistor. To reduce the offset, a low drain current ($I_D = 1pA$), a large width (w=1 µm) and a small length (l=180 nm) are used. The integration of the buffer in the pixel is illustrated and simulated in FIGURE 3.23.

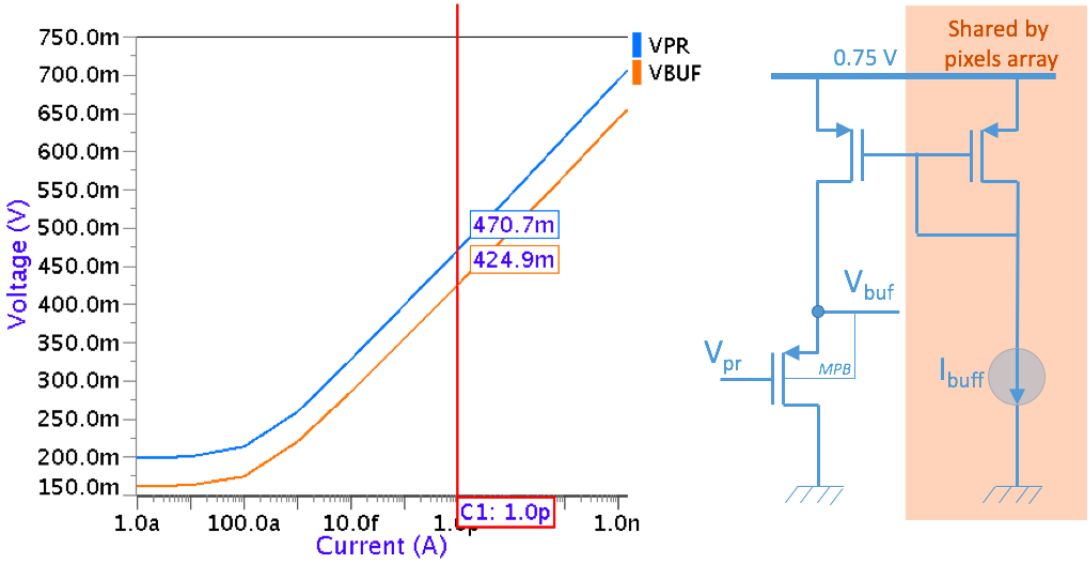


FIGURE 3.23 – Simulation of the buffer architecture.

The offset between V_{pr} and V_{buf} is then of 45.8 mV. In FIGURE 3.24, the same simulation is realized but this time with a Slow NMOS - Slow PMOS process and at -40°C.

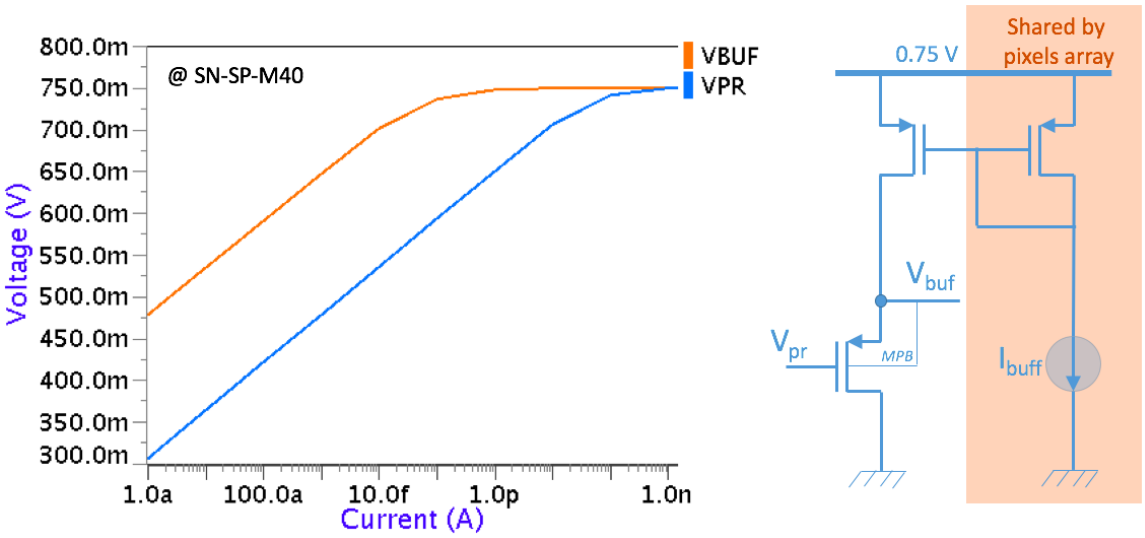


FIGURE 3.24 – Simulation of the buffer architecture in Slow NMOS - Slow PMOS corner at -40°C.

The simulation in the Slow NMOS - Slow PMOS process and at -40°C shows saturation of the buffer output at 100 fA. Hence, it saturates before the voltage V_{pr}. The offset introduced by the buffer increases then the saturation issue at -40°C. Therefore, the buffer is not used in this study. A consequence of this could be a charges injection in the photoreceptor circuit (as mentioned in the DAVIS's paper [5]) during the reset of the SCA. However, at it is demonstrated during the simulation of the whole pixel, this effect is not present in this study. Maybe the DAVIS raises this issue because it uses two different supply voltages, 1.8 V for the photoreceptor circuit and 3.3 V for the rest of the DVS part although this work used only a supply voltage of 0.75 V.

3.4 Switched capacitor amplifier

The switched capacitor amplifier circuit aims to amplify the V_{pr} change between two reset signals. Its schema is recalled in FIGURE 3.25.

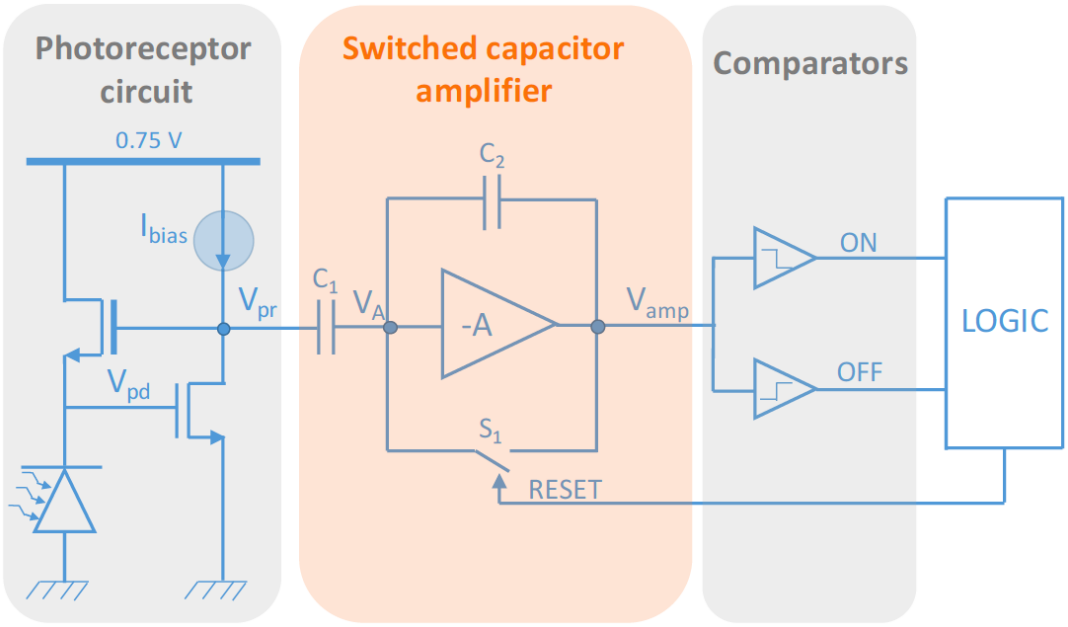


FIGURE 3.25 – Pixel schematic with the switched capacitor amplifier circuit highlighted.

To design this circuit, capacitors are firstly sized. Then, the operational amplifier is designed in order to achieve the different specifications requested by the application. Finally, the switch architecture is discussed.

3.4.1 Sizing of capacitors

As discussed in SECTION 2.4.1, the ratio C_1/C_2, determining the SCA gain of amplification, is fixed at 15. As the pixel area is one of the figures of merit, capacitances should be minimized. In a 0.18 µm CMOS technology, three types of capacitors are proposed: the NCAP, the PCAP and the MIMCAPS. The NCAP capacitor is realized with a NMOS, the PCAP with a PMOS and the MIMCAPS with two metal layers and an insulator. The capacitance per μm^2 of each of them is itemized hereunder:

- **NCAP:** 0.828 fF/µm^2
- **PCAP:** 0.828 fF/µm^2
- **MIMCAPS:** 1.03 fF/µm^2

As capacitor MIMCAPS is the one reaching the highest capacitance per unit of area, it is used in this study. The capacitor C_1 is then constructed with a MIMCAPS of 1.28x1.28 µm^2, corresponding to the minimum size, and its resulting capacitance is 1.69 fF. Therefore, the area taken by capacitors C_1 and C_2 in the layout is (see FIGURE 2.8):

$$(1.28\ \mu m \times 4) \times (1.28\ \mu m \times 4) = 26.2144\ \mu m^2$$

A way to further minimize the capacitors area in the pixel layout is to place the MIM-CAPS above the transistors. However, the capacitors can not overlap the photodiode layout otherwise any light is sensed by the pixel.

3.4.2 Design of the amplifier

The amplifier used in the SCA block is a single-stage OTA [41]. Its architecture is recalled in FIGURE 3.26 with the notations used in this work.

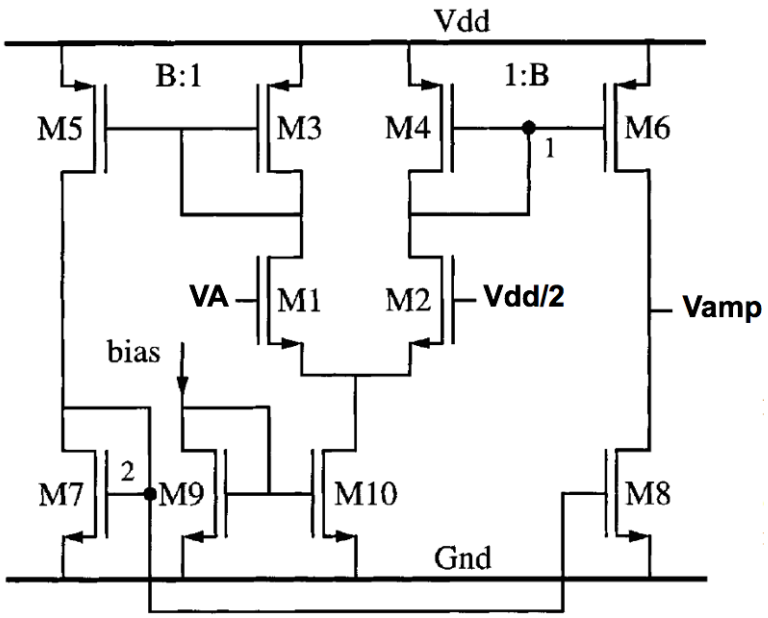


FIGURE 3.26 – CMOS operational amplifier (adapted from [41]).

Its design flow is reported in ANNEXE B as well as its corresponding Matlab code. Only a recall of the design guidelines and the results are given in this section.

Slew rate

During the reset signal, the output voltage V_{amp} is reinitialized at $V_{DD}/2$. The time taking by V_{amp} to reach $V_{DD}/2$ is defined by the slew rate of the amplifier. Hence, if the slew rate increases, V_{amp} reaches faster $V_{DD}/2$. Therefore, the reset signal duration can be decreased and the pixel is more quickly ready to detect the next event. As the slew rate is defined by $SR = 2BI_{bias}/C_2$, a high bias current and/or a high parameter B are necessary to increase it. The capacitor C_2 has already been sized in the previous point.

By trial and error, a slew rate of 10 V/µs is chosen. In this way, the V_{amp} voltage reaches $V_{DD}/2$ at the end of the reset signal in all the corner processes. A parameter B of 1 is chosen and the OTA bias current is set at 10 nA.

DC gain

The amplifier positive input is $V_{DD}/2$ and its negative one is noted V_A. During the reset, V_{amp} is short-circuited at V_A. Therefore, V_A has to be as close as possible to $V_{DD}/2$. A high amplifier DC gain is then requested.

Maximum transistor size

As the pixel area should be minimized, the maximum transistor length and width is fixed at 4 µm. However, to decrease the pixel-to-pixel variations (simulated by a Monte-Carlo simulation), the transistors should be large enough. Therefore, a trade-off exits between the pixel area and the pixel-to-pixel variations.

Phase margin

The phase margin is defined as the difference in phase from 180° at unitary gain. To guarantee the stability of the system, a phase margin around 75° is required. The SCA amplifier is then designed in order to reach a good phase margin.

Hence, the amplifier is designed in order to reach a high slew rate (10 V/µs) and a high DC gain while keeping a good phase margin. Moreover a trade-off is made on the transistor size.

Results

A design of the amplifier succeedes in respecting the different guidelines. It is simulated in FIGURE 3.27 and its sizing is summarized in TABLE 3.5

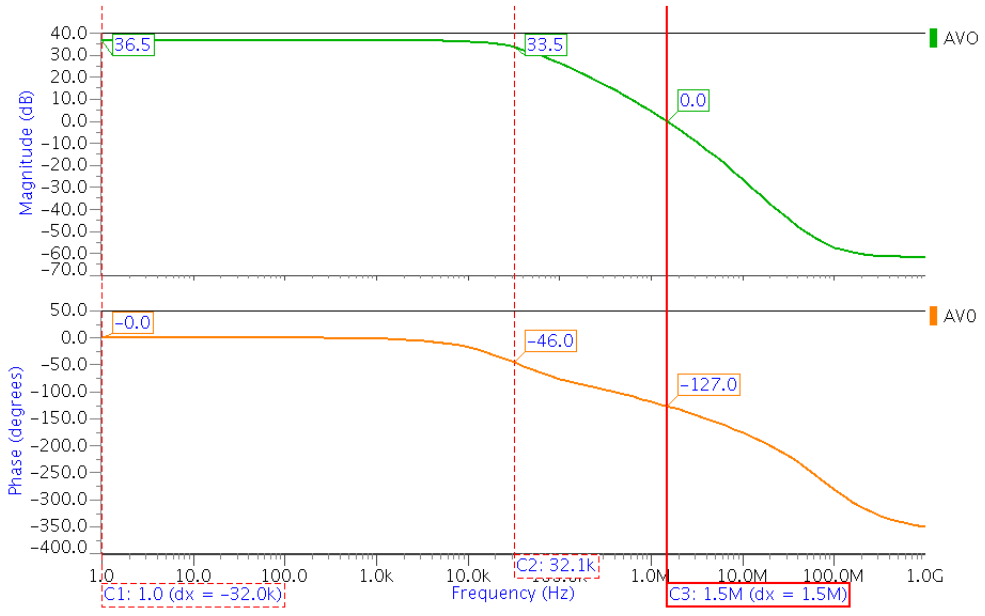


FIGURE 3.27 – Frequency response in open loop of the amplifier used in the switched capacitor amplifier circuit.

TABLE 3.5 – Summary of transistor size used in the amplifier of the SCA circuit.

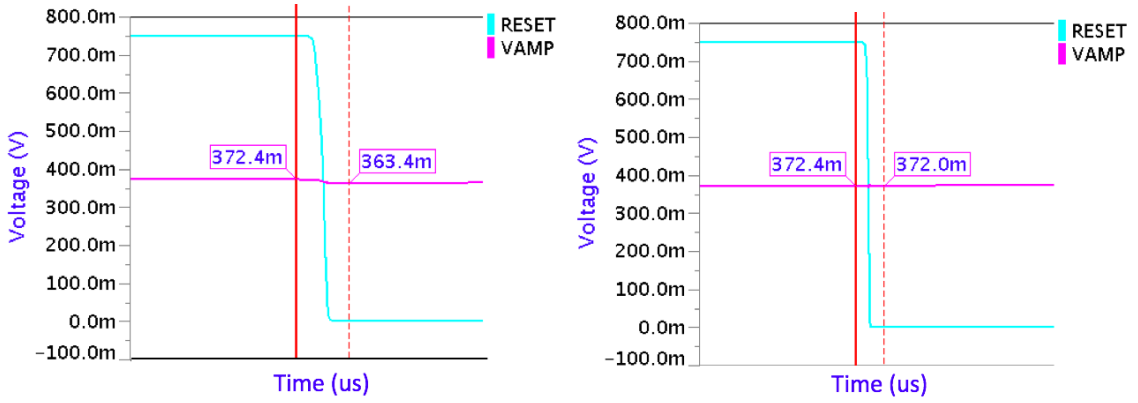
	Width (W)	Length (L)	Transistor type
M1 & M2	500 nm	4 µm	Core
M3 & M4	1 µm	500 nm	Core
M5 & M6	1 µm	500 nm	Core
M7 & M8	3 µm	2 µm	Core
M9 & M10	500 nm	2 µm	Core

This sizing allows to get a DC gain of 36.5 dB, a first pole located at 32.1 kHz and a phase margin of 53°. Moreover, the size used for the transistors are large enough to guarantee a low pixel-to-pixel variation (see SECTION 4.2.3).

3.4.3 Switch design

As explained in SECTION 2.4.3, a good switch design is essential to minimize the charges injection during the reset signal. Therefore, the switch is sized with minimum length and width. Two methods can then be use to further decrease charges injection: the dummy switch and the complementary switch.

The charges injection of a 480x360 nm switch used with a 240x180 nm dummy switch is simulated in FIGURE 3.28a. The simulation shows a V_{amp} decrease of 9 mV after the reset signal. The charges injection of a 240x180 nm switch used with a 240x180 nm complementary switch is simulated in FIGURE 3.28b. The simulation shows a V_{amp} decrease of 0.4 mV after the reset signal.



(a) Dummy switch.

(b) Complementary switch.

FIGURE 3.28 – Simulation of the charges injection during the reset of SCA with a dummy switch at left and a complementary switch at right.

The use of a complementary switch results then in less charges injection than the addition of a dummy switch. This result is intended as a lower switch size is used in the architecture with the complementary switch. A complementary PMOS switch with same switch size is then used in this study to decrease further the charges injection.

3.5 Comparators and Logic

With the logic behind them, the two comparators produce the reset signal used to reset the SCA circuit. Two comparators are necessary to produce ON events or OFF events depending if the light intensity decreases or increases respectively. The two comparators are highlighted in FIGURE 3.29.

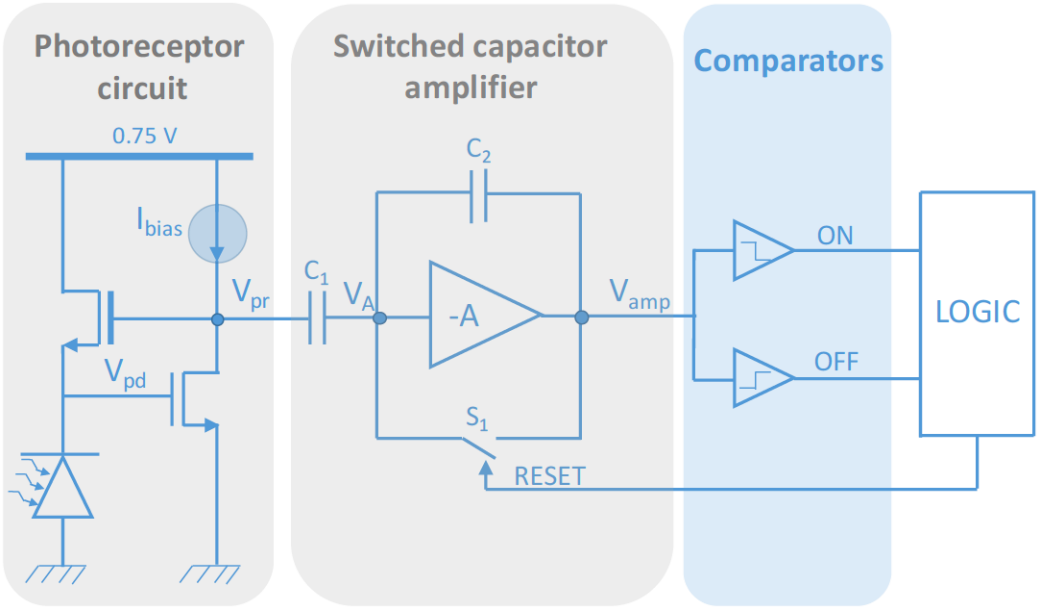


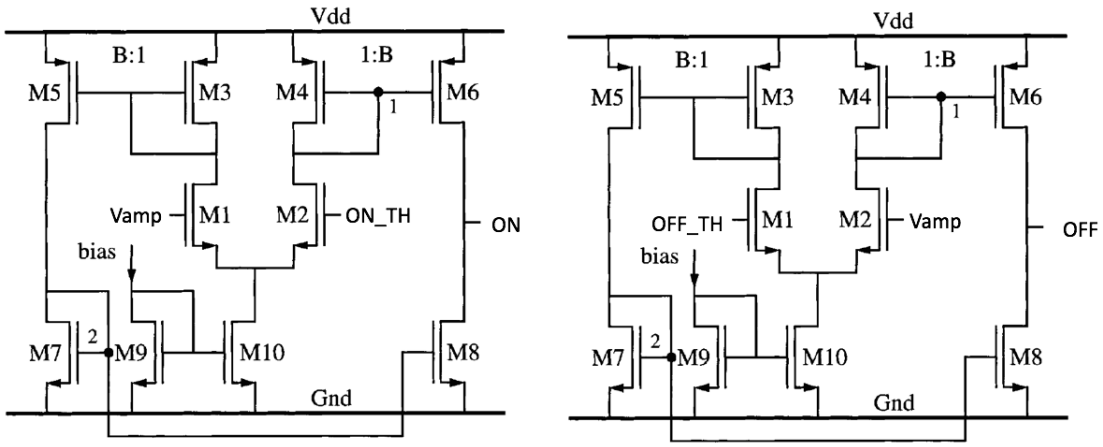
FIGURE 3.29 – Pixel schematic with the comparators highlighted.

To detect a change in light intensity of 10%, corresponding to a V_{pr} change of 3 mV and a V_{amp} change of 45 mV, the two thresholds are fixed at:

ON Threshold: $V_{DD}/2$ - 45 mV

OFF Threshold: $V_{DD}/2$ + 45 mV

The architecture used to implement the comparators is the same one used in the amplifier of the SCA circuit. The DC gain is still maximized while keeping large transistor size to decrease pixel-to-pixel variations during the Monte-Carlo simulation. Moreover, the amplifier is designed in order to reach a good phase margin. However, the slew rate reached in the amplifier of the SCA circuit can be reduced. Hence, the comparators bias current is fixed at 1 nA, decreasing then the power consumption. The architectures of the two amplifiers used to implement the ON and OFF comparators are shown in FIGURE 3.30a and FIGURE 3.30b respectively.



(a) Comparator used to produce ON events. (b) Comparator used to produce OFF events.

FIGURE 3.30 – Architecture of the two comparators (adapted from [41]).

The same OTA sizing that SCA amplifier is used in the two comparators. The frequency response of these comparators with a load capacitor of 2 fF is simulated in FIGURE 3.31. The first pole is located at 4.5 kHz, the DC gain is 35.3 dB and the phase margin is 51.5°.

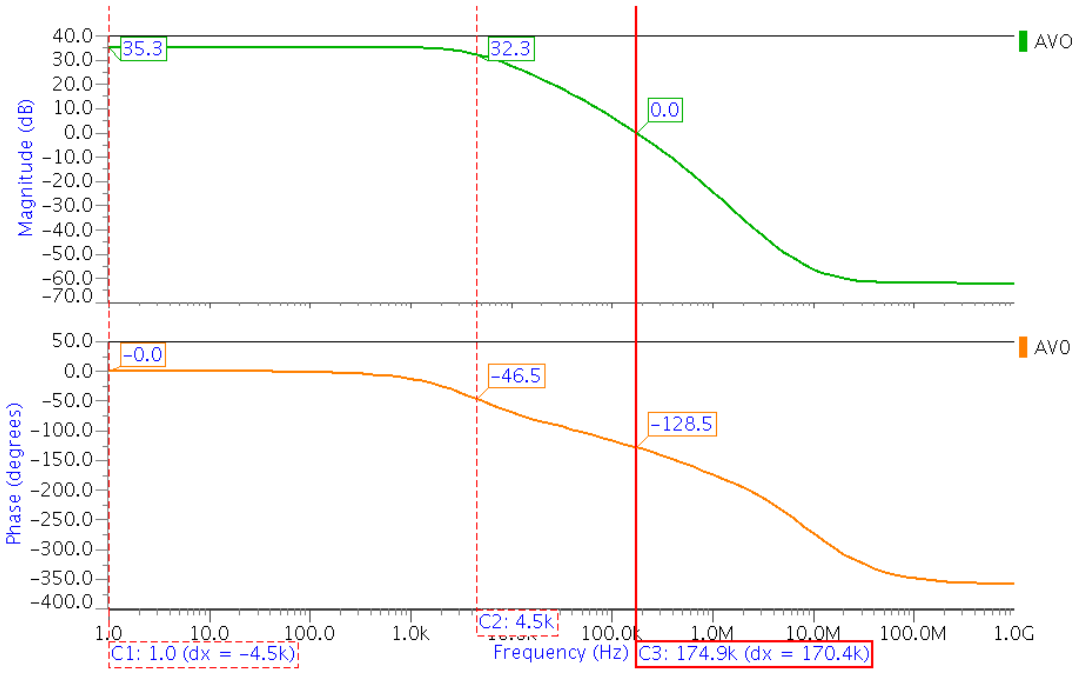
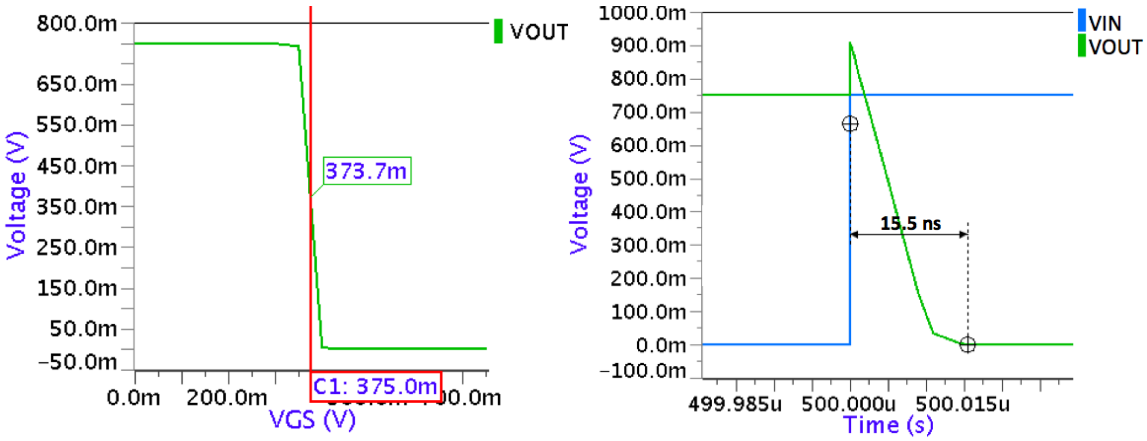


FIGURE 3.31 – Frequency response of the amplifier used in the two comparators with a load capacitor of 2 fF.

3.5.1 Logic chain

As discussed in SECTION 2.6, the logic circuit is the one that fixed the duration of the reset signal. A too long reset signal slows down the pixel. However, the reset signal should be long enough to allow voltage V_{amp} to reach $V_{DD}/2$. Hence, the four inverters used to produce digital ON and OFF signals are composed of a NMOS IO transistor of 680 nmx680 nm and a PMOS IO transistor of 340 nmx340 nm (determined by trial and error). Actually, the NMOS size is twice the PMOS size to get the switching threshold located at $V_{DD}/2$. Moreover, increasing the PMOS and NMOS sizes allows to get a longer response time. The characteristic curve and the response time of such an inverter are represented in FIGURE 3.32a and 3.32b respectively. According to these figures, the switching threshold is well located at $V_{DD}/2$ and the response time of the inverter to a step input voltage is 15.5 ns.



(a) Characterisitic curve.

(b) Time respond for a step input voltage.

FIGURE 3.32 – Characterisitc curve and time response of an inverter realized with a 680 nmx680 nm NMOS IO transistor and a 340 nmx340 nm PMOS IO.

In order to decrease the pixel area, the last two logic gates are designed with minimal PMOS and NMOS core transistor sizes.

Chapter 4

Validation and Characterization

Contents

The pixel design is fully validated and characterized in this chapter. During the validation, the pixel is simulated with a photocurrent and the comparison between the results and the theoretical equations is provided. This comparison allows to point out that a modification in the threshold values is needed to reach better pixel performances. When the pixel is validated, it is characterized in order to compare it with the architecture presented in the literature.

4.1 Validation

This section aims to validate the pixel design. More precisely, the different circuits designed in SECTION 3 are put together and the pixel is simulated with a photocurrent I_{ph}. The change in V_{pr} between two reset signals is measured for all variations in Process-Temperature corners in order to guarantee the detection of a change in light intensity of 10%.

The photoreceptor circuit should detect a change in light intensity of 10% which corresponds to a change in V_{pr} of 3 mV. Hence, in theory, if the light intensity decreases of 10%, the value of V_{amp} reaches:

$$V_{DD}/2 + 15 \times 3 \text{ mV} = 420 \text{ mV}$$

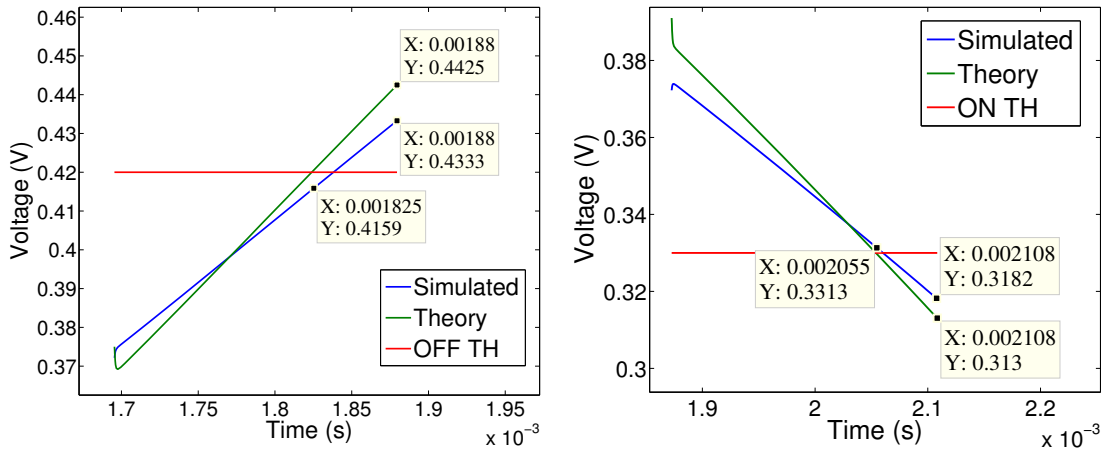
If the light intensity increases of 10%, the value of V_{amp} decreases to:

$$V_{DD}/2 - 15 \times 3 \text{ mV} = 330 \text{ mV}$$

The pixel response to a change in light intensity of 10% at 5 keps (kilo event per second) is represented in FIGURE 4.1a (for an increase of 10%) and 4.1a (for a decrease of 10%). Theses figures show the simulated and the theoretical curves of V_{amp} between two reset signals. The theoretical curve is obtained with:

$$V_{amp} = \frac{V_{DD}}{2} + 15 \times (V_{reset} - V_{pr})$$

with V_{reset} the V_{pr} value at the previous reset signal. The two figures are analyzed hereunder.



(a) OFF event.

(b) ON event.

FIGURE 4.1 – Graph of the simulated and theoretical curves of Vamp between two reset signals.

OFF event: When the photocurrent decreases, the voltage V_{pr} decreases and the corresponding V_{amp} voltage increases. However, the simulated and the theoretical curves do not increase with the same slope. With an OFF threshold fixed at 420 mV, the event is raised when the simulated V_{amp} reaches 433.3 mV. The comparator error is then of 13.3 mV. Moreover, when the event is raised, this corresponds to a theoretical V_{amp} of 442.5 mV. The corresponding change in V_{pr} is then:

$$(442.5 \text{ mV} - 375 \text{ mV})/15 = 4.5 \text{ mV}$$

Therefore, the event is produced for a change in light intensity of 15%. However, the expected change intensity is 10%. Hence, the event should be raised when the theoretical V_{amp} crosses 420 mV corresponding to a simulated V_{amp} of 415.9 mV. If an error of 13.3 mV is considered for the comparator, to produce an error each time the light intensity decreases of 10%, the new threshold is 402.6 mV $\simeq$ 405 mV.

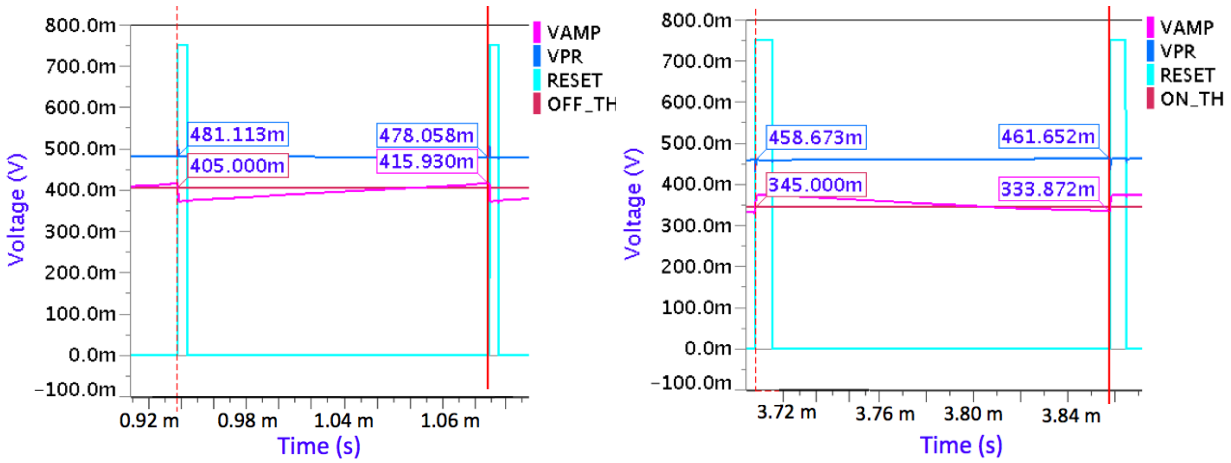
ON event: In the same way as for an OFF event, when the photocurrent increases, the voltage V_{pr} increases and the corresponding V_{amp} voltage decreases. However, the simulated and the theoretical curves do not decrease with the same slope. With an ON threshold fixed at 330 mV, the event is raised when the simulated V_{amp} reaches 318.2 mV. The comparator error is then 11.8 mV. Moreover, when the event is produced, this corresponds to a theoretical V_{amp} of 313 mV. The corresponding change in V_{pr} is then:

$$(375 \text{ mV} - 313 \text{ mV})/15 = 4.13 \text{ mV}$$

Therefore, the event is produced for a change in light intensity of 13.77%. However, the expected change intensity is 10%. Hence, the event should be raised when the theoretical V_{amp} crosses 330 mV corresponding to a simulated V_{amp} of 331.3 mV. If an error of 11.8 mV is considered for the comparator, to produce an error each time the light intensity increases of 10%, the new threshold is 343.1 mV $\simeq$ 345 mV.

Hence, a threshold of 405 mV is used to produce an OFF event and a threshold of 345 mV is used to produce an ON event. These thresholds should allow to raise events when a change in light intensity of 10% is detected. However, as the precision on the light intensity detected is not really important, an error of 2% can still be accepted for the comparators. The change of 8% and 12% of light intensity corresponds respectively to a change in V_{pr} of 2.4 mV and 3.6 mV.

The simulation of the pixel for an OFF and ON event generation with threshold voltages of 405 mV and 350 mV are illustrated respectively in FIGURE 4.2a and 4.2b. The first one shows that an OFF event is produced when voltage V_{amp} reaches 415.93 mV. The corresponding change in V_{pr} voltage is 3.06 mV. Hence, the event is detected for a light change of 10.2%. The second one shows that an ON event is produced when voltage V_{amp} reaches 333.87 mV. The corresponding change in V_{pr} voltage is 2.98 mV. Hence, the event is detected for a light change of 9.93%.



(a) OFF event. (b) ON event.

FIGURE 4.2 – Simulation of the change in V_{pr} between two events.

The same simulation is realized in the different Process-Temperature corners. The corresponding change in V_{pr} for an OFF and ON event are summarized in TABLE 4.1.

TABLE 4.1 – Change in V_{pr} between two events.

	OFF EVENT	ON EVENT
TYP	3.06 mV	2.98 mV
SSM40	3.25 mV	2.71 mV
FSM40	2.79 mV	3.33 mV
SFM40	3.31 mV	2.90 mV
FF50	3.19 mV	3.06 mV
FS50	2.88 mV	3.16 mV
SF50	3.24 mV	2.73 mV

According to TABLE 4.1, an event is generated for a change in V_{pr} between 2.71 mV and 3.31 mV. Hence, in each Process-Temperature corners, events are produced each time a change in light intensity of 10% is sensed, with an acceptable error of 2%. The behavior of the neuromorphic pixel is then validated in each Process-Temperature corners.

4.2 Characterization

The pixel is now characterized in order to compare its performances with the ones reached in the literature. Hence, the pixel dynamic range, the power consumption, the minimum latency, the FPN, the pixel complexity, the pixel area and the pixel scalability are determined.

4.2.1 Dynamic range

In typical conditions, the sensor detects a photocurrent between 110 aA and 1.1 nA (see FIGURE 3.15) corresponding to an illuminance of 0.01 lx and 100,000 lx respectively. Hence, the pixel DR in typical condition is 140 dB. In SSM40 and SFM40 corners, the pixel detects a maximum illuminance of 10,000 lx. The corresponding DR is then 120 dB. Finally, at 50°C, the minimum illuminance detectable by the DVS is 0.1 lx. Hence, the corresponding DR is also 120 dB.

4.2.2 Minimum latency

When the sensor is biased for speed, a minimum latency of 3 µs is reported in the DAVIS pixel [5]. This latency is determined by the time taking by the first event to occur when the pixel is excited with a step photocurrent change of 30% at 1 klx. Hence, a step of photocurrent from 11 pA (corresponding to 1 klx) to 14.3 pA is applied on the pixel of this study. The simulation is realized in FIGURE 4.3.

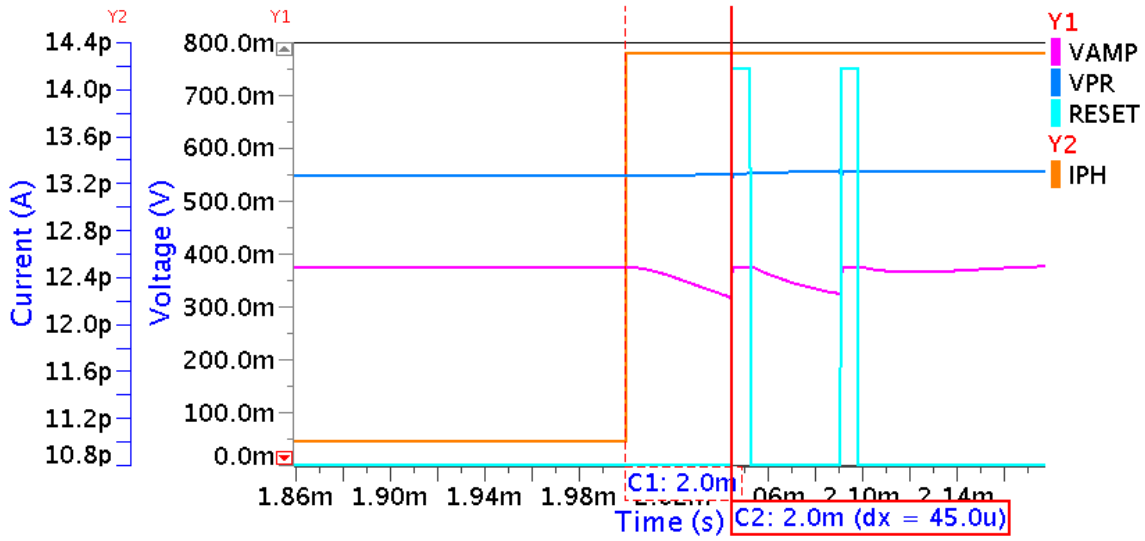


FIGURE 4.3 – Response time of the pixel excited with a current step at 1 klx.

Therefore, the minimum latency is 45 µs. This value is larger than what is reached in the literature. However, the pixel is here supplied with only 0.75 V and it is not biased in order to reach low latency. In CHAPTER 5, the bias of the pixel is discussed in order to reach a lower latency.

4.2.3 Fixed pattern noise

In this context, the fixed pattern noise (FPN) represents the uniformity of response, or the pixel-to-pixel variation. The FPN is calculated as the standard deviation of change in V_{pr} between two reset signals expressed in [%] of illumination change [7]. To determine the FPN of this study, a MC simulation with 10,000 runs is realized in FIGURE 4.4 for an OFF event and in FIGURE 4.5 for an ON event. The two histograms show the V_{pr} variation needed to produce an OFF or ON event respectively. They are described hereunder.

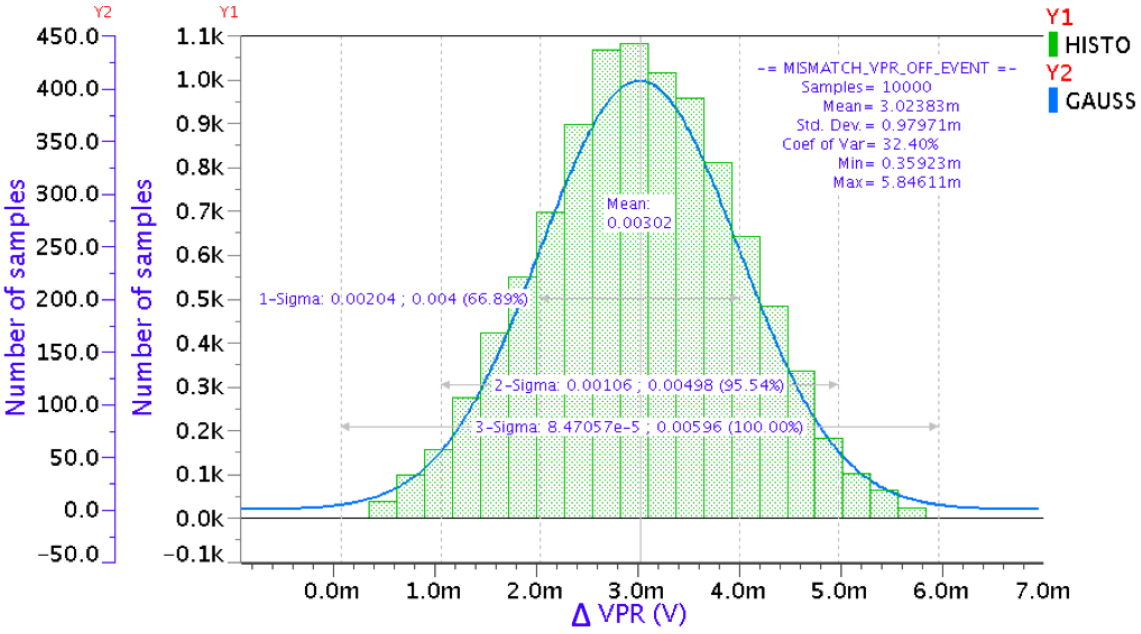


FIGURE 4.4 – Histogram of the change in V_{pr} between two OFF events.

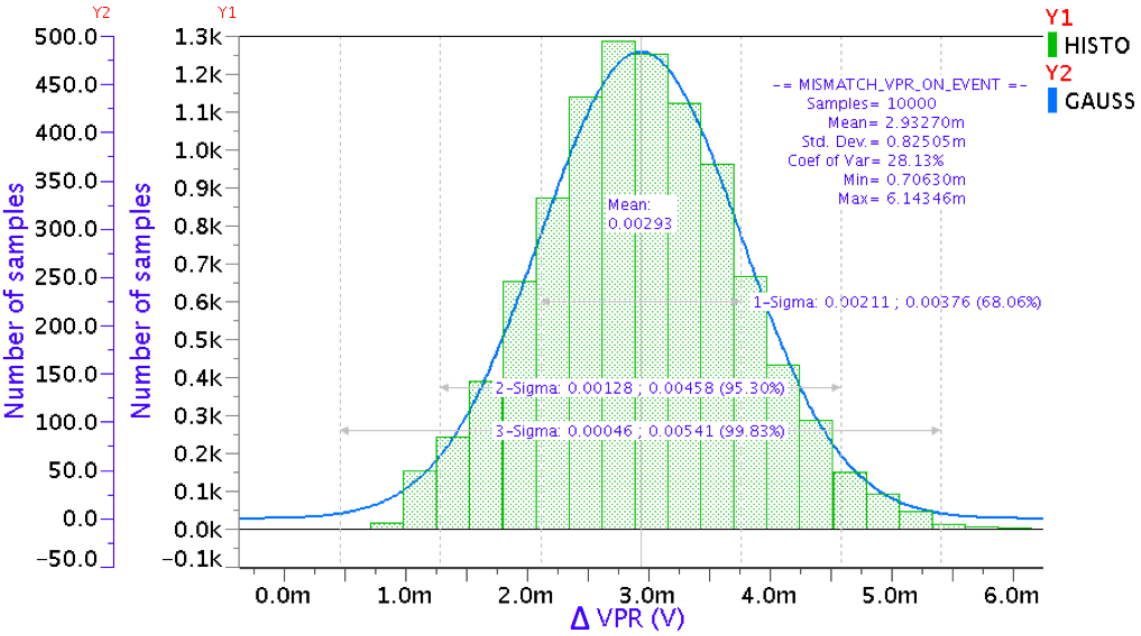


FIGURE 4.5 – Histogram of the change in V_{pr} between two ON events.

OFF event The mean of change in V_{pr} between two OFF events is 3.02 mV. On average, an OFF event is then produced each time a decrease in light intensity of 10% is detected by the pixel. A minimum change in V_{pr} value of 0.36 mV is reached, corresponding to a change in light intensity of 1.2%. Hence, $\sim 2\%$ (~ 200 runs) of pixels in the array produce an OFF event when a contrast decrease of 1.2% is sensed. On the contrary, $\sim 1\%$ (~ 100 runs) produced the event when the contrast decrease of 19.5%. Finally, the standard deviation of the change in V_{pr} is 0.98 mV. Hence, the standard deviation, expressed in [%] of illumination change, corresponds to 3.27%.

ON event In the same way, an ON event is produced each time an increase in light intensity of 10% is sensed by the pixel. A minimum change in V_{pr} value of 0.71 mV is reached, corresponding to a change in light intensity of 2.37%. Hence, $\sim 0.5\%$ (~ 50 runs) of pixels in the array produce an ON event when a contrast increase of 2.37% is sensed. On the contrary, $\sim 0.1\%$ (~ 10 runs) produced the event when the contrast increase of 20.47%. Finally, the standard deviation of the change in V_{pr} is 0.83 mV. Hence, the standard deviation, expressed in [%] of illumination change, corresponds to 2.77%.

4.2.4 Power consumption

The power consumed by the pixel is an important feature. The literature reports a power consumption of 0.16 µm per pixel at high activity. The DC power is calculated for this work as well as the energy needed to produce an event. Moreover, a power consumption at high and low activity is measured. As their definition is not standardized in the literature, an output pixel event rates of 60 keps and 250 keps are respectively considered for a low and a high activity. These values correspond respectively to the average DVS event rate and the peak rates sensed by the DAVIS when a tennis player hitting a backhand stroke is recorded [5].

DC power: The DC power of the pixel is calculated as $P = V_{DD} \times I_{total}$. Hence, with a supply voltage of 0.75 V, a DC power of 20.54 nW is reached. According to the ATIS, the DC power corresponds to its power consumption at low activity. Hence, DC power achieved in this study is far below the one reached in the ATIS pixel.

Energy per event: Although the literature does not give any information about the pixel energy necessary to produce an event, it is calculated in this study. The energy per event is preferred than the power per event as it does not depend on the event rate. The energy per event is measured by integrating the power consumption from the end of a reset signal until the end of another reset signal and by dividing it by the number of spikes produced during this interval. The energy per event obtained is 712.4 fJ/event. Although this energy cannot be compared with other related works, it can be compared with the energy per frame obtained in the CAMEL which is 17 pJ/frame [1]. Hence, the energy per event obtained in this study can be considered as a pretty good performance as it results of a factor of 20 compared to the CAMEL energy.

High activity: A DVS event rate of 250 keps consumes a power of 178 nW.

Low activity: A DVS event rate of 60 keps consumes a power of 42.74 nW.

As the bias voltage generator and the AER protocol are not implemented in this work, the total sensor power consumption is only calculated as a lower bound.

4.2.5 Pixel Complexity

To figure out the pixel complexity, the number of transistors used in each circuit is calculated.

Photoreceptor circuit: The photoreceptor circuit is composed of 1 photodiode and 5 transistors. However, 2 transistors are shared by all pixels in the array. Hence, the photoreceptor circuit of one pixel is composed of 3 transistors.

Switched capacitor amplifier circuit: The switched capacitor amplifier circuit is composed of 2 MIM capacitors, 1 switch (1 transistor), 1 complementary switch (1 transistor) and 1 amplifier (10 transistors with one shared by all the pixels in the array). To construct the switched capacitor amplifier circuit, 11 transistors are therefore necessary.

Comparators circuit: Each comparator circuit is composed of 11 transistors. However, one of them is shared by all pixels in the array. Hence, to construct the two comparators, 20 transistors are needed.

Logic circuit: The logic circuit is composed of 5 inverters (2 transistors for each of them) and 1 OR gate (6 transistors). The logic circuit is then composed of 16 transistors.

Therefore, the pixel complexity is **50 transistors**. This work needs then 3 transistors more than DAVIS pixel.

4.2.6 Pixel area

As the layout is not realized in this Master Thesis, the exact pixel area cannot be determined. However, its minimum value can still be measured. To achieve this purpose, the size of each transistor in each circuit is measured. The size of each transistor is calculated as: $W \times (L + 2 \times L_{diff})$, with L_{diff} the diffusion length.

Photoreceptor circuit: the photodiode area is 25 μm^2, the photoreceptor transistor area is 0.288 μm^2, the bias transistor area is 0.416 μm^2 and the transistor used in the mirror current has an area of 0.296 μm^2. Hence, the total photoreceptor circuit area is 26 μm^2.

Switched capacitor amplifier: In the same way as for the photoreceptor circuit, the SCA circuit area is 19 μm^2. The capacitors area is not taking into account in this measure as their layout can be overlap to the transistor layout.

Comparators: Together, the two comparators take an area of 38 μm^2 in the layout.

Logic: The logic takes 5 μm^2 of area in the layout.

Hence, the minimum pixel area is 88 μm^2 corresponding to a pixel pitch of 10 μm^2 x 10 μm^2.

4.2.7 Fill factor

For a pixel size of 10 μm^2 x 10 μm^2, the fill factor is 25%. However, the pixel area will be larger than this minimum value. Hence, the fill factor of 25% is an upper bound. To increase it, it is possible to increase the photodiode area to fill all the free space in the layout. Hence, the fill factor will be maximized. However, if the photodiode area increases, it also increases its dark current, decreasing therefore sensitivity at low light intensities.

4.2.8 Pixel scalability

The pixel is simulated with different values of supply voltage to verify its scalability. With an appropriate tuning of the threshold voltage values, the pixel still produces ON and OFF events at a supply voltage of 1.8 V, 0.7 V and 0.6 V.

4.2.9 Summary

Our pixel performances are compared with state-of-the-art architectures in Table 4.2. To provide a VGA resolution, an array size of 480x320 is reported for our study. The comparison shows that our design presents better performances than the ones described in the literature, excepted for the minimum latency performance. Actually, this work consumes less power and has the largest DR. Moreover, the FPN is better than the one reached in the DAVIS. Finally, although the correct pixel area cannot be determined without the layout, the minimum pixel area calculated is promising.

TABLE 4.2 – Comparison between our pixel and the state-of-the-art architectures.

	This work	Samsung [32]	DAVIS [5]	ATIS [6]	Barranco 2013 [27]	Barranco 2011 [30]	Lichsteiner [7]	Mallik [26]	Zaghloul [24]
Functionality	**DVS**	DVS	DVS + APS	DVS + Exposure measurements	DVS	DVS	Asynchronous temporal contrast	APS imager + temporal change detection	Asyn. spatial and temporal contrast
CMOS Technology	**0.18 µm CIS MIM**	90 nm CIS 1P5M BSI	0.18 µm CIS 1P6M MIM	0.18 µm CIS 1P6M MIM	0.35 µm CIS 2P4M	0.35 µm CIS 2P4M	0.35 µm CIS 2P4M	0.5 µm CIS 2P3M	0.35 µm CIS 2P4M
Chip size mm^2	**N.A.**	8 x 5.8	5 x 5	9.9 x 8.2	4.9 x 4.9	5.5 x 5.6	6 x 6.3	3 x 3	3.5 x 3.5
Array size	**480 x 320**	640 x 480	240 x 180	304 x 240	128 x 128	128 x 128	128 x 128	90 x 90	96 x 60
Pixel size um^2	**Min. 10 x 10**	9 x 9	18.5 x 18.5	30 x 30	30 x 31	35 x 35	40 x 40	25 x 25	34 x 40
Fill factor	**Max. 25%**	N.A.	22%	30%	10.5%	8.7%	8.1%	17%	14%
Pixel complexity	**50 T.** **1 photodiode**	N.A.	47 T. 1 photodiode	77 T. 2 photodiodes	N.A.	N.A.	26T.	6T.	38T.
Supply voltage	**0.75V**	2.8V analog 1.2V digital	1.8V/3.3V	3.3V analog 1.8V digital	3.3V	3.3V	3.3V	5V	3.3V
Power high activity low activity no activity	 **> 27.34 mW** **> 6.56 mW** **> 3.15 mW**	 50 mW 27 mW N.A.	 14 mW 5 mW N.A.	 175 mW 50 mW 50 mW	 4 mW	 132 mW 231 mW N.A.	 24 mW	 30 mW	 62.5 mW
Power/pixel high activity low activity no activity	 **0.18 μW** **0.043 μW** **0.021 μW**	 0.16 μW 0.088 μW	 0.32 μW 0.12 μW	 2.4 μW 0.69 μW	 0.24 μW	 8.06 μW 14.1 μW	 1.46 μW	 3.7 μW	 10.85 μW
Energy/pixel	**712.4 fJ**	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.
DR	**140dB**	N.A.	130dB DVS 51dB APS	125dB	120dB	100dB	120 dB	51dB	50dB
Min. contrast sensitivity	**10%**	9%	11%	30% @ 1klux	1.5%	10%	15%	2.1%	N.A.
FPN	**3.27% DVS**	N.A.	0.5% APS 3.5% DVS	<0.25% intensity	0.9% DVS	0.4%	2.1%	0.5%	1-2 decades
Min. latency	**45 μs** **@ 1klux**	N.A.	3 μs @ 1klux	< 4 μs @ 1klux	3.2 μs @ 2klux	3.6 μs @ 25klux	15 μs @ 1klux	N.A.	10Meps

Chapter 5

Discussion and Perspectives

Contents

The purpose of this last chapter is to provide guidelines for the performances improvement. Their corresponding trade-offs are given. Moreover, it discusses some design choices. Finally, perspectives for future works are proposed.

5.1 Discussion

The pixel design reaches good performances. However, some of them can still be improved. Therefore, this section aims to give some guidelines for enhancing some pixel performances. The drawbacks of these modifications are also highlighted. The minimum latency, the fill factor as well as the threshold levels performances are discussed in this section.

5.1.1 Minimum Latency

The minimum latency reaches by this work is 45 µs. However, the literature reveals, for the DAVIS pixel, a minimum latency of 3 µs. It is then interesting to provide guidelines to reach lower minimum latency.

Photoreceptor circuit: With a step photocurrent input which has an infinite slope, the photoreceptor circuit does not respond instantaneously to the variation. Hence, the voltage V_{pr} takes time before reaching its final value. A way to decrease the response time of this voltage is to increase the current in the bias transistor in order to improve the slew rate. The higher slew rate is reached for a bias transistor width and length of 240 nm and 180 nm respectively. This modification allows to reach a minimum latency of 18.7 μs. Moreover, decreasing the bias transistor size, also decreases the pixel area. However, a small transistor size is more sensitive to the MC simulation. Hence, the bias point of 150 mV cannot be exact in each run of the MC simulation.

Supply voltage: To further increase the current through the bias transistor, the supply voltage is increased to 1.8 V. Hence, the drain-to-source voltage of the voltage reference transistor (with the gate biased at 150 mV) increases leading to a higher drain current. This current is copied in the bias transistor through the current mirror. With a supply voltage of 1.8 V, a minimum latency of 14.9 μs is reached. However, the price to pay for this improvement is a higher DC power consumption (86 nW). Moreover, this corresponds no more to the supply voltage used in CAMEL where this work should be integrated.

Comparators: A last way to decrease further the minimum latency is to increase the slew rate of comparators. Actually, there were designed with a bias current of 1 nA. If this biasing current is increased by a factor of 10, the slew rate is increased by the same factor. Hence using a comparator bias current of 10 nA allows to reach a minimum latency of 6.2 µs (with the supply voltage still fixed at 1.8 V). However, the static power consumption is also increased and reaches 191 nW.

Hence, a minimum latency of 6.2 µs can be reached with a pixel biasing at the expense of an increase in power consumption.

5.1.2 Fill Factor

As discussed briefly in SECTION 4.2.7, the fill factor can be increased by filling the free space of the layout by the photodiode. Actually, the pixel length and width are always equal in order to get a patch of pixel. Hence, the pixel area is rounded to the closest square area. The free space of the layout can then be used by the photodiode. However, the drawback of this improvement is that it also increases the photodiode dark current. Hence, the sensitivity at low photocurrent is further decreased.

5.1.3 Thresholds

The last point discussed in this section is about the thresholds. Two thresholds of 405 mV and 345 mV, fixed in SECTION 4.1, are used to produce OFF events and ON events respectively. However, these threshold values are defined for offset compensation. Actually, if a light change of 10% should be detected with a SCA gain of gain 15, thresholds of 420 mV and 330 mV should be used. However, due to the error made on the V_{amp} slope and on the threshold levels, they are set to a lower value.

A way to use thresholds of 420 mV and 330 mV by still keeping a light change sensitivity of 10% is to increase the amplifier and comparators DC gain. A way to increase the DC gain of the differential amplifier is to use the design of TABLE 5.1.

TABLE 5.1 – Example of transistors size used to increase the DC gain of the amplifiers.

	Width (W)	Length (L)
M1 & M2	4.1 nm	1 µm
M3 & M4	240 nm	1 µm
M5 & M6	240 nm	1 µm
M7 & M8	2 µm	4 µm
M9 & M10	500 nm	2 µm

Actually, by increasing the width and decreasing the length of W1 and W2, the parameter $(gm/ID)_1$ increases. Moreover, the DC gain is also determined by the parameter V_{ea}.

$$V_{ea} = \frac{V_{ea6}V_{ea8}}{V_{ea6} + V_{ea8}}$$

This parameter increases then when g_{d8} and g_{d6} decrease. Hence, by decreasing the width of M6 and M8 and increasing their length, a higher gain should be obtained. The size of M3 and M4 is fixed to keep the parameter B to unity. Finally, the slew rate of the different amplifiers is increased by a factor of 5. However, the issue with this design is that small sizes of transistors can lead to pixel-to-pixel variations.

The simulation of such an amplifier with a biasing current of 5 nA and a load capacitance of 2 fF is given in FIGURE 5.1.

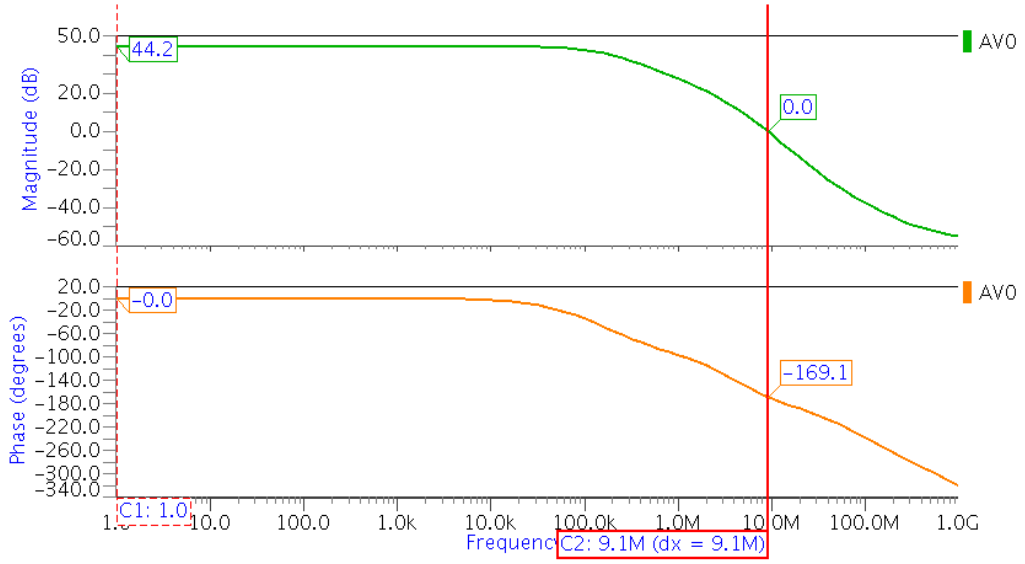
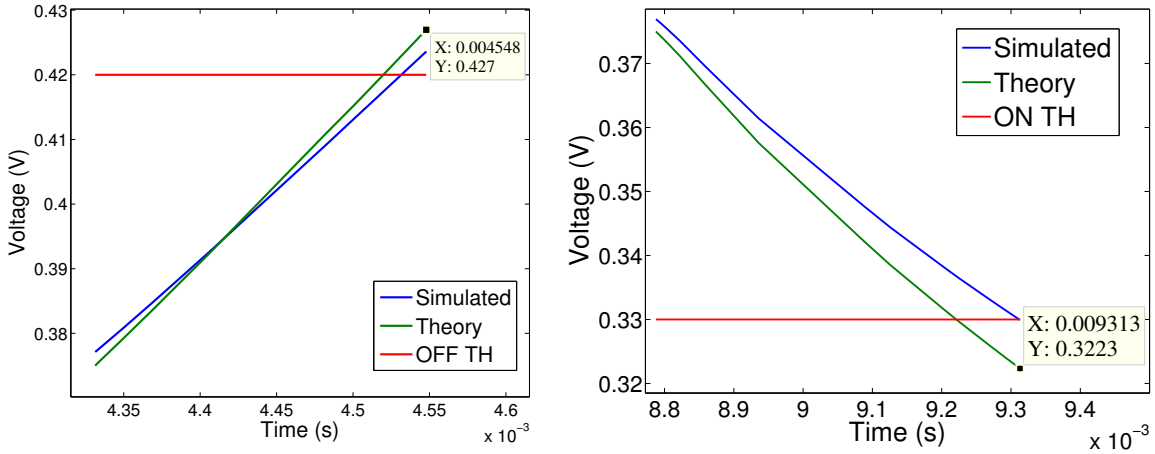


FIGURE 5.1 – Frequency response in open loop of the modified amplifier.

The DC gain obtained is 40.3 dB compared to 35.3 dB before. However, the new phase margin is 30.3° (the previous phase margin was 51.5°). This phase margin can be improved at the price of much higher transistor sizes and therefore a larger pixel area. If this architecture is used in the comparators and on the amplifier of the SCA circuit (with a biasing current of 50 nA), the comparison of the theoretical V_{amp} and the simulated one can be generated in FIGURE 5.2a and 5.2b. These figures show a V_{amp} error of 7 mV for OFF events and an error of 7.7 mV for ON events. Hence, the error in the change in light intensity is 1.5%. With these amplifier designs, there is no need of threshold levels correction.



(a) OFF event.

(b) ON event.

FIGURE 5.2 – Graph of the simulated and theoretical curves of Vamp between two reset signals with modified amplifiers.

Hence, a trade-off should be made between the DC gain, the phase margin, the pixel area and the pixel-to-pixel variation. As the error on threshold levels can be easily corrected by fixing them at a lower value, a decrease of the DC gain is chosen in this work.

5.2 Perspectives

Some perspectives for future work are given in this last section.

Comparators: For design facilities, the pixel comparators architecture is the same one as the SCA amplifier. However, another one could provide better performances at a lower cost. Actually, in the DAVIS, the comparators are implemented with an easier design [5]. Hence, it could be interesting to investigate this new comparator architecture to decrease the pixel power consumption and its complexity.

Threshold levels: In some applications as high-speed texture based recognition, a low contrast sensitivity could be required. Moreover, to use the pixel in different supply voltages, the threshold levels must be adapted. Hence, the integration of a tuning circuit to control the threshold levels has a significant impact on the pixel scalability.

AER: In order to integrate our sensor to a neuromorphic chip, an AER protocol should be implemented. The study of such an architecture and its design is then a great improvement for this work.

Layout: To fully validate our sensor performances, the pixel layout should be drawn. Hence, the exact pixel area could be determined and the simulations post-layout could be realized.

CAMEL: Another perspective is to merge this study with the CAMEL chip. Actually, integrating our DVS with the APS developed in the CAMEL in the same way that in the DAVIS (1 photodiode for the two circuits) would result in a complete image sensor providing both a detection of changes in light intensity and an absolute light information.

Prototype: A last perspective is to realize the prototype of this neuromorphic CMOS imager. The chip could therefore be characterized experimentally and the real photodiode dark current could be measured.

Conclusion

Inspired from human retinae, the development of neuromorphic CMOS imagers over the last few years opens the doors for low data processing and low power consumption sensors. Unlike basic image sensors, neuromorphic imagers designed for sparse vision data acquisition provide asynchronous pixels responding only to relative changes in light intensity. The electrical modeling of the neuron architectures involved in the vision process makes them not only promising for robotics, but also for real-time tracking. Therefore, two main questions are raised:

- How can the human eye be electrically emulated for event-driven sparse data acquisition?
- How to efficiently decrease the power consumption of an asynchronous pixel responding only to relative changes in light intensity?

To respond more precisely to these two questions, our study was divided into five chapters. The fundamentals behind the neuromorphic imager were firstly reviewed in Chapter 1. The architecture of the human retina was characterized, and the photodiode principles of operation were reminded. Moreover, some of its relevant figures of merit (fill factor, dynamic range, responsivity, efficiency, dark current and junction capacitances) were defined. A state of the art of the different dynamic vision sensors was also presented in Chapter 1. The Dynamic and Active pixel Vision Sensor from Brandli *et al.*, called DAVIS, stood out thanks to its good performances in dynamic range, power consumption and pixel complexity. This imager integrates both an active pixel sensor and a dynamic vision sensor to provide concurrently asynchronous events and synchronous absolute light information. The asynchronous events are produced thanks to a photoreceptor circuit, a switched capacitor amplifier circuit and two comparators, modeling respectively photoreceptors, bipolar and ganglion cells of the human retina, therefore providing answers to our first question.

Based on this analysis, an asynchronous neuromorphic pixel was studied to understand the different challenges to be overcome during its implementation. The pixel architecture was inspired from Brandly *et al.* work but was designed with three figures of merit in mind: power consumption, pixel area and dynamic range. Indeed, a biomimetic sensor must use as little power as possible while providing a high dynamic range and a low pixel area. Moreover, compared to state-of-the-art DVS working at 1.8 V or above, the main constraint added to this study is a supply voltage of 0.75 V to be compatible with the CAMEL image sensor from UCL. Guidelines were first given in Chapter 2 in order to provide a design methodology usable in any technology. The pixel principles of operation were studied before the discussion of each circuit block composing the pixel architecture.

The p^+/n-well/p-sub type photodiode was chosen for its high responsivity and the equations behind the switched capacitor amplifier were established. Moreover, guidelines about the transistor sizing were given during the discussion.

A pixel design in a mature 0.18 µm CMOS technology and supplied with 0.75 V was proposed in CHAPTER 3. The purpose of this chapter was to provide an efficient pixel design to respond efficiently to the three figures of merit targeted. Different simulations were realized to find the best transistors sizing.

Our pixel was characterized, fully validated and compared to state-of-the-art architectures in CHAPTER 4. Fifty transistors, one photodiode and two MIMCAPS were needed to efficiently implement it. Moreover, the proposed pixel exhibits the best dynamic range (140 dB) at the lowest static power consumption (20.54 nW/pixel) but at the expense of an increase in minimum latency (46.4 μs). Its design allows us to obtain an asynchronous pixel creating ON and OFF events each time a minimum change in light intensity of 10% is sensed while keeping a fixed pattern noise of 3%. Although this preliminary study does not integrate the layout, the minimum pixel area calculated is 10x10 µm^2 which is then promising compared to the literature. Hence, we succeeded in designing an efficient asynchronous pixel responding only to relative changes in light intensity at low power consumption and high dynamic range, answering therefore to our second question.

Trade-offs between minimum latency and power consumption were discussed in CHAPTER 5. By increasing power consumption to 191 nW, a minimum latency of 6.2 µs was obtained. Even though this result was still two times larger than the minimum latency reached in the DAVIS, it gave guidelines to easily decrease the feature. Finally, perspectives for future works were proposed. A necessary improvement of this study will be to realize the pixel layout and to integrate it to the image sensor from UCL. This would therefore result in a complete image sensor providing both asynchronous and synchronous light information.

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Appendix A

CAMEL

In 2016, an ultra-low power VGA time based CMOS imager (CAMEL) was developed at UCL [1]. CAMEL aims to integrate vision capabilities on the Internet-of-Things which requires ultra-low power and high resolution imagers. Their imager, schematized in FIGURE A.1, is based on previous works [2, 45].

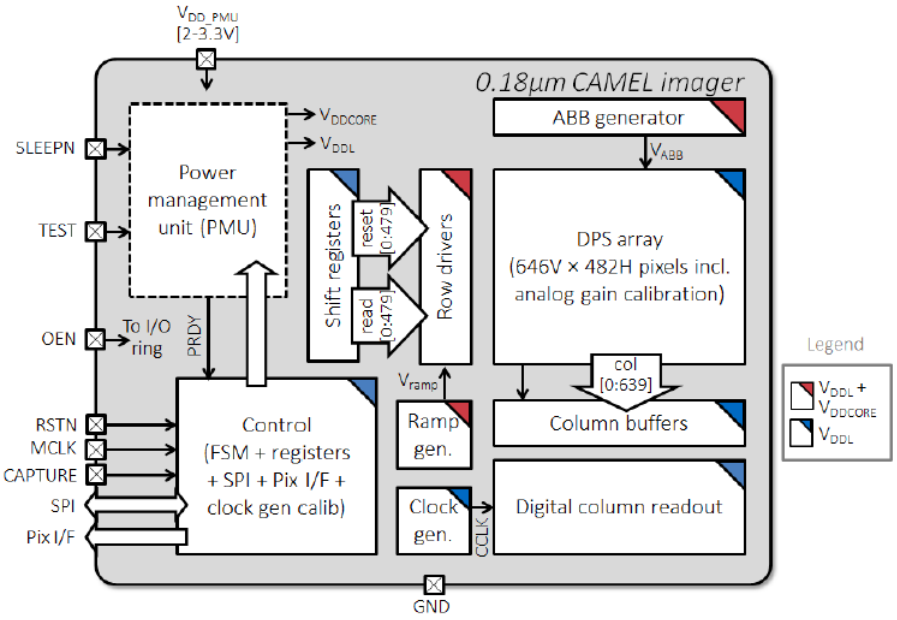

FIGURE A.1 – Architecture of the ultra-low power VGA time based CMOS imager codename "CAMEL" (from [1])

This time-based imager adapts three key innovations from [2]:

- *low power delta reset sampling:* at the reset level, the pixel signal is sampled and subtracted from the output signal as it corresponds to the offset of the in-pixel comparator. Therefore, the delta reset sampling reduces the the FPN occasioned by the pixel-to-pixel mismatch in the comparator.

- *wide range adaptive body biasing (ABB):* a voltage VABB is applied to the PMOS transistors body. The voltage is generated from a comparator replica located outside of the pixel array. Therefore, the ratio between the NMOS and the PMOS transistor is kept through the cross process corners.
- *low Zout gating of the 2T in-pixel comparator:* when the pixel is not read, the in-pixel comparator is gated. That allows to decrease the gate leakage current from the photodiode through the NMOS transistor of the comparator. Therefore, the power consumption decreases.

Compare to SunPixer [2], the CAMEL resolution is extended to VGA. Moreover, it integrates a DC/DC converter on the chip. Therefore, the chip is supplied by a single supply voltage. Finally, the CAMEL migrates the design from 65 nm to a more mature CMOS technology 0.18 µm while still maintaining a high DR and a low FPN inside a constrained power budget. The comparison between the SunPixer [2] and the CAMEL is presented in Table A.1.

Table A.1 – Performance result comparison between CAMEL and SunPixer [1].

	SunPixer	CAMEL
Technology	65 nm LP CMOS	0.18 µm RFCMOS
Array Resolution	128x128	640x480
Area	0.69 mm^2	18.276 mm^2
Supply voltage	0.5 V	0.6 V-0.8 V
Max frame rate	32 fps	8.5 fps
Pixel size	4x4 μm^2	5.8x5.8 μm^2
Fill factor	57%	32.4%
FPN	0.66% w/ DRS 9.3% w/o DRS	0.078% w/ DRS 0.62% w/o DRS
Temporal noise	0.4% w/ DRS 0.3% w/o DRS	0.100% w/ DRS 0.064% w/o DRS
Total power consumption	7.6 µW w/ DRS 5.6 µW w/o DRS @ 32 fps	470 µW w/ DRS 328 µW w/o DRS @ 8.5 fps
Energy	17 [pJ/frame/pixel] @ 32 fps	177.3 [pJ/frame/pixel] @ 8.5 fps
Dynamic range	42 dB w/ DRS 20 dB w/o DRS	61.6 dB w/ DRS 49.9 dB w/o DRS Peak SNR
Peak SNR	27 dB	37.5 dB

Appendix B

Single-stage CMOS operational amplifier

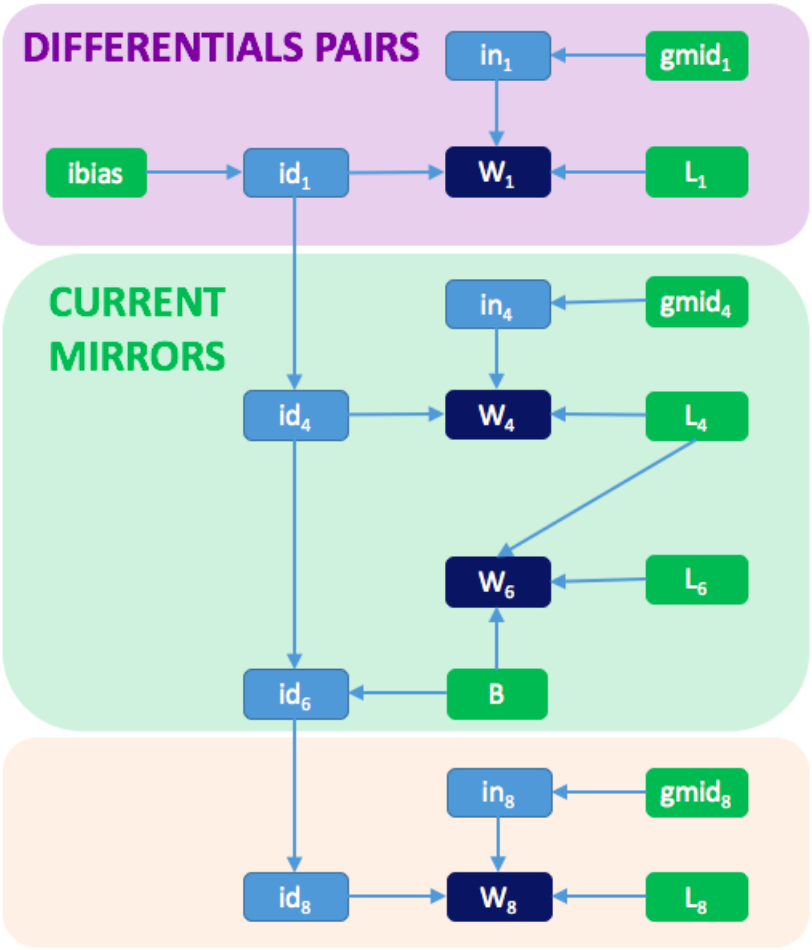

FIGURE B.1 – Design flow of the SOI CMOS Operational Amplifier.

Matlab Code

```
%-----------------------------------------------------
%------     ELEC2650    ----------------------------
%------ MATLAB CODE OTA ----------------------------
%-----------------------------------------------------
clc;
close all;
clear all;
format short e;
warning('off', 'MATLAB:interp1:NaNinY');

%% Library extraction
%-----------------------------------------------------
% you can access to :
% vgs, vdsat [V]
% dl, dw [um]
% in [A]
% gmid, gmsid, gdid
% cgg, cdd, css, cbb, cgs, csg, cds, csd, cdg, cgd, cgb, cbg, cdb, cbd, ...
    cbs, csb [F/m2]
% cgso, cgdo, cgbo, cbdj, cbsj [F/m]
%-----------------------------------------------------
% To access to Gm/Id for example : nlvtlp.gmid
%-----------------------------------------------------
[nmos.VGS nmos.DL nmos.DW nmos.VDSAT nmos.IN nmos.GMID nmos.GMSID ...
    nmos.GDID nmos.CGG nmos.CDD nmos.CSS nmos.CBB nmos.CGS nmos.CSG ...
    nmos.CDS nmos.CSD nmos.CDG nmos.CGD nmos.CGB nmos.CBG nmos.CDB ...
    nmos.CBD nmos.CBS nmos.CSB nmos.CGSO nmos.CGDO nmos.CGBO nmos.CBDJ ...
    nmos.CBSJ nmos.VEA] = textread('../eldo/data/N_18_MM.txt', '%f %f %f ...
    %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f ...
    %f %f %f %f ', 'headerlines', 2, 'whitespace', ' \b\t\n');
[pmos.VGS pmos.DL pmos.DW pmos.VDSAT pmos.IN pmos.GMID pmos.GMSID ...
    pmos.GDID pmos.CGG pmos.CDD pmos.CSS pmos.CBB pmos.CGS pmos.CSG ...
    pmos.CDS pmos.CSD pmos.CDG pmos.CGD pmos.CGB pmos.CBG pmos.CDB ...
    pmos.CBD pmos.CBS pmos.CSB pmos.CGSO pmos.CGDO pmos.CGBO pmos.CBDJ ...
    pmos.CBSJ pmos.VEA] = textread('../eldo/data/P_18_MM.txt', '%f %f %f ...
    %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f %f ...
    %f %f %f %f ', 'headerlines', 2, 'whitespace', ' \b\t\n');

%% Data modification: suppressing first points to obtain a monotonic ...
    function (for splines)
M = max(nmos.GMID);   Inl = find(nmos.GMID==M, 1, 'last');
M = max(pmos.GMID);   Ipl = find(pmos.GMID==M, 1, 'last');

nmos.VGS = nmos.VGS(Inl:end);   nmos.IN = nmos.IN(Inl:end);   nmos.GMID ...
    = nmos.GMID(Inl:end);
pmos.VGS = pmos.VGS(Ipl:end);   pmos.IN = pmos.IN(Ipl:end);   pmos.GMID ...
    = pmos.GMID(Ipl:end);

%% Obtain techno curves
obtain_techno_curves({nmos}, {'nmos'});
obtain_techno_curves({pmos}, {'pmos'});

%% Specifications
```

```
38 ibias = 1e-9;
39 CL = 1e-15;
40
41 L1 = 4e-6   ; L2 = L1;
42 L3 = 500e-9 ; L4 = L3;
43 L5 = 500e-9 ; L6 = L5;
44 L7 = 2e-6   ; L8 = L7;
45
46 %% Design choice
47 B = 1;
48 gmid1 = 35;
49 gmid4 = 25;
50 gmid6 = gmid4;
51 gmid8 = 28;
52
53 M1 = nmos;
54 M4 = pmos;
55 M6 = pmos;
56 M8 = nmos;
57
58 %% Design algorithm
59 id1 = ibias/2;
60 gm1 = id1*gmid1;
61 fT = (gm1*B)/(2*pi*CL);
62 in1 = 10.^interp1(M1.GMID, log10(M1.IN), gmid1);
63 vgs1 = interp1(M1.GMID, M1.VGS, gmid1);
64 W1 = id1/in1*L1;
65
66 id4 = id1;
67 in4 = 10.^interp1(M4.GMID, log10(-M4.IN), gmid4);
68 vsg4 = interp1(M4.GMID, M4.VGS, gmid4);
69 W4 = id1/in4*L4;
70 gm4 = gmid4*id1;
71
72 W6 = B*W4*L6/L4;
73 id6 = id4*B;
74
75 id8 = id6;
76 VOUT = interp1(M8.GMID, M8.VGS, gmid8);
77 in8 = 10.^interp1(M8.GMID, log10(M8.IN), gmid8);
78 gm8 = gmid8*id8;
79 W8 = id8/in8*L8;
80
81 Cgs1 = 2/3*interp1(M1.GMID, M1.CGS, gmid1)*W1*L1;
82 Cgs4 = 2/3*interp1(M4.GMID, M4.CGS, gmid4)*W4*L4;
83 Cgs6 = 2/3*interp1(M6.GMID, M6.CGS, gmid6)*W6*L6;
84 Cgso4 = interp1(M4.GMID, M4.CGSO, gmid4)*W4;
85 Cgso6 = interp1(M6.GMID, M6.CGSO, gmid6)*W6;
86 Cgdo2 = interp1(M1.GMID, M1.CGDO, gmid1)*W1;
87 Cgdo6 = interp1(M6.GMID, M6.CGDO, gmid6)*W6;
88 Cbd2 = interp1(M1.GMID, M1.CBDJ, gmid1)*W1;
89 Cbd4 = interp1(M4.GMID, M4.CBDJ, gmid4)*W4;
90
91 Cgs7 = 2/3*interp1(M8.GMID, M8.CGS, gmid7)*W8*L8;
92 Cgs8 = 2/3*interp1(M8.GMID, M8.CGS, gmid8)*W8*L8;
93 Cgso7 = interp1(M8.GMID, M8.CGSO, gmid7)*W8;
```

```
Cgso8 = interp1(M8.GMID, M8.CGSO, gmid8)*W8;
Cgdo5 = interp1(M6.GMID, M6.CGDO, gmid6)*W6;
Cgdo8 = interp1(M8.GMID, M8.CGDO, gmid8)*W8;
Cbd7 = interp1(M8.GMID, M8.CBDJ, gmid8)*W8;
Cbd5 = interp1(M6.GMID, M6.CBDJ, gmid6)*W6;

Cgd2 = interp1(M1.GMID, M1.CDG, gmid1)*W1*L1;
Cgd6 = interp1(M6.GMID, M6.CDG, gmid6)*W6*L6;

cpp = Cgs4+Cgs6+Cgso4+Cgso6+Cgdo2+Cgdo6+Cbd2+Cbd4;%+Cgd2+Cgd6;
cpn = Cgs7+Cgs8+Cgso7+Cgso8+Cgdo5+Cgdo8+Cbd7+Cbd5;%+Cgd5+Cgd8;

Veaeq = 1/(1/interp1(M6.GMID, M6.VEA, gmid6) + 1/interp1(M8.GMID, ...
    M8.VEA, gmid8));

Gain = gmid1*Veaeq;

Poled = id7./Veaeq/CL/2/pi;
Polep = gm4/(2*pi*cpp);
Polen = gm7/(2*pi*cpn);
Zeron = 2*Polen;

fprintf('-----------------------------------------------------------\n');
fprintf('Performances\n')
fprintf('-----------------------------------------------------------\n');
fprintf('Gain : %g \n', Gain);
fprintf('Gain : %g [dB]\n', 20*log10(Gain));
fprintf('GBW : %g [Hz]\n',fT);
fprintf('Position du pole : %g [MHz]\n',Polep*1e-6);
fprintf('Position du doublet : %g [MHz]\n',Polen*1e-6);
fprintf('Courant de polarisation : %g [nA]\n', 2*id1*1e9);
fprintf('Power : %g [nW]\n', 4*id1*0.75*1e9);
fprintf('-----------------------------------------------------------\n');
fprintf('Point DC\n')
fprintf('-----------------------------------------------------------\n');
fprintf('vgs1 : %3.2g [V]\n', vgs1);
fprintf('vsg4 : %3.2g [V]\n', vsg4);
fprintf('-----------------------------------------------------------\n');
fprintf('Dimensionnement\n')
fprintf('-----------------------------------------------------------\n');
fprintf('W1 : %3.2g [nm]\n', W1*1e9);
fprintf('W4 : %3.2g [nm]\n', W4*1e9);
fprintf('W6 : %3.2g [nm]\n', W6*1e9);
fprintf('W8 : %3.2g [nm]\n', W7*1e9);
```

Appendix C

Photodiode layout

The DIOP_MM and DIONW_MM layouts are represented in Figure C.1 and C.2 respectively with the size given at each photodiode in this study.

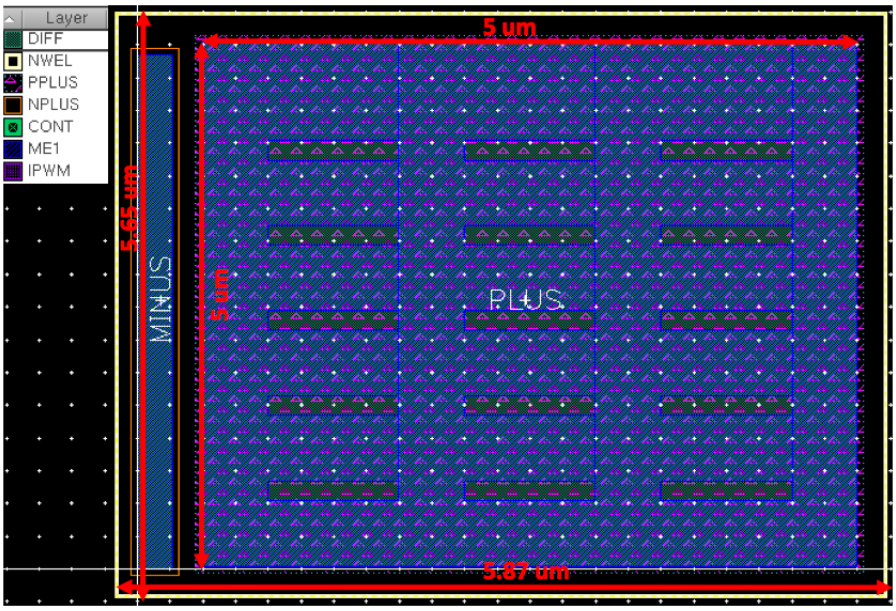

Figure C.1 – DIOP_MM layout.

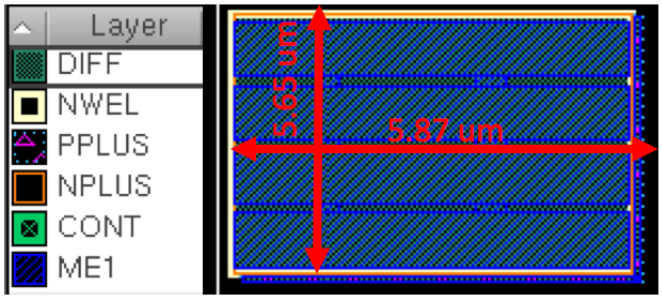

Figure C.2 – DIONW_MM layout.

Appendix D

Eldo script

```
*****************************************************
**** DVS circuit ********************************
*****************************************************

.include '/users/rousseauna/CMOS018_RFMOD_MC.lib'
.option gmin=1e-24
.option AEX
.option NOCATMX
.option be
.temp '25'

* -- VOLTAGE GENERATION ------------------------------
.PARAM VDD=0.75
VVREF  VREF   AVSS DC 150m
VVON   ON_TH  AVSS DC 'VDD/2 - 30m'
VVOFF  OFF_TH AVSS DC 'VDD/2 + 30m'
VVDD_2 VDD_2  AVSS DC 'VDD/2'
VDD    AVDD   AVSS DC VDD
VGND   AVSS   0    DC 0


* -- PHOTORECEPTOR CIRCUIT ------------------------------
*PHOTORECEPTOR_CIRCUIT
xMN6 AVDD VPR  VPD  AVSS N_33_MM w=240n l=800n
xMN7 VPR  VPD  AVSS AVSS n_18_mm w=400n l=800n

D0 AVSS VPD diop_mm  l=5e-6    w=5e-6    m=1
D1 AVSS VPD dionw_mm l=5.87e-6 w=5.65e-6 m=1
IPH VPD AVSS DC 2p PULSE (11p 14.3p 2m 1f 1f 40m 100m)

*Mirror current
xMP1     VPR VN   AVDD AVDD p_18_mm w=400n l=500n
xMirror1 VN  VN   AVDD AVDD p_18_mm w=400n l=500n
xMirror2 VN  VREF AVSS AVSS n_18_mm w=400n l=800n
```

```
* -- SWITCHED CAP AMP -------------------------------
xMSWITCH  VA  RESET  VAMP  AVSS n_18_mm w=240n l=180n
xMSWITCHP VA  RESETN VAMP  AVDD p_18_mm w=240n l=180n
C1        VA  VAMP   mimcaps_mm L=1.28u w=1.28u M=1
C2        VPR VA     mimcaps_mm L=1.28u w=1.28u M=15

*AMP
xMAMP1  N3    VA     N4    AVSS n_18_mm w=500n l=4u
xMAMP2  N1    VDD_2  N4    AVSS n_18_mm w=500n l=4u
xMAMP3  N3    N3     AVDD  AVDD p_18_mm w=1u   l=500n
xMAMP4  N1    N1     AVDD  AVDD p_18_mm w=1u   l=500n
xMAMP5  N2    N3     AVDD  AVDD p_18_mm w=1u   l=500n
xMAMP6  VAMP  N1     AVDD  AVDD p_18_mm w=1u   l=500n
xMAMP7  N2    N2     AVSS  AVSS n_18_mm w=3u   l=2u
xMAMP8  VAMP  N2     AVSS  AVSS n_18_mm w=3u   l=2u
xMAMP9  N4    NB     AVSS  AVSS n_18_mm w=500n l=2u
xMAMP10 NB    NB     AVSS  AVSS n_18_mm w=500n l=2u
IAMP    AVDD  NB     DC    10n

* -- COMPARATORS -------------------------------------
*COMP_ON
xMCON1  NCON3 VAMP   NCON4 AVSS n_18_mm w=500n l=4u
xMCON2  NCON1 ON_TH  NCON4 AVSS n_18_mm w=500n l=4u
xMCON3  NCON3 NCON3  AVDD  AVDD p_18_mm w=1u   l=500n
xMCON4  NCON1 NCON1  AVDD  AVDD p_18_mm w=1u   l=500n
xMCON5  NCON2 NCON3  AVDD  AVDD p_18_mm w=1u   l=500n
xMCON6  VCON  NCON1  AVDD  AVDD p_18_mm w=1u   l=500n
xMCON7  NCON2 NCON2  AVSS  AVSS n_18_mm w=3u   l=2u
xMCON8  VCON  NCON2  AVSS  AVSS n_18_mm w=3u   l=2u
xMCON9  NCON4 NBON   AVSS  AVSS n_18_mm w=500n l=2u
xMCON10 NBON  NBON   AVSS  AVSS n_18_mm w=500n l=2u
ICON    AVDD  NBON   DC    1n

*COMP_OFF
xMCOF1  NCOF3 OFF_TH NCOF4 AVSS n_18_mm w=500n l=4u
xMCOF2  NCOF1 VAMP   NCOF4 AVSS n_18_mm w=500n l=4u
xMCOF3  NCOF3 NCOF3  AVDD  AVDD p_18_mm w=1u   l=500n
xMCOF4  NCOF1 NCOF1  AVDD  AVDD p_18_mm w=1u   l=500n
xMCOF5  NCOF2 NCOF3  AVDD  AVDD p_18_mm w=1u   l=500n
xMCOF6  VCOF  NCOF1  AVDD  AVDD p_18_mm w=1u   l=500n
xMCOF7  NCOF2 NCOF2  AVSS  AVSS n_18_mm w=3u   l=2u
xMCOF8  VCOF  NCOF2  AVSS  AVSS n_18_mm w=3u   l=2u
xMCOF9  NCOF4 NBOF   AVSS  AVSS n_18_mm w=500n l=2u
xMCOF10 NBOF  NBOF   AVSS  AVSS n_18_mm w=500n l=2u
ICOF    AVDD  NBOF   DC    1n
```

```
* -- LOGIC ---------------------------------------
*INV1_OFF
xM9  NINVOF VCOF   AVDD AVDD p_33_mm w=340n l=340n
xM10 NINVOF VCOF   AVSS AVSS n_33_mm w=680n l=680n

*INV2_OFF
xM17 OFF_E  NINVOF AVDD AVDD p_33_mm w=340n l=340n
xM16 OFF_E  NINVOF AVSS AVSS n_33_mm w=680n l=680n


*INV1_ON
xM18 NINVON VCON   AVDD AVDD p_33_mm w=340n l=340n
xM19 NINVON VCON   AVSS AVSS n_33_mm w=680n l=680n

*INV42_ON
xM21 ON_E   NINVON AVDD AVDD p_33_mm w=340n l=340n
xM20 ON_E   NINVON AVSS AVSS n_33_mm w=680n l=680n


*INV_RESET
xM56 RESETN RESET  AVDD AVDD p_18_mm w=240n l=180n
xM58 RESETN RESET  AVSS AVSS n_18_mm w=480n l=360n

*OR1_ON_OFF
xMOR1 NOR1  OFF_E  AVDD AVDD p_18_mm w=240n l=180n
xMOR2 RESET NOR2   AVDD AVDD p_18_mm w=240n l=180n
xMOR3 NOR2  ON_E   NOR1 AVDD p_18_mm w=240n l=180n
xMOR4 RESET NOR2   AVSS AVSS n_18_mm w=480n l=360n
xMOR5 NOR2 ON_E    AVSS AVSS n_18_mm w=500n l=400n
xMOR6 NOR2 OFF_E   AVSS AVSS n_18_mm w=500n l=400n


* -- SIMULATION ----------------------------------------------
.TRAN 0.1m 15m
.PLOT TRAN V(ON_TH) V(OFF_TH) V(VAMP) V(VPR) V(RESET) V(VBUF) V(VPD) V(VA) I(IPH)
.PROBE V
.PROBE I

* MC simulations
*.mc 10000 all
*.mprun max_nbjobs=4

* Corner simulations
*.include '/users/rousseauna/CMOS018_RFMOD_corners.lib'
```

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