

École polytechnique de Louvain

Design of an inverter for flywheel energy storage systems in space applications

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Academic year 2025–2026
Master [120] in Electrical Engineering

Abstract

Flywheel Energy Storage Systems are a promising alternative to chemical batteries for low Earth orbit satellites, offering higher efficiency, longer lifetime, and tolerance to deep discharges. This master's thesis addresses the design and experimental validation of the inverter at the heart of such a system, with a focus on the trade-offs between semiconductor technology, switching frequency, bus voltage, and modulation strategy under the constraints defined by the European Cooperation for Space Standardization.

A datasheet-based analytical loss model is developed for a single inverter leg and applied to ten candidate switches spanning Si, SiC, and GaN technologies. The IGOT65R025D2 GaN High-Electron-Mobility Transistor from Infineon is selected for its performance, radiation tolerance, and space qualification and is analyzed in greater depth. The full inverter design is carried out, encompassing the gate driver, input filter, thermal budget, and LTspice simulations. A single-leg prototype on a four-layer PCB confirms the simulation results: measured switching waveforms and power losses are in good agreement with the model, validating it as a reliable basis for scaling to a complete three-phase inverter.

Acknowledgment

This work would not have been possible without the help and support of many people, and I am grateful to each of them.

First and foremost, I would like to thank my supervisor, Professor Marc Bekemans, for giving me the opportunity to work on this subject and for his active involvement at the key stages of the project. His experience in the field made his advice consistently valuable, and his guidance shaped the direction of this work in meaningful ways. I am also grateful to him for encouraging me to include an experimental component in the project. Designing a PCB, selecting components, soldering, debugging, and conducting high-voltage tests were all experiences I had never had before, and they gave me a real bridge between theory and the practical realities of power electronics.

I would also like to thank Benjamin Spitaels, who supported my day-to-day work and was especially present in the final stretch of the project. The time we spent together in the laboratory was invaluable: without his guidance and hands-on expertise, safely conducting the experimental tests would simply not have been possible.

My thanks also go to the CREDEM team at UCLouvain. Thierry Daras gave me access to the university's laboratory and equipment, and patiently answered my many questions during the prototype preparation phase. Simon De Jaeger taught me how to solder components onto a PCB and helped me through the more technical steps of the experimental phase.

Finally, I want to thank my parents, sisters, and friends for their support and for making these five years of study such a rewarding experience.

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List of Acronyms

BLDC Brushless Direct Current.

DoD Depth of Discharge.

ECSS European Cooperation for Space Standardization.

EMF Electromotive Force.

FESS Flywheel Energy Storage System.

FET Field-Effect Transistor.

FWM Full Wave Modulation.

HEMT High Electron Mobility Transistor.

IGBT Insulated Gate Bipolar Transistor.

LEO Low Earth Orbit.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

PCB Printed Circuit Board.

PMSM Permanent Magnet Synchronous Machine.

RMS Root Mean Square.

rpm Revolutions Per Minute.

SPWM Sinusoidal Pulse Width Modulation.

TIM Thermal Interface Material.

THIPWM Third Harmonic Injection Pulse Width Modulation.

WBG Wide Band Gap.

WTHD Weighted Total Harmonic Distortion.

1 Introduction

Low Earth Orbit (LEO) satellites operate at relatively low altitudes (around 800 km). This configuration provides low communication latency, reduced transmission power requirements, and lower launch costs. Consequently, LEO satellites are widely used for telecommunication applications [1]. Making several orbits per day, they regularly pass through Earth’s shadow. However, since satellites rely on photovoltaic panels for power generation, they require an energy storage system to remain operational when sunlight is unavailable. This is traditionally achieved using batteries, but recent technological advances have made Flywheel Energy Storage Systems (FESSs) a promising alternative for space applications [2].

1.1 Flywheel energy storage system

Space missions require energy storage systems with long operational lifetimes. In chemical batteries, the Depth of Discharge (DoD) has a strong impact on cycle life: deeper discharges shorten the number of usable cycles and thus reduce lifetime, see Figure 1.1. This limitation is particularly significant for LEO satellites, which undergo frequent eclipses and therefore experience many charge–discharge cycles.

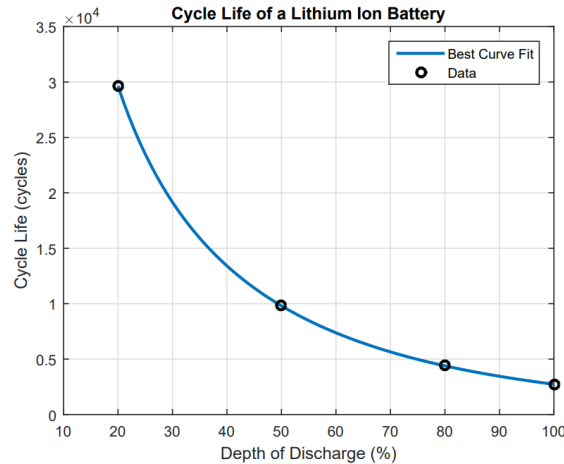


Figure 1.1: Impact of depth of discharge on cycle life of batteries [3].

To preserve lifetime, only a small portion of a satellite’s battery capacity is actually used, which lowers the effective specific energy (Wh/kg) of the system. FESSs overcome this issue by tolerating a much higher depth of discharge without significant degradation. As a result,

they offer higher specific energy, as well as superior efficiency and service life compared to chemical batteries. A comparison between both technologies (without taking the DoD into account) is summarized in Table 1.1 [4][5][6].

	Chemical Battery	Flywheel
Efficiency	70–80%	85–95%
Specific energy (Wh/kg)	30–200	5–150
Service life (years)	3–15	> 20

Table 1.1: Comparison of battery and flywheel energy storage technologies [4][5][6].

A typical FESS consists of a flywheel, a motor/generator, a power electronic converter, and a control system, as illustrated in Figure 1.2. When electricity production exceeds demand, the flywheel accelerates and stores the surplus as rotational kinetic energy. Conversely, during power demand, the flywheel decelerates, converting stored kinetic energy back into electricity. The stored kinetic energy is given by:

$$E_{kin} = \frac{1}{2} J \omega^2 \quad (1.1)$$

where J is the moment of inertia of the flywheel and ω its angular velocity. As shown in Equation 1.1, reducing the flywheel speed by a factor of two releases 75% of its stored kinetic energy.

The inverter controls the motor/generator, converting the mechanical energy stored in the flywheel into electrical power suitable for the spacecraft's bus. Therefore, the inverter must be both efficient and reliable while meeting the specific constraints of space applications, such as radiation tolerance and thermal management.

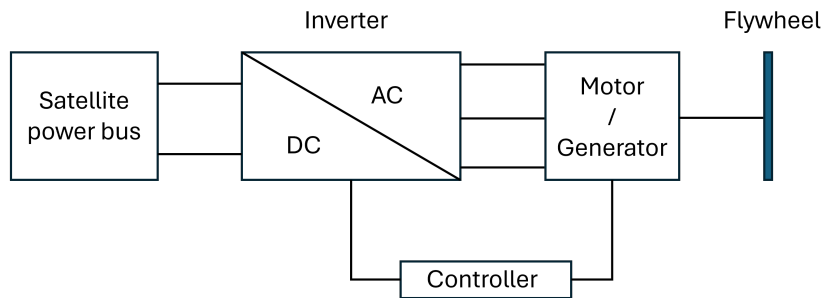


Figure 1.2: General structure of a FESS.

The target specifications of the FESS in the context of this master's thesis are summarized in Table 1.2.

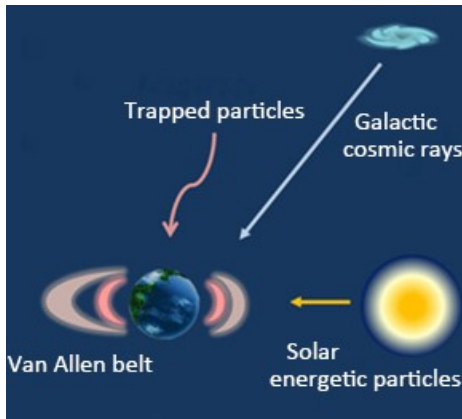
Feature	Target Value
Storage Capacity	2.5 kWh
Peak Power	8 kW
Depth of Discharge	75%
Maximum Motor Speed	50 000 rpm
Satellite Power Bus Voltage	28 V / 70 V / (150 V)

Table 1.2: Flywheel energy storage system specifications.

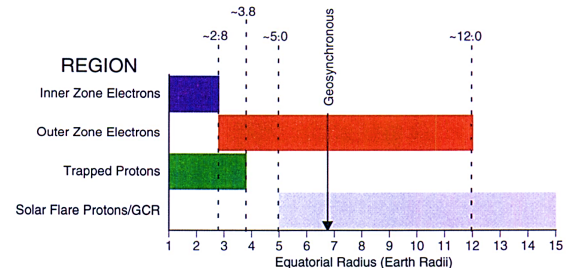
The value of 150 V for the bus voltage is included in parentheses because it is not a standard bus voltage in this context, but it is considered as a potential option that could be enabled by the use of a DC-DC converter between the satellite bus and the inverter.

1.2 Space environment

The space environment is characterized by high radiation levels, which can significantly impact the performance of on-board electronic systems. In orbit around the Earth, spacecraft are exposed to two main types of radiation: trapped radiation and transient radiation [7]. The trapped radiation consists of charged particles confined to certain regions of space (called the Van Allen belts) by the Earth's magnetic field. The transient radiation is composed of solar particles emitted during solar flares and cosmic rays originating from outside the solar system. Figure 1.3a illustrates the different origins of space radiation. In Figure 1.3b, the significant types of radiation depending on the distance from the center of the Earth are presented. According to this figure, the main source of radiation for LEO satellites (altitude lower than 1 earth radius), is the trapped radiation.



(a) Origins of radiation in space [8].



(b) Regions of significant radiation around Earth [7].

Figure 1.3: Space radiation.

The effects of radiation on electronic components are as follows [7]:

- Total Ionizing Dose: the cumulative effect of ionizing radiation. Charge accumulation in insulating materials can alter the potential at the interface structure.
- Displacement Damage Dose: the cumulative effect of non-ionizing radiation. When the energy absorbed by lattice atoms exceeds their binding energy, atomic displacement occurs.

- Single Event Effects: caused by a single charged particle striking a sensitive region of a microelectronic device. Effects range from transient logic upsets to permanent device destruction.

To mitigate these effects, radiation-hardened components are used, shielding is applied, and sensitive devices are derated according to European Cooperation for Space Standardization (ECSS) guidelines [9].

1.3 Objectives

This master's thesis focuses on the design of an inverter for flywheel energy storage for space applications. It provides a structured methodology for the system design, analyzing the impact of the following choices on the performance of the inverter:

- Supplied power and voltage levels
- Choice of power semiconductor technology
- Modulation strategy and switching frequency

The goal is to answer the following question: how should a three-phase inverter be designed and validated for driving a high-speed motor in a FESS with the given specifications intended for LEO applications, and what are the critical trade-offs between semiconductor technology, switching frequency, bus voltage, and modulation strategy?

The methodology and general organization of this work were partially inspired by previous work conducted in [10].

1.4 Methodology

First, a review of inverter topologies, modulation strategies, power semiconductor technologies, and synchronous machine fundamentals will be conducted. The objective is to choose a suitable topology for the inverter and the expected levels of voltage, current and switching frequencies.

Then, a theoretical simplified model of the switch will be developed. This model will be used to compute the expected losses (conduction and switching losses) of the transistors. The goal will be to analyze the impact of switching frequencies and current levels on these losses. Key parameters will be identified to allow an efficient comparison between different kinds of power semiconductor technology.

After that, simulation will be conducted on LTspice and a complete design guide for the inverter will be proposed, including the design of the gate driver and the input filter. The thermal management of the system will also be studied.

Finally, a prototype of a single-leg inverter will be built and tested. The experimental results will be compared with the simulations to validate the design choices made during the project.

2 System description

With the application context and target specifications established, the next step is to determine the operating envelope that the inverter must satisfy. This requires answering two questions before any component can be selected: what switching frequency is imposed by the motor speed and the chosen modulation strategy, and what maximum phase current must the inverter supply across the full speed range of the flywheel?

This chapter addresses both questions systematically, and a designer reusing this work can extract the following from this chapter:

- a comparison of the modulation strategies in terms of output voltage quality, DC bus utilization, and switching frequency requirements, given in Table 2.3.
- a lower bound on the maximum phase current as a function of bus voltage, motor synchronous inductance, and flux-weakening angle, given in Figures 2.16 and 2.17 for the two- and four-flywheel configurations.

These results feed directly into the loss model and component comparison of Chapters 3 and 4. Any change to the bus voltage, the motor design, or the number of flywheels is reflected immediately in the current estimates, without requiring the loss model itself to be rederived.

2.1 Inverter

2.1.1 Topologies

The electrical schematic of a classical three-phase inverter is shown in Figure 2.1. Each phase is connected to one inverter leg composed of two switches. The switches operate alternately to connect the midpoint either to $+0.5V_{DC}$ or $-0.5V_{DC}$, thus generating an AC voltage.

Alternative inverter topologies also exist. If the connected motor has open-ended windings, the three-phase inverter can be replaced by three single-phase full-bridge inverters. Each full-bridge inverter connects its single-phase load between two inverter legs, which increases the total number of switches. However, when switching losses dominate over conduction losses, this configuration can be advantageous for achieving the same Root Mean Square (RMS) phase current ripple [11]. Since the motor in this application operates at high speed, the required switching frequency is high, increasing switching losses. Therefore, the full-bridge configuration may be a suitable choice in this context. Nevertheless, the classical

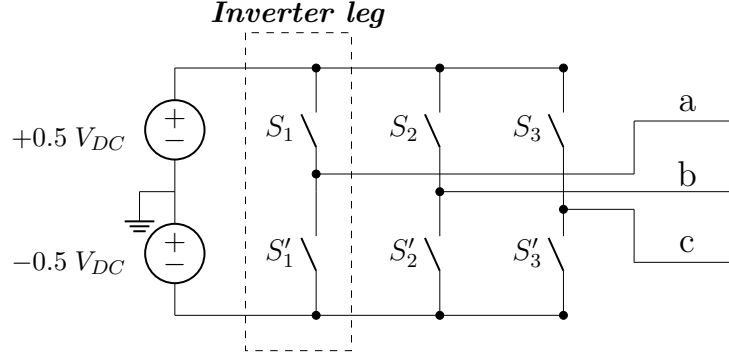


Figure 2.1: Classical three-phase inverter circuit schematic.

three-phase inverter topology will be studied in greater detail in this work, since it reduces the number of switches and does not require open-ended windings.

Multilevel inverter topologies have also been developed. By increasing the number of switches per leg, the output midpoint can take more discrete voltage levels (three in the case of a three-level inverter). This enables higher bus voltages using the same semiconductor devices, because voltage stress is distributed across more switches. This topology, represented in Figure 2.2, is particularly advantageous for applications where the voltage level is higher, compared to the bus voltage of a satellite.

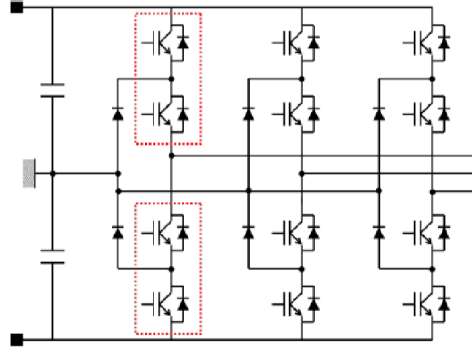


Figure 2.2: Three-level three-phase inverter circuit schematic [12].

2.1.2 Efficiency

Inverters lose most of their power through the semiconductor switches [13]. Two main types of losses can be distinguished. The first are conduction losses, caused by the voltage drop across the switch when it conducts current. The second are switching losses, which occur during the transitions between the on and off states. These are particularly significant at high switching frequencies, as in high-speed motor drives.

The overall efficiency η of the inverter depends on the output power P and the total losses, as expressed in Equation 2.1:

$$\eta = \frac{P}{P + P_{cond} + P_{switch}} \quad (2.1)$$

2.1.3 Modulation techniques

Several common modulation techniques are presented below. The choice of modulation method affects both the inverter efficiency and the quality of the output waveform. Increasing the switching frequency generally improves output power quality by reducing low-order harmonics, but also raises switching losses, thereby lowering overall efficiency. The techniques discussed here are illustrated using the typical three-phase inverter topology shown in Figure 2.1, though the principles apply to other configurations as well.

Key metrics used to compare modulation techniques include [14]:

- **Weighted Total Harmonic Distortion (WTHD):** A modified version of the Total Harmonic Distortion (THD) that weights each harmonic by its order, since low-order harmonics induce proportionally larger current distortion in the load. It is defined as:

$$wTHD = \sqrt{\sum_{h=2}^{\infty} \left(\frac{V_h}{hV_1} \right)^2} \quad (2.2)$$

where V_h is the RMS amplitude of the h^{th} harmonic. The acceptable harmonic content depends on the equipment driven by the inverter. For motors, harmonics increase losses, generate torque ripple, and raise the risk of overheating [15], which reduces efficiency and shortens lifetime.

- **Switching frequency (f_{sw}):** The rate at which the semiconductor switches turn on and off. Higher f_{sw} improves waveform quality but increases switching losses.
- **DC bus utilization ratio (λ):** The ratio of the fundamental peak phase-to-phase output voltage to the DC bus voltage.

Sinusoidal pulse width modulation

The Sinusoidal Pulse Width Modulation (SPWM) technique controls the switching of the inverter transistors by comparing a high-frequency carrier signal with a low-frequency sinusoidal modulating signal, as illustrated in Figure 2.3. When the carrier signal is higher than the modulating signal, the phase output voltage V_A equals $-V_{DC}/2$; when it is lower, V_A equals $V_{DC}/2$. This process is applied independently to each phase by operating the corresponding switches.

By adjusting the amplitude of the modulating signal, the RMS value of the output voltage can be controlled. The modulation index m is defined as the ratio between the amplitude of the modulating signal and that of the carrier signal. The frequency of the modulating signal determines the output voltage frequency, while the carrier frequency defines the switching frequency.

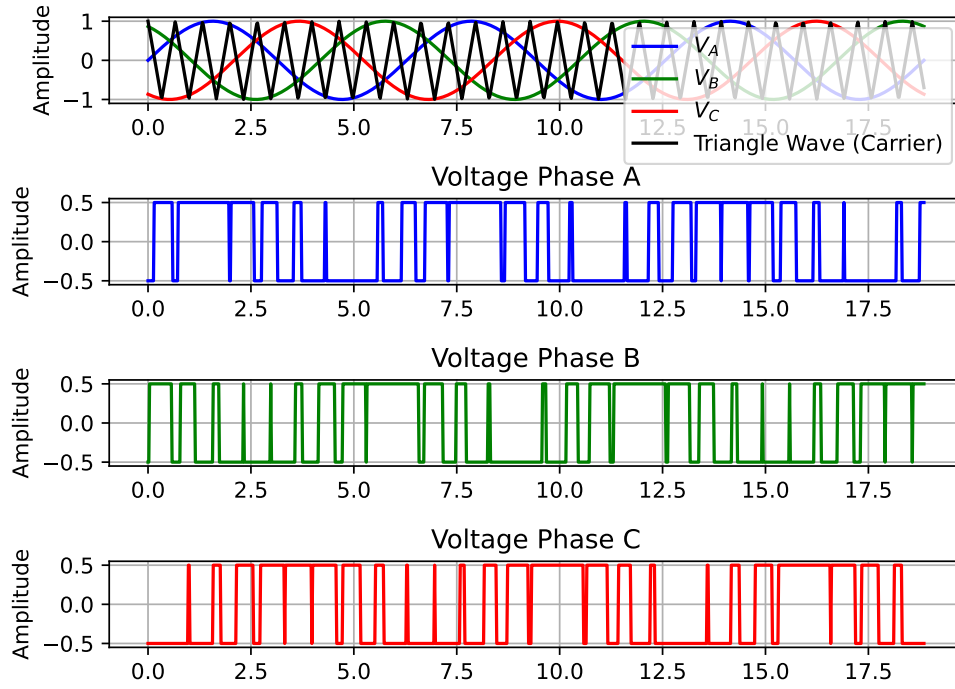


Figure 2.3: Illustration of the SPWM principle.

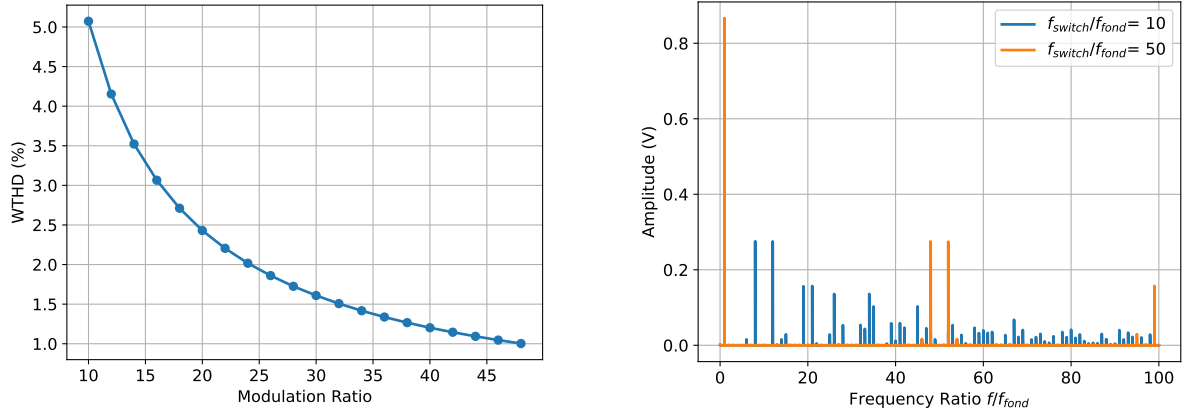
To ensure proper operation, the ratio $n = f_{sw}/f$ between the switching frequency and the modulating frequency should satisfy the conditions in Table 2.1, depending on whether f_{sw} is a synchronous multiple of f [12]:

	f_{sw}/f
Asynchronous operation	≥ 20
Synchronous operation	$8 - 20$

 Table 2.1: Recommended ratio n between switching and modulating frequencies [12].

However, since the modulating frequency is determined by the motor speed, choosing synchronous operation would require constantly adapting the switching frequency, which is not practical.

The WTHD depending on the switching-to-modulating frequency ratio n is shown in Figure 2.4a. It can be seen that increasing the switching frequency reduces this metric, improving the output voltage quality. This can be explained by the spectrum of the output phase-to-phase voltage, shown in Figure 2.4b for a modulating frequency of 800 Hz and a bus voltage of 1V. The peaks that can be seen on this figure are pushed further away from the fundamental when the switching frequency is increased, thus lowering the WTHD. Incidentally, it can be seen that the amplitude of the fundamental is approximately 0.866 times the DC bus voltage, which corresponds to a DC bus utilization ratio λ of 0.866.



(a) WTHD of the output phase-to-phase voltage. (b) Spectrum of the output phase-to-phase voltage for two different values of n with a DC bus voltage of 1V.

Figure 2.4: Output voltage quality for SPWM technique

The modulation index m also affects the output voltage quality. This is shown in Figure 2.5.

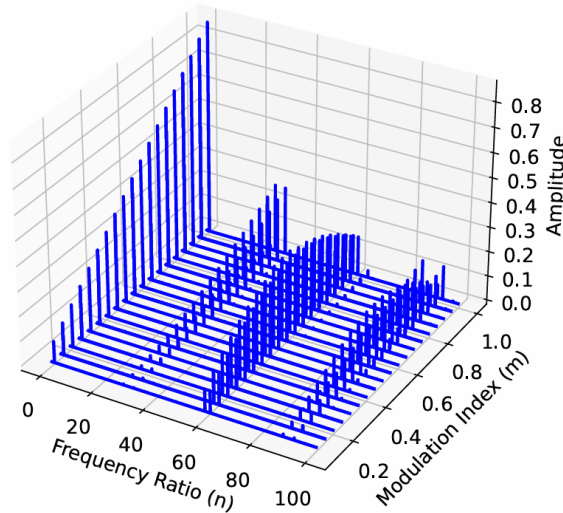


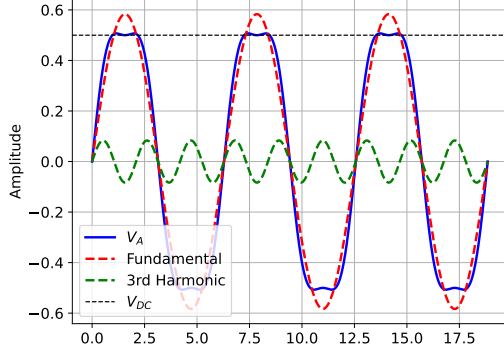
Figure 2.5: Spectrum of the output phase-to-phase voltage using the SPWM technique depending on the modulation index m for $f_{sw} = 30f$ and a DC bus voltage of 1V.

Third harmonic injection pulse width modulation

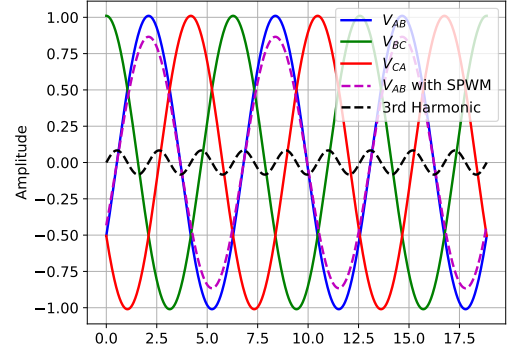
The Third Harmonic Injection Pulse Width Modulation (THIPWM) increases the usable DC bus voltage by approximately 15%. The technique consists of adding a third-harmonic component to the fundamental modulating signal as illustrated in Figure 2.6a. The resulting modulating waveform (shown in blue) is the sum of the fundamental and a third-harmonic component that is in phase with it.

As shown in Figure 2.6b, the third harmonics are common to all three phases. Consequently, they cancel out in the phase-to-phase voltages, which means that they are not seen by the

motor and therefore do not affect torque production or overall motor operation. The neutral point voltage, however, is modified by the injection. For this reason, the neutral point must remain floating to prevent homopolar currents [12].



(a) Third harmonic injection principle, phase-to-neutral voltages.



(b) Output phase-to-phase voltage using the THIPWM technique.

Figure 2.6: Illustration of the THIPWM technique.

As shown in Figure 2.6, the amplitude of the fundamental, and thus the DC bus utilization ratio, is increased to 1. Except for this, the spectrum of the output phase-to-phase voltage (here shown with $f = 800$ Hz and a switching-to-fundamental frequency ratio of 30) is very similar to the one of the SPWM technique. The WTHD is slightly reduced to 1.36% compared to 1.56% for SPWM.

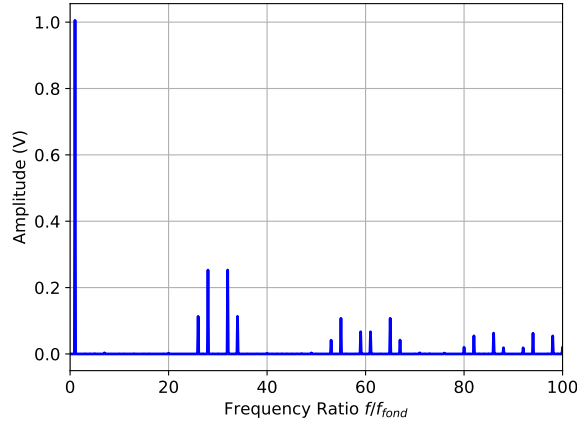


Figure 2.7: Spectrum of the phase-to-phase voltage for the THIPWM technique.

Full wave modulation

The Full Wave Modulation (PWM) technique consists in applying square waveforms directly to the motor terminals. It allows a high utilization of the DC bus voltage. The switching frequency is also reduced compared to SPWM, which lowers the switching losses. However, the low-order harmonic content of the output voltage is higher, which can be detrimental to motor operation. In addition, these harmonics are more difficult to filter. As illustrated

in Figure 2.8a, the phase-to-neutral voltages are square waveforms, and the phase-to-phase voltages are “quasi-square” waveforms (Figure 2.8b).

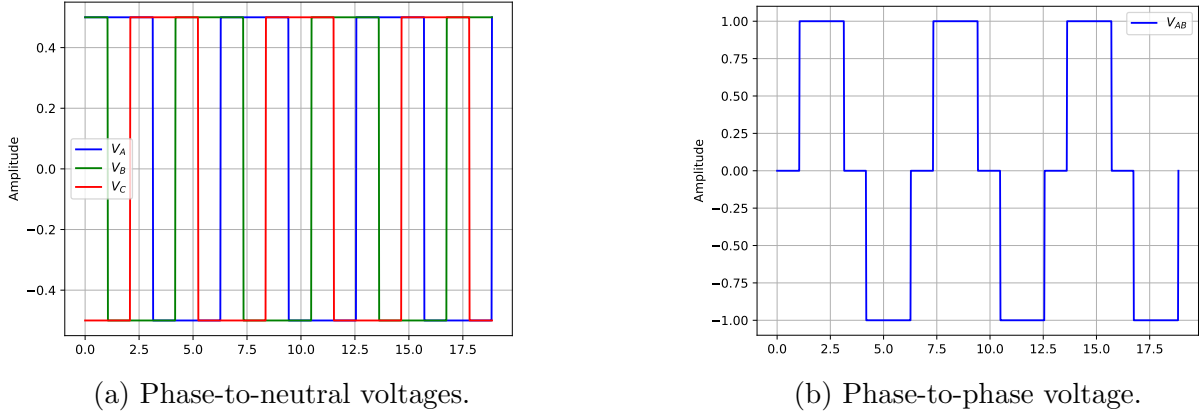


Figure 2.8: Illustration of the output waveforms using the FWM technique with a DC bus voltage of 1V.

The spectrum of the phase-to-phase voltage for a modulating frequency of 800 Hz is shown in Figure 2.9. Compared to the previous techniques, the DC bus utilization ratio is higher ($\lambda = 1.1$). However, the low-order harmonics content is also higher, which explains a higher WTHD of 4.64%. These harmonics are closer to the fundamental, and thus more difficult to filter, which can have an impact on the motor.

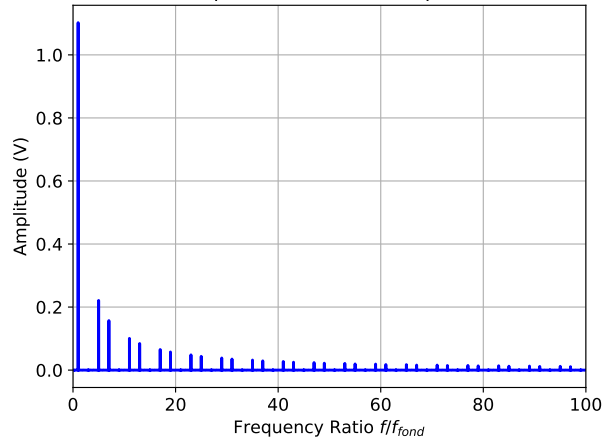


Figure 2.9: Spectrum of the phase-to-phase voltage using the FWM technique with a DC bus voltage of 1V.

Other modulation techniques

Other modulation strategies have been developed to address limitations of the methods presented above.

- **Space Vector Modulation:** this technique represents the three-phase voltages as a single rotating vector in a two-dimensional plane. By controlling the magnitude

and angle of this vector, the inverter outputs are synthesized. Space Vector Modulation achieves better DC bus utilization than SPWM and allows optimized switching sequences that reduce switching losses [14].

- **Calculated Harmonic Elimination:** this method eliminates selected harmonics from the output voltage by computing optimal switching angles. It improves output voltage quality compared to FWM while maintaining a lower switching frequency than SPWM.

2.2 High-speed motor

2.2.1 Motor types

Table 2.2 summarizes and compares several motor types used in FESS applications. In this work, the target motor operates at up to 50 000 rpm in a space environment. Given these requirements, a permanent-magnet machine is the most suitable choice, owing to its high specific power, high efficiency, and capacity to operate at very high rotational speeds.

Features	Induction Motor	Switched Reluctant Motor	Permanent Magnet Motor
Specific Power (kW/kg)	0.7	0.7	1.2
Efficiency (%)	91–94	90	95–97
Maximum Speed (rpm)	900–15,000	>15,000	>30,000

Table 2.2: Comparison of motors typically used in FESS [4].

The two main types of permanent-magnet machines are:

- Permanent Magnet Synchronous Machine (PMSM)
- Brushless Direct Current (BLDC) motor

BLDC machines exhibit a trapezoidal back-EMF waveform, whereas PMSMs have a sinusoidal back-EMF. PMSMs are generally preferred for high-speed applications because they provide a smoother torque than BLDC machines, although they require more complex control [4]. Given that the target application is a high-speed FESS, a PMSM will be considered in this work.

2.2.2 Permanent magnet synchronous motor

The single-phase equivalent circuit of a PMSM is shown in Figure 2.10. R_s denotes the stator series resistance, and $jX_s = j\omega_e L_s$ represents the synchronous reactance, where $\omega_e = p\omega_m$ is the electrical angular frequency, ω_m is the mechanical angular frequency, p is the number of pole pairs, and L_s is the stator synchronous inductance.

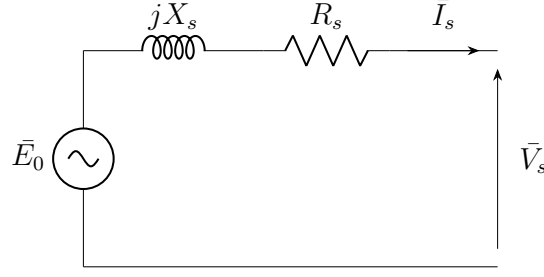


Figure 2.10: Single-phase equivalent circuit of the generator.

In this circuit, $\bar{E}_0$ represents the back-EMF produced by the rotor's rotation. It corresponds to the open-circuit voltage induced in the stator windings. As shown in Equation 2.3, the back-EMF is proportional to the mechanical speed of the motor:

$$E_0 = K\omega_e = \frac{\phi_0}{\sqrt{2}}\omega_e \quad (2.3)$$

where ϕ_0 is the peak value of the flux intercepted by the stator windings. The electrical power transferred by the motor into mechanical power can be expressed as:

$$P = T\omega_m = 3E_0I_s \cos(\psi) \quad (2.4)$$

where T is the torque produced by the motor, I_s is the RMS value of the stator current, and ψ is the angle between the back-EMF and the stator current.

2.2.3 Switching frequency

The electrical angular velocity ω_e is determined by the mechanical angular velocity of the motor and the number of pairs of poles p :

$$\omega_e = p\omega_m \quad (2.5)$$

The corresponding switching frequencies of the inverter, for various modulation techniques and pole-pair configurations, are summarized in Table 2.3. For the SPWM technique, a ratio of $f_{sw}/f_{max} \geq 20$ is considered. This value can be adapted depending on the application, and is usually constant along the entire range of rotational speed. For the FWM technique, the switching frequency is equal to twice the electrical frequency. The indicated values correspond to the maximum mechanical speed of 50 000 Revolutions Per Minute (rpm).

MT \ p	1	2
SPWM	≥ 16.67	≥ 33.33
FWM	0.833	1.67

Table 2.3: Inverter switching frequency in kHz depending on the modulation technique (MT) and the number of pole pairs p for a maximum mechanical speed of 50 000 rpm.

2.3 Power transfer

2.3.1 Power transfer between AC sources

The power transfer between the motor and the inverter can be analyzed using the equivalent circuit shown in Figure 2.11, where E_0 is the back-EMF of the motor, V_{inv} is the inverter output voltage, and jX_s is the stator reactance. The angle δ represents the load angle, which is the phase difference between the back-EMF and the inverter voltage. The stator resistance is neglected in this analysis, as it is typically much smaller than the reactance at high speeds.

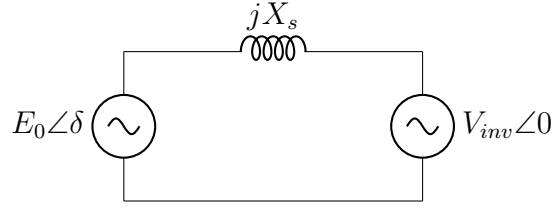


Figure 2.11: Equivalent single-phase circuit for power transfer analysis between the inverter and the motor.

The power transfer between the motor and the inverter can be expressed as:

$$P = 3 \frac{E_0 V_{inv}}{X_s} \sin(\delta) \quad (2.6)$$

$$Q_{motor} = 3 \frac{E_0 (E_0 - V_{inv} \cos(\delta))}{X_s} \quad (2.7)$$

$$Q_{inv} = 3 \frac{V_{inv} (E_0 \cos(\delta) - V_{inv})}{X_s} \quad (2.8)$$

The factor 3 arises from the three-phase nature of the system, with E_0 and V_{inv} being phase-to-neutral RMS voltages [16]. The phasor diagram is represented in Figure 2.12a. Moreover, the total power received can be represented in a circle with a P-Q axis system, as shown in Figure 2.12b. This representation illustrates the impact of V_{inv} and δ on the power exchange, and shows that these are the two main variables to control the motor.

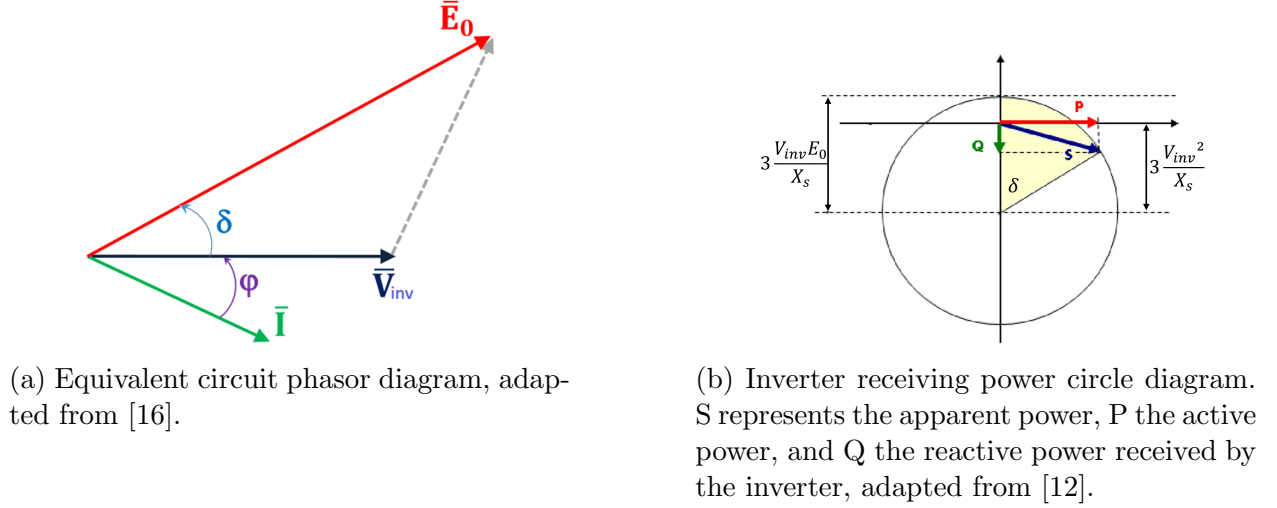


Figure 2.12: Phasor and power circle diagrams for power transfer analysis between the inverter and the motor.

2.3.2 Maximum current estimation

The maximum current flowing from the inverter to the motor is a key input for the loss model developed in Chapter 3. To match the specifications of the FESS (see Table 1.2), the total transmitted power should be of 8 kW. Furthermore, to neutralize the net angular momentum imparted to the spacecraft, at least two flywheels rotating in opposite directions are required. The maximum transmitted power per motor is therefore 4 kW. Since a DoD of 75% is required, the minimum flywheel speed is half of its maximum value according to Equation 1.1. The back-EMF E_0 is therefore also reduced to half of its maximum value (see Equation 2.3). According to the equations developed in Section 2.2.2, the highest current therefore occurs when the flywheel operates at its minimum speed.

Without flux weakening

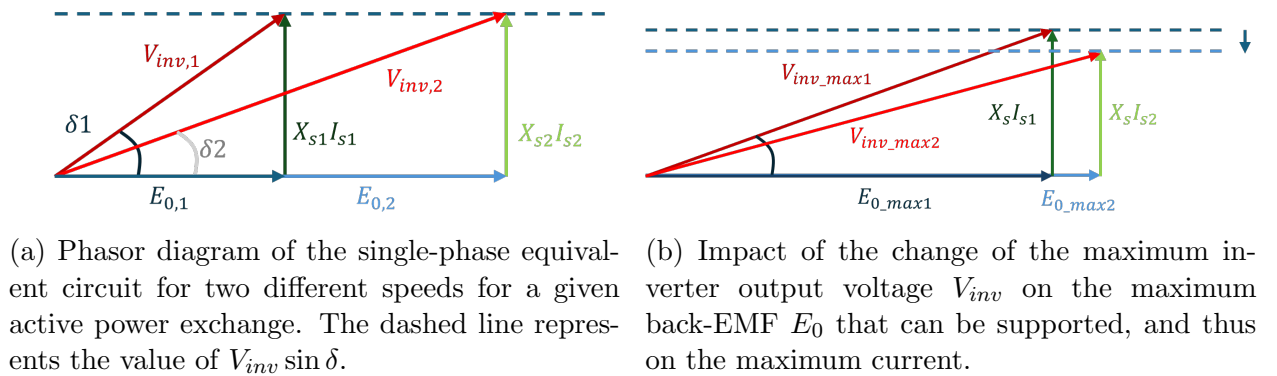


Figure 2.13: Phasor representation of the single-phase equivalent circuit used for the maximum current estimation without flux weakening.

The phasor diagram of the equivalent circuit is represented in Figure 2.13a. This figure represents the situation where power is transferred from the inverter to the motor, in two cases: minimum (1) and maximum (2) speeds for the same active power. Because the stator resistance is neglected in this first analysis, the equations are symmetric: transferring power from the motor to the inverter differs only in the sign of the load angle δ .

According to Equation 2.4, the current is minimized when the stator current phasor is aligned with the back-EMF phasor, i.e., $\psi = 0$. This condition is satisfied in Figure 2.13, where the $jX_s I$ phasor is orthogonal to the back-EMF phasor. Supposing $\psi = 0$ at every speed, the maximum back-EMF, is limited by the inverter maximum output voltage $V_{inv,2}$, in light red in Figure 2.13a. With Equation 2.3, and knowing that $X_s = \omega_e L$, the active power transfer equation can be written as:

$$P = 3 \frac{V_{inv} K p \omega_e}{X_s} \sin(\delta) \quad (2.9)$$

$$= 3 \frac{V_{inv} K p}{L_s} \sin(\delta) \quad (2.10)$$

This means that for a given output power P , the value of $V_{inv} \sin \delta$, represented by the dashed line in Figure 2.13a, is independent of ω_e , and thus constant. The load angle δ (see Equation 2.6) is then determined by the value of the synchronous inductance of the motor. Since $\psi = 0$ at every speed, the maximum value of E_0 (in light blue in Figure 2.13a) that the inverter can support in this condition can be computed, see Figure 2.14b. As shown in Figure 2.13b, increasing the maximum V_{inv} (e.g. by changing the modulation technique) increases the maximum back-EMF, and thus reduces the maximum current. Finally, knowing the value of L_s , a lower bound on the maximum current can be estimated, as shown in Figure 2.14a (for $p = 1$ and $V_{bus} = 70V$).

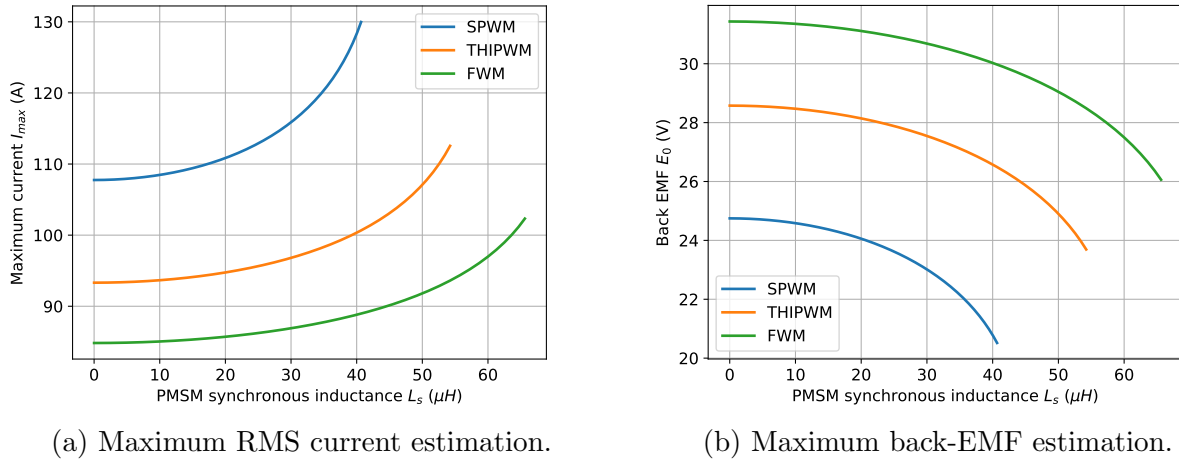


Figure 2.14: Maximum current and back-EMF estimation without flux weakening for a DC bus voltage of 70 V, $p = 1$ and a power of 4 kW.

With flux weakening

If the stator and back-EMF phasors are kept aligned, the maximum current for which the inverter is designed is encountered only at the lowest speed. By using a $\psi \neq 0$, the back-EMF phasor, represented in blue in Figure 2.15a can be increased. This technique is known as

flux weakening. As a result, the maximum current can be further reduced, as illustrated in Figure 2.15b for $p = 1$. The development of the relation between the maximum current and the maximum angle ψ is done in Appendix B. The drawback of this technique is that, at higher speed, the current provided by the inverter is increased. This leads to higher losses in the inverter and in the stator windings, affecting the efficiency.

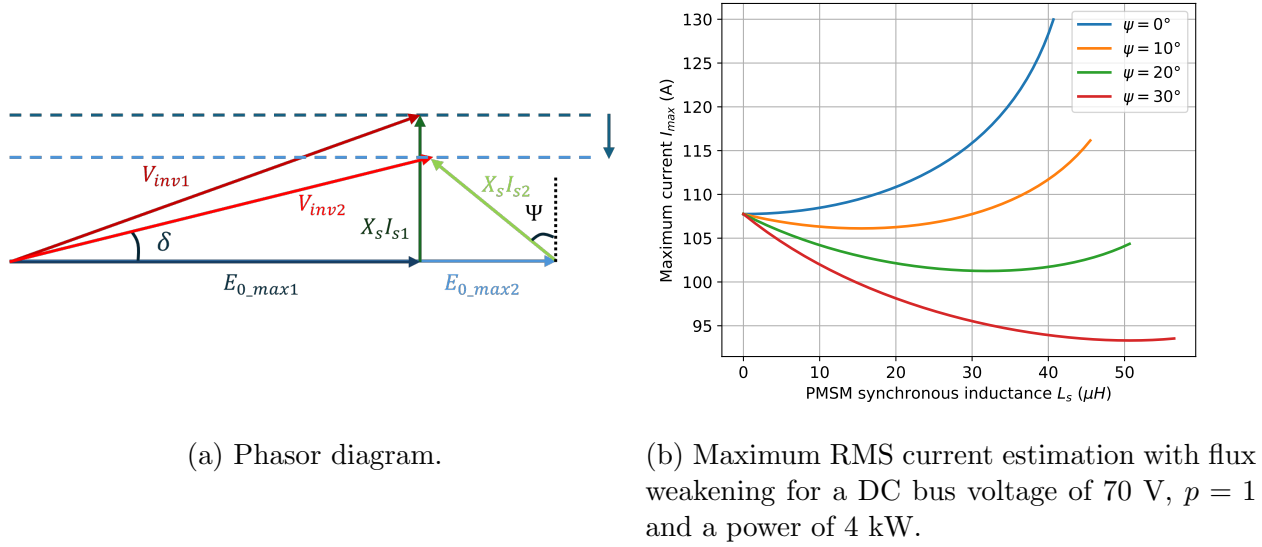


Figure 2.15: Phasor analysis and maximum current estimation under flux weakening.

Summary

The different estimations of the maximum current that will flow from the inverter to the motor are summarized in Figures 2.16 and 2.17 for different bus voltages with SPWM modulation technique and for a 2 and 4 wheels system. This is a lower bound estimation, as it assumes that K and L_s can be designed independently. Moreover, it assumes an ideal control of the motor, and does not take into account the stator resistance and parasitic inductances. In addition, the computations above do not account for transient periods. Strong acceleration or deceleration of the motor may lead to higher current levels. This analysis has also been done for a motor with only one pair of poles. For several pairs of poles, the value of currents would stay similar, but for lower inductances. Finally, these values are RMS values and not peak values. They can be directly used as inputs for the inverter design in the following chapters.

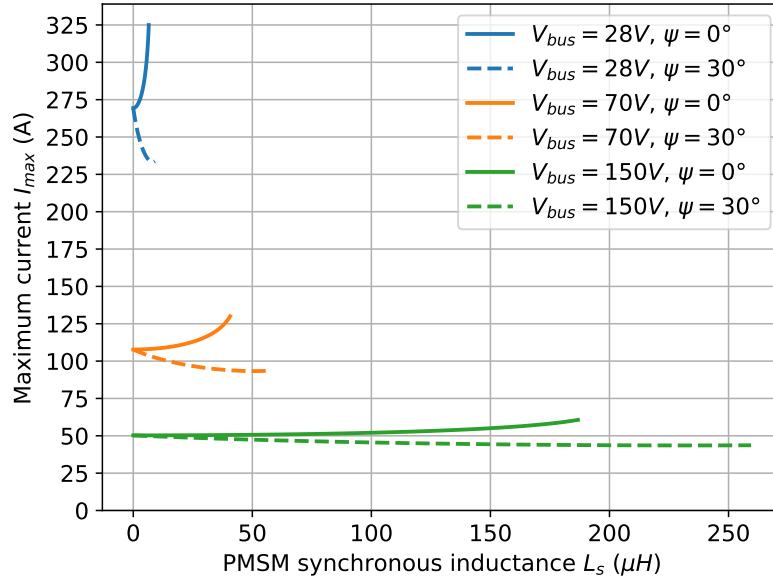


Figure 2.16: Maximum RMS current estimation for different DC bus voltages and flux weakening strategies for $P = 4000$ W (2 wheels system).

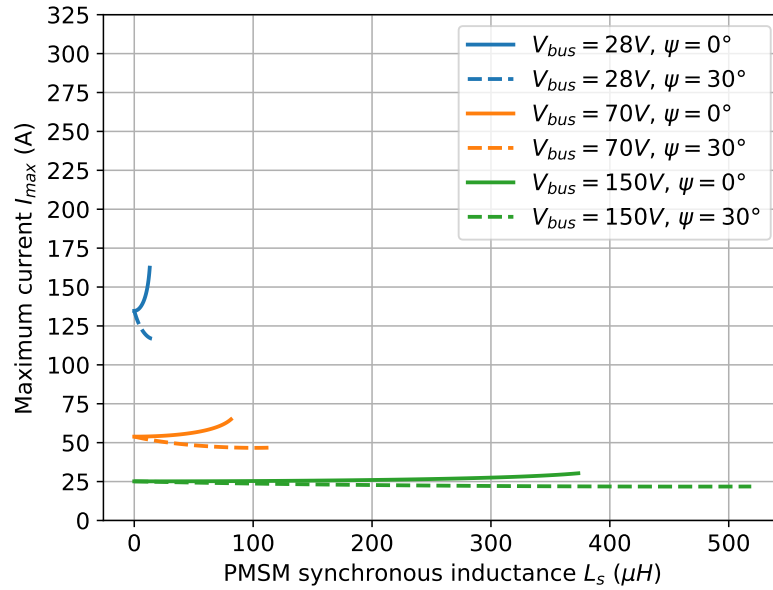


Figure 2.17: Maximum RMS current estimation for different DC bus voltages and flux weakening strategies for $P = 2000$ W (4 wheels system).

It can already be observed that the maximum current is significantly reduced by using a higher bus voltage and by using flux weakening. The maximum value of the synchronous inductance L_s also needs to be carefully monitored while designing the motor. In the next chapters, a focus will be put on the 70 V and 150 V bus voltage cases, with $p = 1$.

3 Power devices and loss modeling

Chapter 2 established that the inverter must operate at switching frequencies above 16.67 kHz (when using the SPWM technique) and supply phase currents that depend strongly on the bus voltage and motor parameters. Tools are now needed to translate those operating conditions into component-level loss estimates.

In this chapter, different families of power switches are reviewed, and a datasheet-based loss model is derived for a single inverter leg. All parameters required by the model are extractable from standard manufacturer datasheets, making it applicable to any Field-Effect Transistor (FET)-based device and directly usable for the technology comparison of Chapter 4.

3.1 Field-Effect Transistors overview

Different types of power electronic switches can be used in the inverter stage of a motor drive. The two most common categories are Insulated Gate Bipolar Transistors (IGBTs) and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). In addition, other types of FETs, such as gallium nitride (GaN) High Electron Mobility Transistors (HEMTs), are increasingly used in power converters. Each type has its own advantages and disadvantages in terms of switching speed, conduction losses, and thermal performance. While IGBTs are typically used for higher current and voltage applications, their switching losses are higher than those of FET-based devices [17]. Therefore, this study focuses on FETs, including both MOSFETs and GaN HEMTs.

3.1.1 MOSFET operating principles

Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are used as switches in power electronics because their switching efficiency is higher than that of other switch technologies [18]. These devices are voltage-controlled: the gate voltage regulates the conductivity of a channel between the source and drain terminals.

Power MOSFETs usually have a vertical structure, as represented in Figure 3.1. Thousands of structures like that are assembled in parallel in commercial MOSFETs. N-MOSFETs (n-doped drain and source) have a lower on-state resistivity than P-MOSFETs (p-doped drain and source), because of the higher mobility of electrons compared to holes. This structure naturally includes a diode (PN junction) between the drain and the source, represented in

red in the figure. This body diode allows reverse current to flow when a negative voltage is applied across the drain and source.

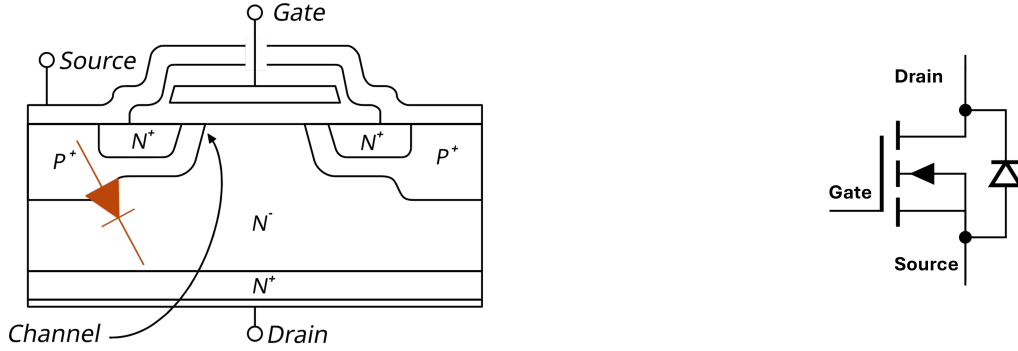


Figure 3.1: Structure and symbol of a MOSFET [18].

When the voltage between the gate and the source is high enough ($V_{gs} > V_{th}$, with V_{th} being the threshold voltage), the relation between the source - drain voltage and the drain current becomes linear, see Figure 3.2. The on-state switch can thus be reduced to a resistor, called $R_{ds,on}$. Several parasitic capacitances, represented in Figure 3.3, influence the dynamics of the switch, and thus the switching losses. These capacitances are typically grouped into three equivalent capacitances: the input, output, and reverse transfer capacitances, denoted C_{iss} , C_{oss} , and C_{rss} , respectively.

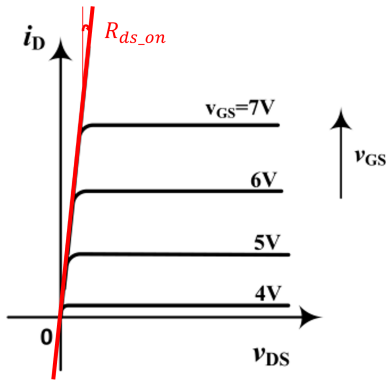


Figure 3.2: Current-voltage characteristics of a MOSFET, adapted from [19].

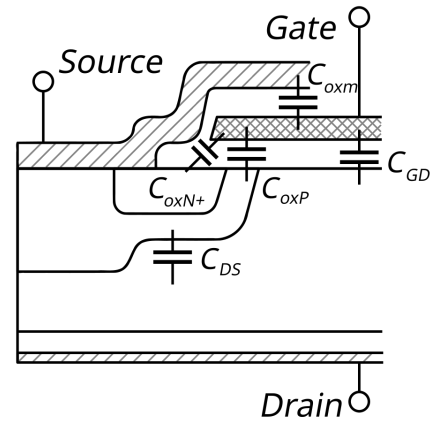


Figure 3.3: Parasitic capacitances of a MOSFET [18].

For Si MOSFETs, the structure can be improved to yield the superjunction MOSFET (SJ-MOSFET). This structure reduces the on-state resistance $R_{ds,on}$ and the switching times, and increases the drain-source breakdown voltage capability [20].

3.1.2 Wide Band Gap FETs

Wide Band Gap (WBG) semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), can be used to improve the performance of power switches. The properties of these materials are summarized in Table 3.1. These WBG materials have a larger breakdown field, allowing for a thinner drift region in the FET structure. This results in a lower on-state resistance $R_{ds,on}$ for the same voltage rating, leading to reduced conduction losses. Additionally, thinner devices have lower parasitic capacitances, which decreases switching losses and enables higher switching frequencies. Furthermore, WBG semiconductors exhibit higher thermal conductivity, allowing for better heat dissipation and operation at elevated temperatures. Finally, the higher electron saturation velocity in WBG materials allows for faster switching speeds, further enhancing efficiency in high-frequency applications [21].

Property	Si	4H - SiC	GaN
Bandgap (eV)	1.12	3.23	3.4
Breakdown field (MV/cm)	0.3	2.5	3.3
Mobility (cm^2/Vs)	1440	950	1400
Thermal conductivity (W/cmK)	1.3	3.7	2.5
Electron saturation velocity ($\times 10^7$ cm/s)	1.0	2.0	2.4

Table 3.1: Material properties of Si, SiC and GaN [22].

While SiC MOSFETs usually have a vertical structure similar to silicon MOSFETs, GaN FETs often utilize a lateral structure built on a silicon substrate, as depicted in Figure 3.4. This kind of switch is called a HEMT. GaN HEMTs are field-effect transistors based on a heterostructure, typically AlGaN/GaN, in which a high-density two-dimensional electron gas (2DEG) forms at the interface due to spontaneous and piezoelectric polarization effects. This 2DEG provides a conduction channel with very high electron mobility and low resistance. The drain current is controlled by the gate voltage, which modulates the electron density in this channel. In contrast to MOSFETs, where the channel is created by inversion under an insulated gate oxide, the channel in a HEMT exists naturally without the need for inversion. This device is thus normally-ON, which is undesirable in power electronics. Enhancement (E)-mode HEMTs, which are normally-off, have thus been developed to address this issue. Several methods are used to deplete the 2DEG channel, ensuring the expected behavior. As a result of this structure, GaN HEMTs have no inherent body diode, unlike Si and SiC MOSFETs [23]. GaN HEMTs are also very resistant to radiation, due to the intrinsic properties of the material, making them particularly suitable for space applications [24].

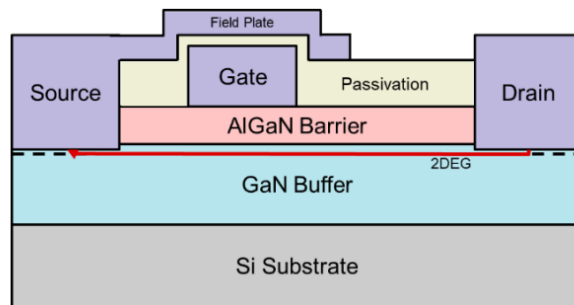


Figure 3.4: Lateral GaN HEMT structure [25].

3.1.3 Technology comparison

The different technologies are used in different applications, as shown in Figure 3.5. Si MOSFETs are preferred for low power applications, while SiC MOSFETs are used for high power devices. GaN FETs are mainly used for very high frequency and low to medium power applications [20].

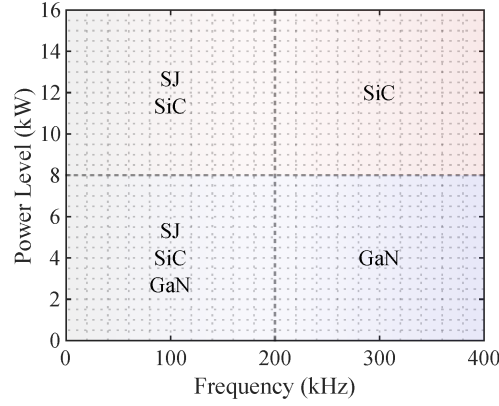


Figure 3.5: Usage domains of different power switch technologies [20].

3.2 Analytical loss model

In this section, the losses occurring in a single inverter leg are analyzed, and a model is developed to estimate them from device characteristics. The model is applicable to all transistor types considered in this study, and is based on datasheet information. The two primary types of losses in power electronic switches are switching losses and conduction losses.

3.2.1 Switching losses

Switching losses occur during the transition of a switch from one state to another. Ideally, when a switch is on, the voltage across it is zero, and when it is off, the current through it is zero. During the switching interval, both voltage and current can be non-zero simultaneously, resulting in overlap losses.

Since the load is primarily inductive due to the motor windings [26], the AC current can be approximated as constant during each switching interval. Four different switching patterns are illustrated in Figures 3.6 and 3.7. In each case, the phase voltage transitions either from V to 0, or from 0 to V . In the graphs, the voltage is represented in orange and the current in blue. The sign of the current and voltage is given by the direction of the arrows. Hence, the current is considered positive when it flows from the inverter to the load, and is denoted in this work as an outgoing current. Furthermore, the current shown in the graphs is the channel current only, and does not include any current flowing through the body diode.



Figure 3.6: Switching pattern for an incoming output current.



Figure 3.7: Switching pattern for an outgoing output current.

During each switching event, one transistor stops while the other starts conducting. To prevent shoot-through, a dead-time is introduced between the turn-off and turn-on of the two transistors. Due to the inductive load, the current is constant and needs to flow through the body diodes of the MOSFETs during this transition period. For this reason, some transistors are turned on with an already null voltage between their source and drain. GaN HEMTs, which have no body diode, must conduct in reverse during these transitions. This is possible even with a zero or negative gate bias. It can be observed that, for each switching situation, only one transistor per inverter leg experiences losses due to the simultaneous switching of voltage and current, called overlap losses. In Figure 3.6, only the bottom transistor undergoes a voltage transition at its terminals while switching. The upper transistor, in contrast, does not experience a direct voltage change because the conduction of the body diode reduces the voltage before the transistor switches. The same reasoning applies to the other three switching patterns. To analyze the switching losses quantitatively, a transistor model, represented in Figure 3.8, including parasitic components is used [26].

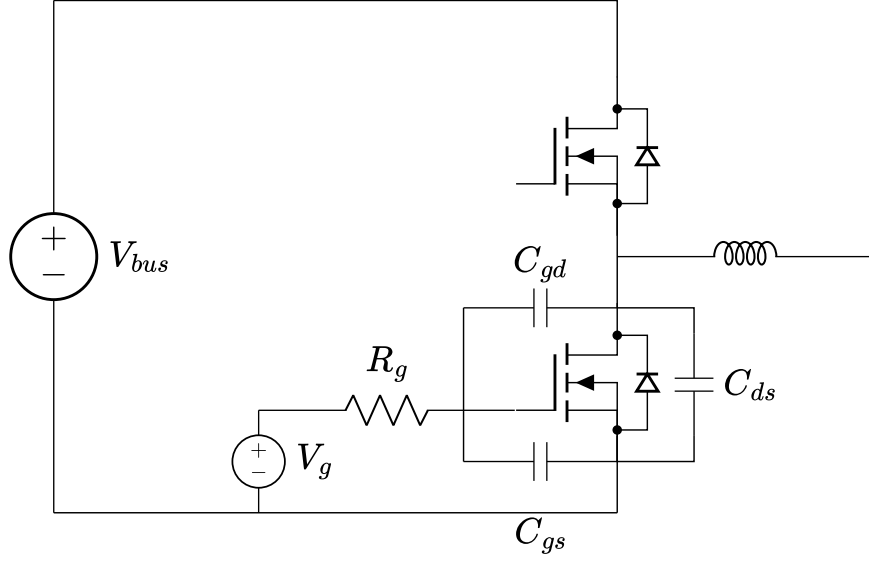


Figure 3.8: Transistor equivalent circuit with parasitic components.

Overlap losses

The turn-on and turn-off waveforms of the top transistor, corresponding to the switching pattern shown in Figure 3.7, are illustrated in Figure 3.9 [27]. The overlap losses are clearly visible in these waveforms, highlighted as P_{ON} . This power depends on the voltage and current levels before and after the switching event, as well as on the rise and fall times of the current and voltage. These times are primarily determined by the parasitic capacitances C_{gd} and C_{gs} , and the gate resistance R_g . The next part of this section presents a method to estimate the overlap losses using typical data provided in datasheets [26, 27, 28].

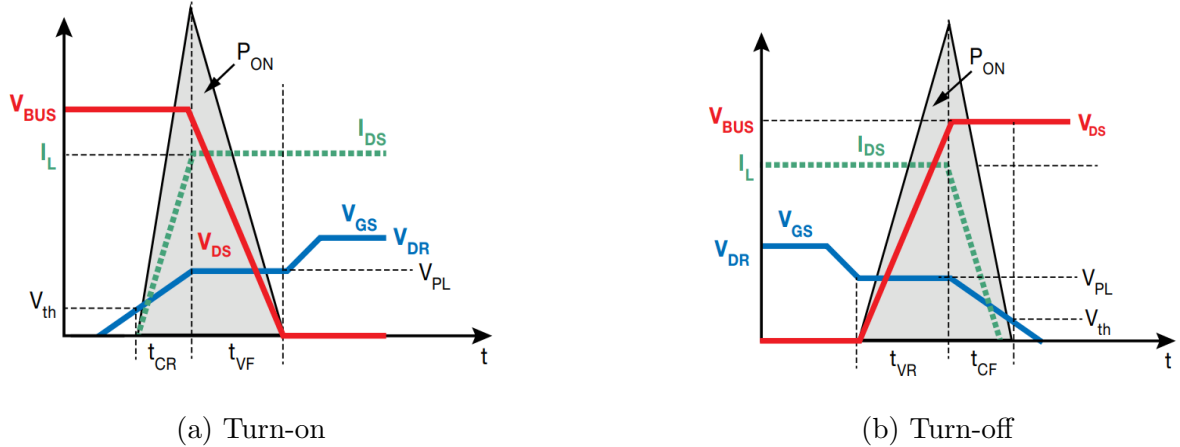


Figure 3.9: Simplified turn-on and turn-off waveforms of a MOSFET [27].

The turn-on switching period can be divided into two intervals: the current rise time t_{cr} and the voltage fall time t_{vf} , as illustrated in Figure 3.9a. Initially, the gate voltage V_{gs} rises from 0 to the transistor threshold voltage V_{th} . The drain current I_{ds} then begins to increase toward its final value. The rise time of the gate voltage depends on the gate resistance R_g

and the input capacitance $C_{iss} = C_{gd} + C_{gs}$. During this interval, the bottom body diode continues to conduct, keeping $V_{ds} = V_{BUS}$. The current rise time t_{cr} is usually provided in the datasheet.

Once I_{ds} reaches the load current I_L , the bottom body diode stops conducting, and the drain voltage begins to fall. At this point, the gate voltage stabilizes at a plateau V_{pl} due to the Miller effect. This effect is the increase in the equivalent capacitance between the input and output of an amplifier, seen from the input [29]. In this situation, the input is the gate, the output the drain and C_{gd} is in between. V_{ds} decreases without any influence of V_{gs} : this can be seen as an infinite gain between the input and the output. As a result, the equivalent capacitance is also infinite, as long as V_{ds} does not reach its final value. This prevents the input voltage V_{gs} from rising further during the decrease of V_{ds} .

The discharge of the drain node occurs through the gate resistance:

$$t_{vf} = V_{BUS} \frac{C_{gd}}{I_g} \quad (3.1)$$

where

$$I_g = \frac{V_g - V_{pl}}{R_g}. \quad (3.2)$$

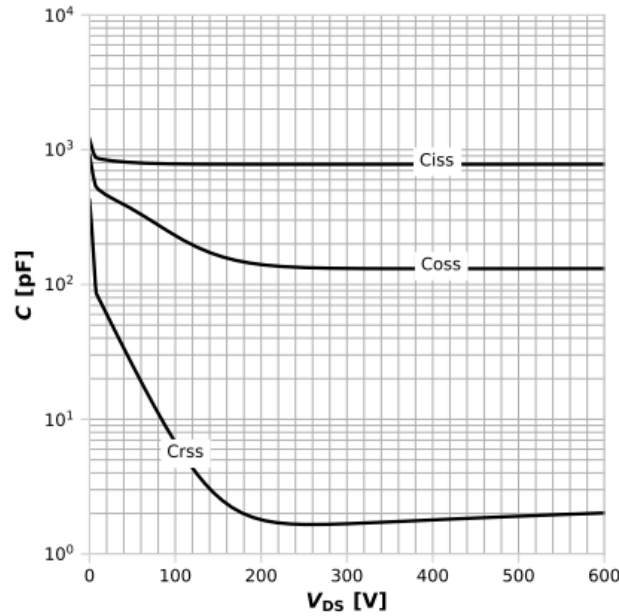


Figure 3.10: Non-linear capacitances of the IGOT65R025D2 GaN HEMT [30]

Directly using Equation 3.1 is often inaccurate due to the strong non-linearity of the reverse transfer capacitance $C_{rss} = C_{gd}$, as shown in Figure 3.10. One practical approach is to select two points on the curve and use an average value:

$$C_{gd,eff} = \begin{cases} C_{gd}(V_{BUS}), & V_{ds} \in [V_{BUS}/2, V_{BUS}], \\ C_{gd}(R_{ds,on}I_L), & \text{otherwise.} \end{cases} \quad (3.3)$$

Thus,

$$t_{vf} = \frac{t_{vf1} + t_{vf2}}{2}, \quad (3.4)$$

with

$$t_{vf1} = V_{BUS} \frac{C_{gd}(V_{BUS})}{I_g}, \quad (3.5)$$

$$t_{vf2} = V_{BUS} \frac{C_{gd}(R_{ds,on} I_L)}{I_g}. \quad (3.6)$$

For the turn-off switching times, t_{vr} and t_{cf} can be determined in the same way. The current fall time t_{cf} is usually provided in the datasheet, and the voltage rise time t_{vr} can be computed similarly to t_{vf} :

$$t_{vr} = \frac{t_{vr1} + t_{vr2}}{2}, \quad (3.7)$$

$$t_{vr1} = V_{BUS} \frac{C_{gd}(V_{BUS})}{I_g}, \quad (3.8)$$

$$t_{vr2} = V_{BUS} \frac{C_{gd}(R_{ds,on} I_L)}{I_g}, \quad (3.9)$$

with $V_g = 0$ during turn-off, giving

$$I_g = \frac{V_{pl}}{R_g}. \quad (3.10)$$

Finally, the overlap losses are computed as

$$E_{on} = \frac{1}{2} V_{BUS} I_L (t_{cr} + t_{vf}), \quad (3.11)$$

$$E_{off} = \frac{1}{2} V_{BUS} I_L (t_{vr} + t_{cf}). \quad (3.12)$$

Output capacitance losses

The charging and discharging of the output capacitance $C_{oss} = C_{ds} + C_{gd}$ also contribute to power losses. Since C_{oss} is nonlinear, as illustrated in Figure 3.10, the energy lost cannot be simply calculated as

$$E_{oss} = \frac{1}{2} C_{oss} V_{BUS}^2. \quad (3.13)$$

Instead, it should be computed as

$$E_{oss} = \int_0^{V_{BUS}} C_{oss}(V_{ds}) V_{ds} dV_{ds}. \quad (3.14)$$

For a symmetrical half-bridge inverter leg, the total switching losses due to the output capacitance can be expressed as [27]:

$$E_{oss} = V_{BUS} Q_{oss}, \quad (3.15)$$

where

$$Q_{oss} = \int_0^{V_{BUS}} C_{oss}(V_{ds}) dV_{ds}. \quad (3.16)$$

Using the two-point method introduced for C_{gd} , C_{oss} can be approximated as:

$$Q_{oss} \approx \frac{C_{oss}(V_{BUS}) + C_{oss}(R_{ds,on}I_L)}{2} V_{BUS}. \quad (3.17)$$

Gate drive losses

Gate drive losses correspond to the energy required to charge and discharge the transistor input capacitance C_{iss} during each switching event. The total energy for an inverter leg can be calculated as:

$$E_{gd} = Q_g V_g, \quad (3.18)$$

where V_g is the gate-source voltage applied to the transistor, and Q_g is the total gate charge needed to switch the device. Q_g is typically provided in the datasheet. This energy is dissipated in the gate resistance R_g as well as in the driver circuitry.

Reverse recovery losses

The reverse recovery losses occur in the body diode of the MOSFET during switching events when the diode transitions from conducting to blocking state. When the diode is turned off, a negative current flows for a short duration due to the stored charge in the diode, see Figure 3.11. This reverse recovery current causes additional losses in the switch. The reverse recovery losses for an inverter leg can be estimated as:

$$E_{rr} = V_{BUS} Q_{rr} \quad (3.19)$$

where Q_{rr} is the reverse recovery charge, typically provided in the datasheet. While GaN HEMTs do not have a body diode and thus do not exhibit reverse recovery losses, Si and SiC MOSFETs do have body diodes, making this loss component relevant for those technologies. To reduce reverse recovery losses, external Schottky diodes are sometimes placed in parallel with the MOSFETs, as their reverse recovery charge is significantly lower than that of the MOSFET body diode.

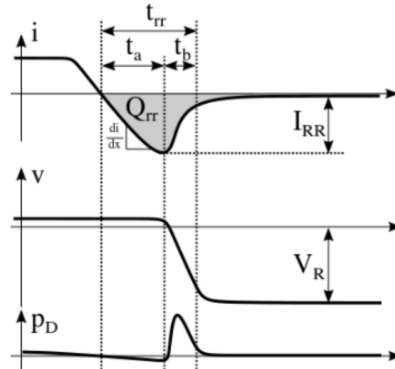


Figure 3.11: Reverse recovery current waveform [31].

3.2.2 Conduction losses

Conduction losses occur when the switch is in the on-state. In this condition, the transistor can be modeled as a resistance $R_{ds,on}$ between drain and source, and the conduction losses of an inverter leg are calculated as:

$$P_{cond} = R_{ds,on} I_{ds}^2. \quad (3.20)$$

3.2.3 Key design parameters

In this section, a loss model for a single inverter leg has been developed and can now be used to compare candidate components. The key parameters required for this comparison, which are typically provided in datasheets, are summarized in Table 3.2. In addition, application-specific parameters, such as load current, bus voltage and switching frequency, are needed to compute the actual losses, and can be estimated from the previous sections.

Loss type	Parameter	Symbol
Overlap losses	Reverse transfer capacitance (at V_{BUS} and $R_{ds,on}I_L$)	C_{rss}
	Gate resistance	R_g
	Current rise and fall time	t_{cr}, t_{cf}
	Miller plateau voltage	V_{pl}
	Gate voltage	V_g
Output capacitance losses	Output capacitance (at V_{BUS} and $R_{ds,on}I_L$)	C_{oss}
Gate drive losses	Gate charge	Q_g
	Gate voltage	V_g
Reverse recovery losses	Reverse recovery charge	Q_{rr}
Conduction losses	On-state resistance	$R_{ds,on}$

Table 3.2: Parameters for inverter leg loss calculation.

4 Component selection

The loss model of Chapter 3 and the current envelope of Chapter 2 together define a quantitative basis for comparing candidate switches. This chapter applies that model to ten devices spanning Si, SiC, and GaN technologies, evaluating their losses as a function of switching frequency and load current under the operating conditions identified earlier. The analysis helps identify a component that is suited to the application, which will be used for all subsequent design work.

The devices considered in this study are listed in Table 4.1. All electrical and thermal parameters used in the loss model (see Table 3.2) were extracted from the corresponding manufacturer datasheets [32, 33, 34, 35, 36, 37, 38, 30, 39, 40]. These devices come from different manufacturers and have different voltage and current ratings, relevant for the targeted application. In this section, blue identifies Si MOSFETs, orange identifies SiC MOSFETs, and green identifies GaN HEMTs. Numbers are also used to identify the devices, according to the order in the table.

	Device	Technology	V_{DS} (V)	I_D (A)	$R_{ds,on}$ (m Ω)	$R_{\theta JC}$ (K/W)
1	BUY15CS23J-01	Si MOSFET	150	23	51	1.66
2	IRHNS9A7264	Si MOSFET	250	82	17	0.50
3	IRHNS67164	Si MOSFET	150	56	18	0.50
4	BUY15CS57A-01	Si MOSFET	150	57	9	0.50
5	E4M0015075J2	SiC MOSFET	750	156	15	0.26
6	AIMDQ75R008M1H	SiC MOSFET	750	173	8	0.02
7	SCT016H120G3AG	SiC MOSFET	1200	112	16	0.02
8	IGOT65R025D2	GaN HEMT	650	61	25	0.68
9	EPC7018DSH	GaN HEMT	100	67	5	2.05
10	EPC7030MSH	GaN HEMT	250	50	15	0.94

Table 4.1: List of the power switches considered.

4.1 Component figure of merit

A common figure of merit for power switches is the output charge Q_{oss} versus the on-state resistance $R_{ds,on}$ [41]. Q_{oss} has an impact on the switching speed of the device, and thus on switching losses, while $R_{ds,on}$ influences conduction losses. A device with low values for both parameters is desirable to minimize overall losses. Both parameters depend on the

channel width : a wider channel reduces the on-state resistance but increases the amount of stored charges. In Figure 4.1, this trade-off is illustrated for the different devices. This allows to make a first comparison and choice depending on the expected switching speed. For example, GaN HEMTs exhibit very low Q_{oss} values, indicating good switching potential.

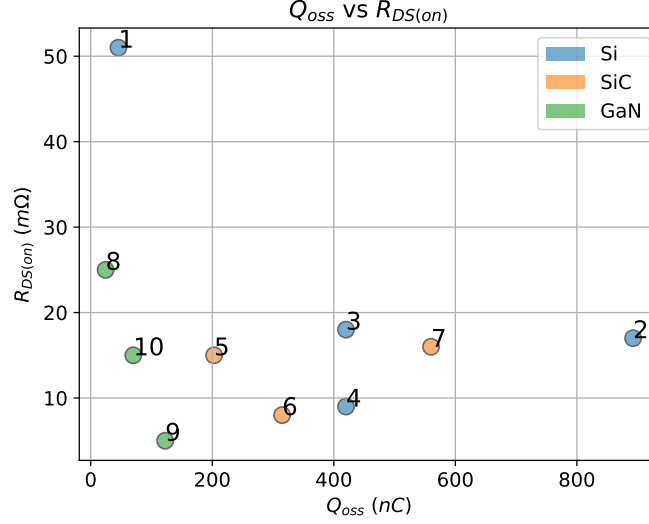


Figure 4.1: Q_{oss} vs. $R_{ds,on}$ trade-off for the candidate components.

4.2 Impact of the switching frequency

Using the model presented in Section 3, a comparison of the losses per transistor depending on the switching frequency has been done, at 2 different junction temperatures, with a 15A RMS current and a 70V bus voltage. The results are presented in Figures 4.2, considering that the devices can be cooled to dissipate this power while keeping a constant junction temperature.

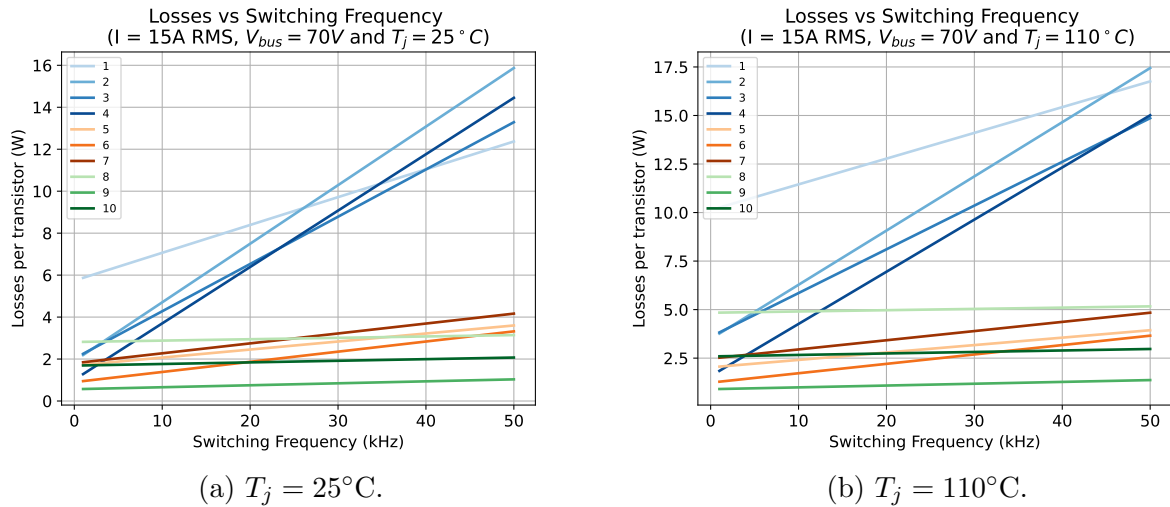


Figure 4.2: Influence of the switching frequency on losses per transistor in an inverter leg.

It can be observed that the power losses increase linearly with the switching frequency. This is because the switching energy does not depend on the frequency. At low switching frequencies, Si MOSFETs performance approaches that of WBG devices because conduction losses, which are similar across technologies, dominate. The difference between the devices becomes more significant at higher switching frequencies, where switching losses dominate. The losses of the GaN HEMTs are almost constant for the considered frequency range, showing their good switching performance. The SiC devices show also a better behavior than the Si devices, with lower losses at high frequency.

The junction temperature has an impact on the on-state resistance, resulting in an increase in the conduction losses. The resistance of the IGOT65R025D2 is for example more than doubled when the junction temperature increases from 25°C to 150°C.

4.3 Impact of the load current

As seen in Section 3, the conduction losses depend on the square of the load current, while the switching losses increase almost linearly with it. As a result, components where the conduction losses dominate will see their losses increase more rapidly with the load current. This is illustrated in Figures 4.3, where the losses per transistor are plotted against the RMS load current, at two different switching frequencies and a junction temperature of 110°C. At a low frequency, the performances of Si MOSFETs are close to WBG MOSFETs because conduction losses have here a more important impact. However, at higher switching frequency, the difference between the technologies is more significant, with WBG devices showing lower losses.

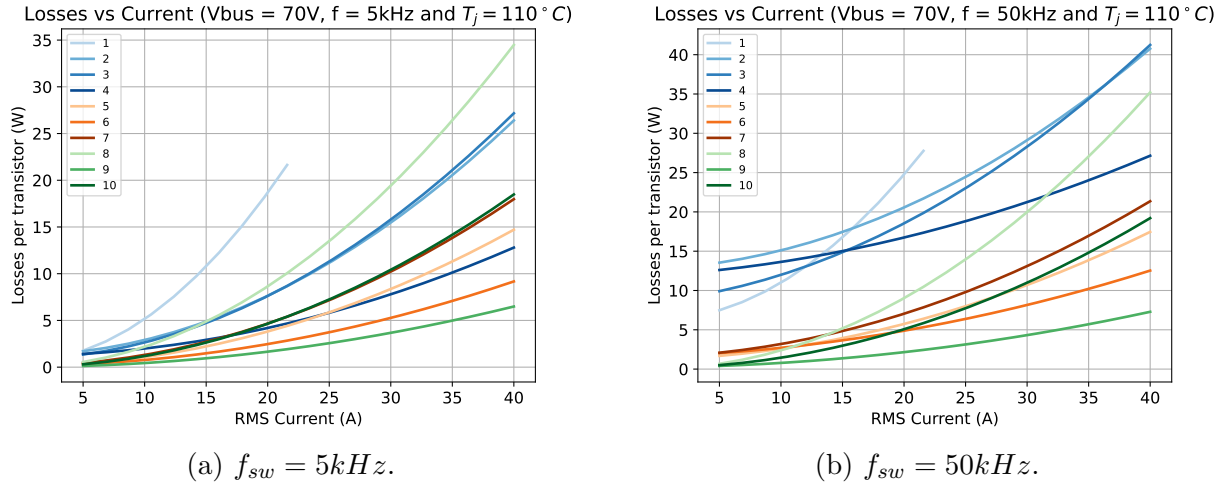


Figure 4.3: Influence of the RMS output current on losses per transistor in an inverter leg.

4.4 Component choice

In this study, the GaN HEMT IGOT65R025D2 represented in Figure 4.4, has been selected. According to Figures 4.2 and 4.3, it exhibits low switching losses, enabling operation across

a wide range of switching frequencies. Si MOSFETs exhibit significantly higher switching losses and are therefore less suitable for high-frequency operation. SiC MOSFETs also perform well, but they are not yet qualified for space missions. They are currently under study to be used in space with a high derating [42]. This explains why high-voltage-rated SiC MOSFETs were included in the study despite the targeted bus voltage being lower. Given this context, a component with existing space qualification was preferred for further development.

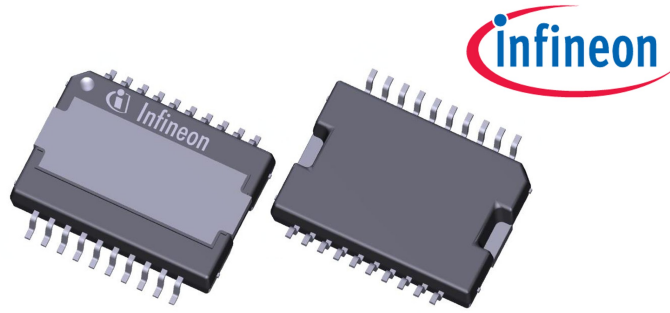


Figure 4.4: Representation of the IGOT65R025D2 GaN HEMT [30].

5 Inverter design

The component selection of Chapter 4 fixes the switch for the remainder of the design: the IGOT65R025D2 GaN HEMT, operating at bus voltages of 70 V and 150 V. This chapter translates these choices into a complete inverter design, covering every subsystem between the DC bus and the motor terminals.

Specifically, this chapter enables the following:

- applying the ECSS derating guidelines to determine the maximum allowable electrical and thermal stress on the selected transistor.
- designing the gate drive circuit and verifying its correct operation through LTspice waveform analysis.
- sizing the input filter to comply with ECSS conducted-emission requirements for the chosen switching frequency.
- estimating the junction temperature and maximum power dissipation under space thermal constraints.
- estimating the conduction and switching losses as a function of switching frequency and bus voltage, and determining the number of transistors in parallel required to remain within the thermal budget.

The loss estimation derived here serves as the reference against which the experimental measurements of Chapter 6 will be compared.

5.1 Space environment constraints

As discussed in Section 1.2, spacecraft are exposed to high levels of radiation in space. To "extend component life, increase reliability and enhance the end-of-life performance of equipment" [43], the ECSS recommends applying a derating to electronic components used in space applications. Derating consists in operating a component below its maximum rated stress levels (voltage, current, power, or temperature). The rationale is to reduce the overlap region between the stress and strength distributions (see Figure 5.1) by shifting the stress distribution to lower values.

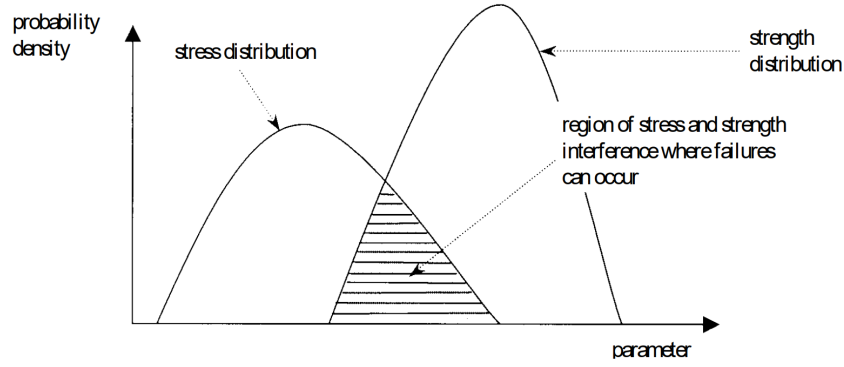


Figure 5.1: Parameter stress versus strength relationship [43].

Each component type has specific derating guidelines defined by the ECSS, as summarized in Table 5.1 for transistors [43].

Parameter	Load ratio or limit
Drain to source voltage V_{DS}	80% of rated
Gate to source voltage V_{GS}	75% of rated
Drain current I_{DS}	75% of rated
Power dissipation P_D	65% of rated
Junction temperature T_J	110 °C or $T_{j,max} - 40$ °C (whichever is lower)

Table 5.1: Derating guidelines for transistors [43].

5.2 Gate drivers

5.2.1 Circuit description

The gate driver provides the necessary voltage and current to switch on and off the transistors in the inverter. For the chosen component, a RC interface is recommended [44], as shown in Figure 5.2. Unlike a regular MOSFET, this transistor has an ohmic gate contact, and is called a gate injection transistor (GIT). As a consequence, the transistor can be represented with a diode between the gate and source, and the I_g/V_{gs} curve is similar to a diode IV curve, see Figure 5.3.

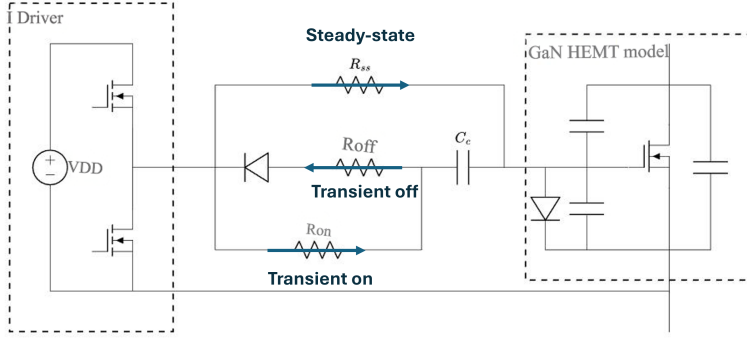


Figure 5.2: Gate driver schematic.

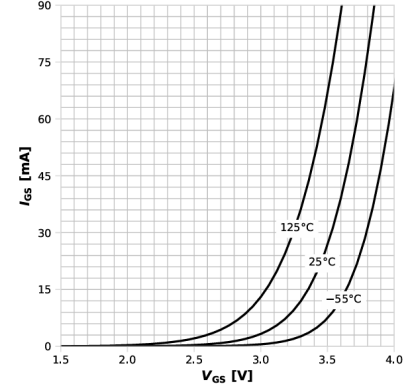


Figure 5.3: Gate current versus gate voltage curve for the IGOT65R025D2[30].

The transistor needs a constant small on-current in steady state to keep the channel open, and a large current during switching to increase the switching speed, as represented in Figure 5.4. Two current paths are provided. The first is a low-resistance path through C_c (controlled by R_{on} and R_{off}) that supplies the large transient current during switching. Once the capacitance is charged, a smaller current flows through a higher resistance path (R_{ss}). The charged capacitance also provides a negative voltage to the gate during turn-off. This reduces the risk of false turn-on due to voltage spikes or noise, and thus increases the reliability of the system.

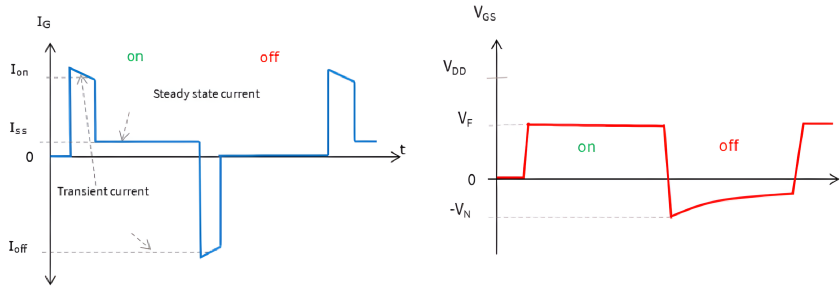


Figure 5.4: Schematic of gate driver waveforms, adapted from [44].

5.2.2 Parameter tuning

In this driver interface, the parameters C_c , R_{ss} , R_{on} and R_{off} need to be tuned.

First, the minimum voltage during off-state (V_N) is given by [44]:

$$V_N = \frac{C_c(V_{DD} - V_F) - Q_{G,tot}}{C_c + C_{gs}} \quad (5.1)$$

There is a trade-off in selecting V_N . A more negative V_N reduces the risk of false turn-on, thereby increasing reliability, but it also increases losses during dead times, when the transistor is off yet still conducting in reverse due to the inductive load. This value should be

between -3 V and -5 V. To ensure a negative voltage, the total charge stored in the coupling capacitor C_c must be higher than the total gate charge $Q_{G,tot}$, according to Equation 5.1. It is thus recommended to choose $C_c \approx (2 - 3) \frac{Q_{G,tot}}{V_{DD} - V_F}$, with V_F the forward voltage of the diode between gate and source. A typical value for V_{DD} is between 8 and 12 V [44].

When the transistor is on, it must be biased by a small steady-state current. The maximal current is given in the datasheet [30], and applying a derating factor of 75% to the gate current, the maximum allowable value is approximately 34.5 mA. The value of R_{ss} can be calculated as:

$$R_{ss} = \frac{V_{DD} - V_F}{I_{G,on}} \quad (5.2)$$

Finally, the values of R_{on} and R_{off} can be tuned to adjust the switching speed. A faster switching reduces the switching energy, but increase the risk of inductive overvoltages. Typical values are around 2.2 Ω for R_{off} , and between 6.8 and 27 Ω for R_{on} , for $V_{DD} = 10V$ [44]. To ensure good reliability, $R_{on} = 27\Omega$ and $R_{off} = 2.2\Omega$ are selected. The final values of the parameters are summarized in Table 5.2.

Parameter	Value
V_{DD}	10 V
C_c	5 nF
V_N	-4.5 V
R_{ss}	200 Ω
R_{on}	27 Ω
R_{off}	2.2 Ω

Table 5.2: Gate driver parameters.

5.2.3 LTspice simulation and waveform analysis

Simulations of the gate drive circuit were performed in LTspice, with an equivalent circuit represented in Figure 5.5. The IGOT65R025D2 transistor simulation model is the one provided by Infineon. For high-frequency converters, parasitic inductances can significantly affect the performance. These inductances are caused by the conductors (and especially loops) in the circuit and will oppose the rapid change of current during switching, causing voltage spikes. This can lead to increased switching losses and potential damage to the transistor. To be closer to the reality, two parasitic elements have been added to the circuit: a gate loop inductance of 2.5 nH, and a power loop inductance of 5 nH [45].

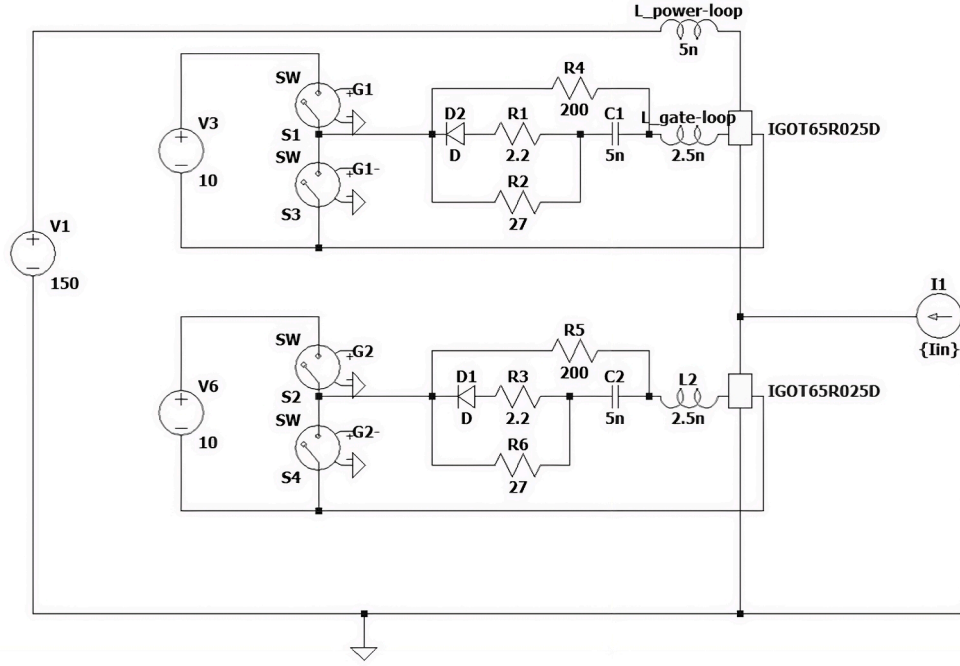


Figure 5.5: LTspice schematic used for the simulation of the single-leg inverter.

The resulting waveforms for a 150V DC supply, a 10A incoming (from load to inverter) current and a 50 ns dead-time are shown in Figures 5.6 and 5.8, and are analyzed below. The parameters used are those given in Table 5.2. The waveforms for an outgoing (from inverter to load) current are shown in Appendix A. In the next figures, the current is signed as positive when it flows into the transistor.

High-to-low transition analysis

The high-to-low transition (output voltage going from V_{BUS} to 0V) is shown in Figure 5.6. First, the gate voltage of the top transistor (shown in blue in the upper panel) decreases, and a dead time is applied during which both transistors are off. The negative voltage that can be observed during the dead time is due to the coupling capacitor C_c , which provides a negative voltage to the gate of the transistor turning off.

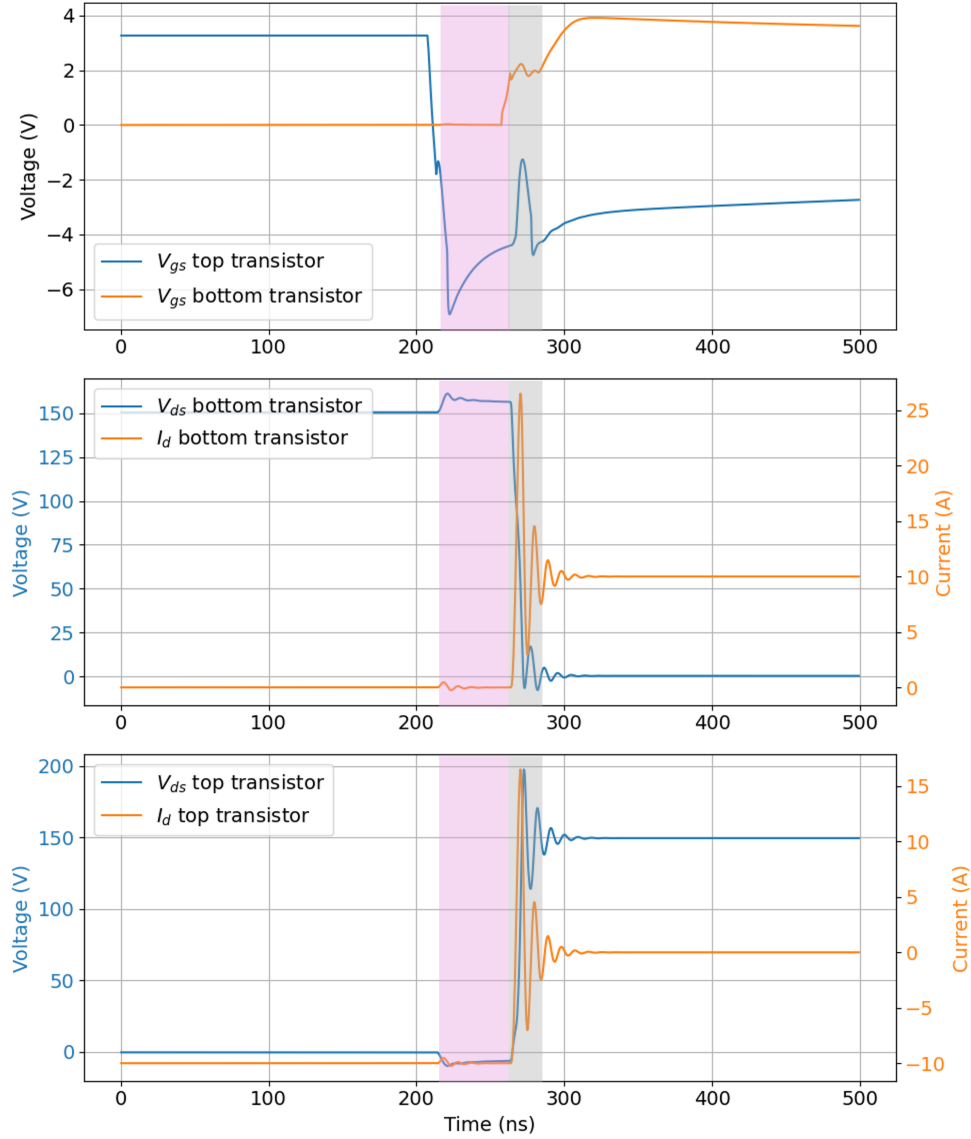


Figure 5.6: Simulated waveforms during high-to-low transition, 10 A incoming current, $V_{BUS} = 150V$ and a dead time of 50 ns.

When V_{gs} reaches a negative voltage (pink area), the top transistor keeps conducting in reverse due to the constant load current. As a result, the output voltage (V_{ds} of the bottom transistor) rises. This is because, to conduct in reverse, the transistor requires a drain-to-gate voltage above the threshold voltage. Hence, the source voltage is increased, accordingly to the curves given in Figure 5.7. This offset can also be seen in the V_{ds} of the top transistor in the last figure.

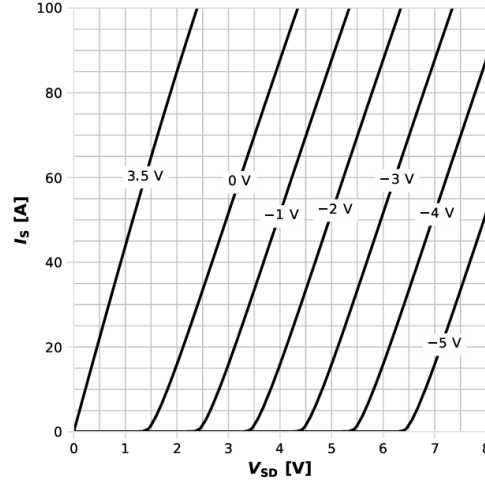


Figure 5.7: Current versus voltage curve of the transistor, for different V_{gs} values [30].

Then, the bottom transistor is turned on and its gate voltage rises. Two phenomena are observable during this transition (gray areas). First, the gate voltage of the bottom transistor (shown in orange in the upper panel) exhibits a plateau, analogous to the Miller plateau in a MOSFET. Second, the gate voltage of the top transistor makes a peak, which is due to the parasitic drain to gate capacitance C_{gd} . When the output voltage falls from V_{BUS} to 0 V, the gate voltage (referenced to the source) decreases, requiring a large current to discharge C_{gd} . The parasitic inductance of the gate loop opposes this rapid current change, causing a voltage spike. This effect can be severe because it may cause false turn-on of the transistor, producing a shoot-through current that damages the system. This is one of the reasons why a negative voltage during off-state is recommended, as it will reduce the risk of false turn-on by increasing the margin between the gate voltage and the threshold voltage.

Finally, a high overshoot in current can be observed. This can be explained by the charging and discharging of the parasitic output capacitances of the transistors C_{oss} . When V_{ds} of the top transistor goes from 0 V to V_{BUS} , a high current is needed to charge its output capacitance. This current is going in the opposite direction of the load current, and thus flows through the channel of the bottom transistor causing this high overshoot. Oscillations of several MHz are also observable after the switching transition, caused by the interaction between parasitic inductances and capacitances. These oscillations contribute to additional losses and potential device damage, and should therefore be minimized by reducing parasitic elements in the Printed Circuit Board (PCB) layout [45].

Low-to-high transition analysis

The low-to-high transition (output voltage going from 0 V to V_{BUS}) is shown in Figure 5.8. First, the bottom transistor is turned off. Its V_{gs} decreases of around 10V, which is the voltage across the coupling capacitor C_c , and becomes thus negative.

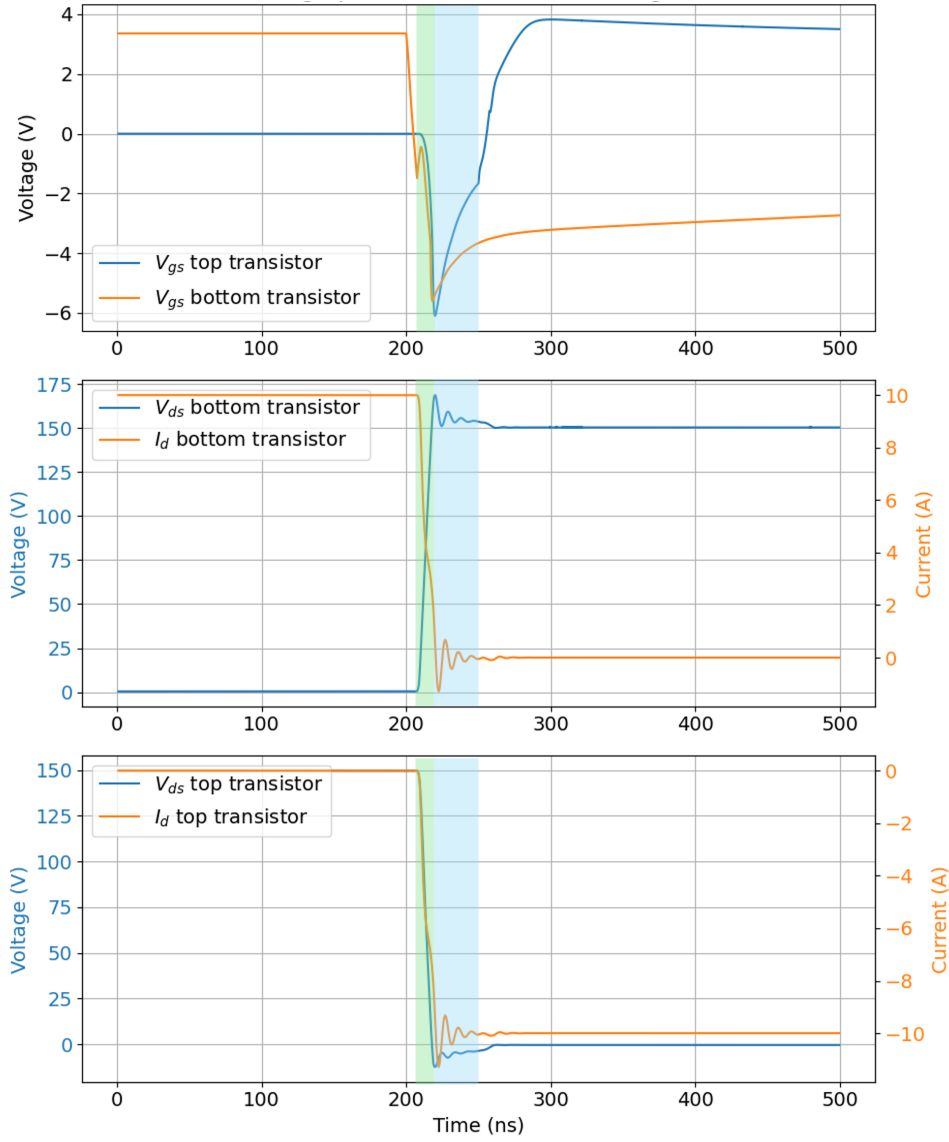


Figure 5.8: Simulated waveforms during low-to-high transition, 10 A incoming current, $V_{BUS} = 150V$ and a dead time of 50 ns.

Once V_{gs} of the bottom transistor reaches a negative voltage (green area), the top transistor starts conducting in reverse. As a result, the output voltage (V_{ds} of the bottom transistor) goes down. As for the previous situation, C_{gd} of the top transistor needs to be discharged, and the parasitic inductance of the gate loop causes a voltage spike on its gate. Nevertheless, this is not as critical as previously, because it can not cause a change in the state of the transistor.

Just after the current rise, a voltage overshoot appears due to the power loop inductance. As shown in the blue shaded region, a further overvoltage is observable during the reverse conduction of the top transistor.

It can also be observed that the overshoot in current is less pronounced than before. This is because, this time, the upper C_{oss} can be discharged through the channel of the top transistor, while the bottom C_{oss} is charged by the load current. The inrush current observed before is thus not present anymore.

5.2.4 Bootstrapping

Both transistors need to be supplied by a voltage between their source and their gate. For the bottom transistor, this voltage is easily provided since the source is connected to ground. For the top transistor, however, the source voltage is not fixed; a floating supply is therefore required. This floating voltage can be provided by a flyback converter, but this means using another power electronic circuit. A simpler solution is to use a bootstrapping circuit, which uses the switching of the transistor to charge a capacitor and provide the necessary voltage. The principle of bootstrapping is illustrated in Figure 5.9. During the low state, the capacitor C_{boot} is charged through the diode by the supply voltage V_{DD} (see Figure 5.9a). During the high state, the energy stored in the capacitor can be used to drive the upper transistor (see Figure 5.9b). The floating voltage is thus provided by the capacitor, which is charged during the off-state of the upper transistor.

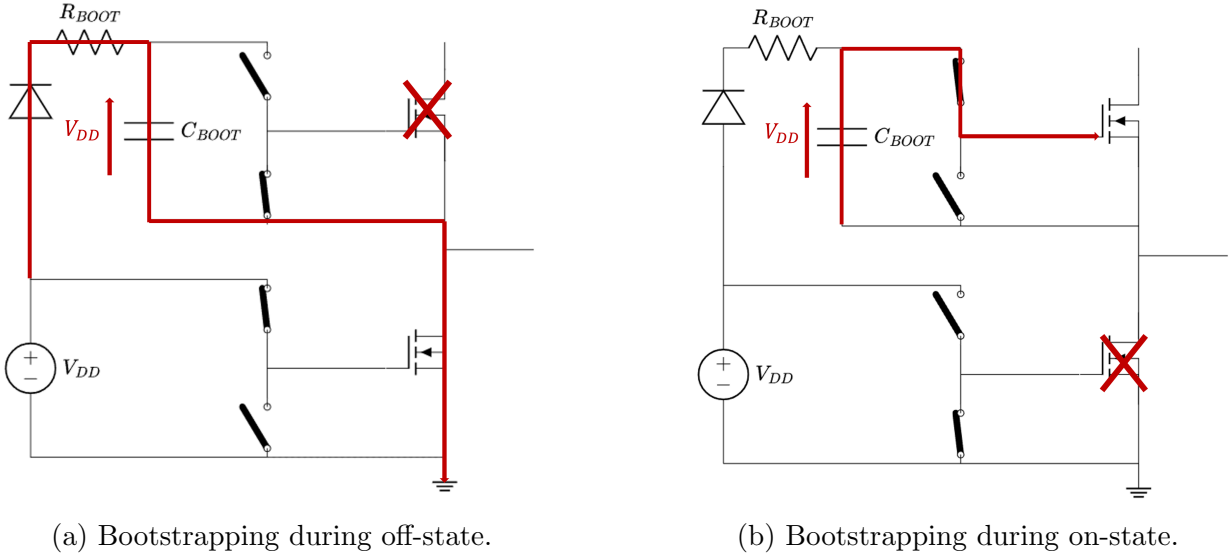


Figure 5.9: Bootstrapping circuit operating principle.

The voltage across the capacitor should not decrease by more than 10% during the on-state [46]. Knowing the maximum average current that the transistor can draw through the gate, the minimum value of the capacitor can be calculated depending on the switching frequency f , the maximum duty cycle D and the supply voltage V_{DD} .

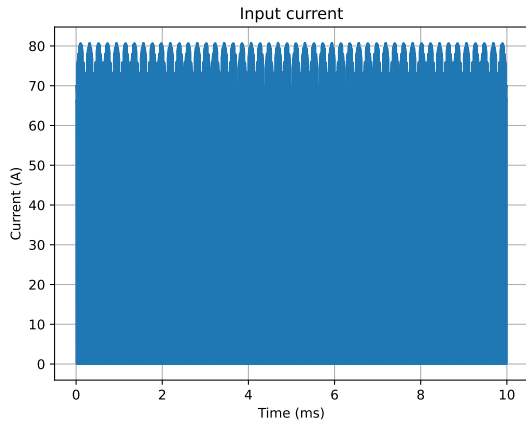
$$\begin{aligned}
 I &= C_{boot} \frac{dV}{dt} \\
 \Leftrightarrow \Delta V &= \frac{1}{C_{boot}} \int I dt \\
 \Leftrightarrow C_{boot} &= \frac{I_{avg} \cdot D}{f \cdot V_{DD} \cdot 0.1}
 \end{aligned}$$

The bootstrapping resistance R_{boot} has an impact on the speed of charging of the capacitor. Its role is to limit the inrush current when the capacitor is charging, and thus protect the supply and the diode. However, a too large resistance will increase the time required to charge the capacitor [46]. The peak current can be estimated as $I_{peak} = \frac{V_{DD} - V_{f,diode}}{R_{boot}}$. For a

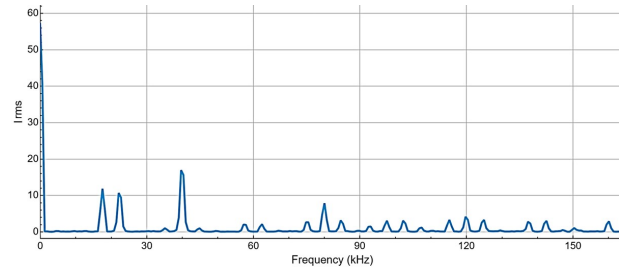
supply voltage of 10 V and a maximum peak current of 1 A, the bootstrapping resistance should be around $10\ \Omega$, which is a typical value for this parameter [47].

5.3 Input filter

Because of the high switching frequency of the inverter, the input current (supposed to be a DC current) is highly distorted. The input current of a three-phase inverter without any filtering in time domain and its spectrum are shown in Figure 5.10. In this situation, an input current of $I = \frac{4kW}{70V} = 57A$ has been taken (situation with $V_{BUS} = 70V$ and 2 wheels). The switching frequency is set to 20 kHz, which corresponds roughly to the minimum switching frequency required for a SPWM, as presented in Section 2.2.3. However, the filter can be adapted to other current and switching frequency levels by following the same design process.



(a) Time domain.



(b) Frequency spectrum.

Figure 5.10: Input current of a three-phase inverter without input filter ($V_{BUS} = 70V$, $I = 57\text{ A}$, 20 kHz switching frequency).

Unlike terrestrial power grids, conducted emissions are not regulated in space; requirements are instead mission-specific. However, the ECSS produced recommendations concerning maximum levels of conducted disturbance, as shown in Figure 5.11 [48]. The highest peak in the spectrum of the input current occurs at around 40 kHz, with an RMS value of approximately 16.89 A. According to the ECSS recommendations, the maximum allowable conducted disturbance at this frequency is approximately $85\text{ dB}\mu\text{A}$, corresponding to a current of approximately 18 mA. The input filter must therefore attenuate the current at 40 kHz by approximately 60 dB.

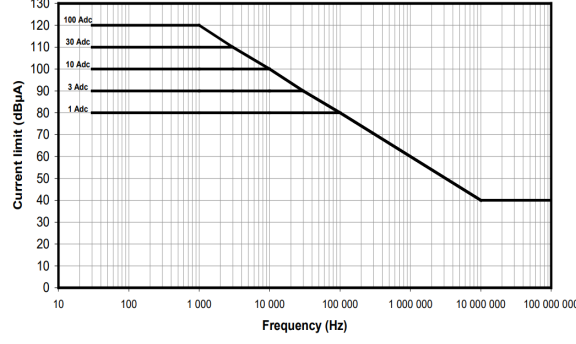


Figure 5.11: Recommended maximum levels of conducted disturbance for space applications [48]

An LC filter (Figure 5.12) is selected to attenuate the disturbances. This filter has a cut-off frequency of $f_c = \frac{1}{2\pi\sqrt{LC}}$ and provides 40 dB/decade of attenuation above it [49]. For a required attenuation of approximately 60 dB, the cut-off frequency is $f_c \approx 1.25$ kHz.

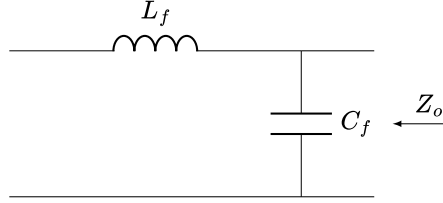
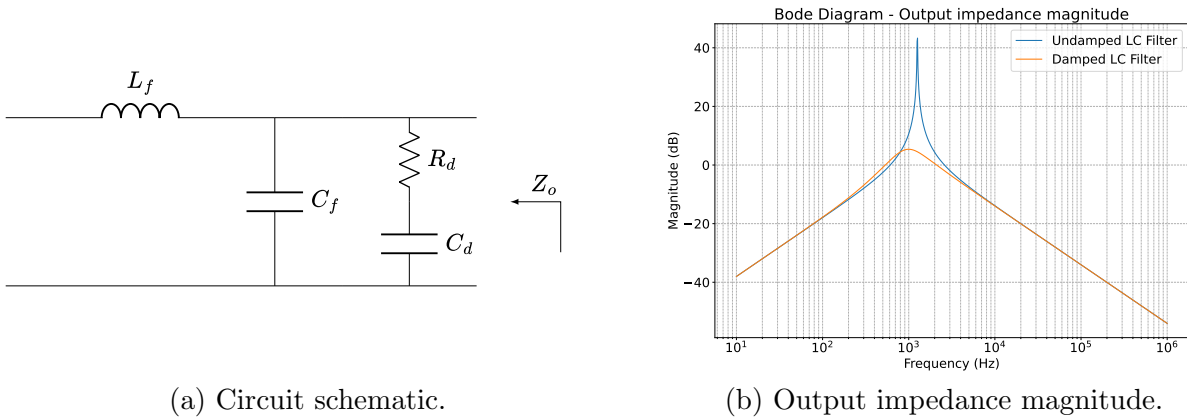


Figure 5.12: LC low-pass filter

The output impedance Z_O can be seen as the parallelization of an inductor and a capacitor. As shown in Figure 5.13b, the impedance of the filter is high at the cut-off frequency, which can be source of instability. To reduce this effect, a damping resistor can be added in parallel with the inductor, as shown in Figure 5.13a, allowing a low inductance path for the current at the cut-off frequency. Its value is given by $R_d = \sqrt{\frac{L_f}{C_f}}$ [49]. A capacitor is also added in series with the resistance to reduce DC losses. The damping capacitor should be high enough to not impact the performance of the filter, but not so high as to significantly increase the size of the components on the PCB. A good trade-off is $C_d = 3 \times C_f$ [12].



(a) Circuit schematic.

(b) Output impedance magnitude.

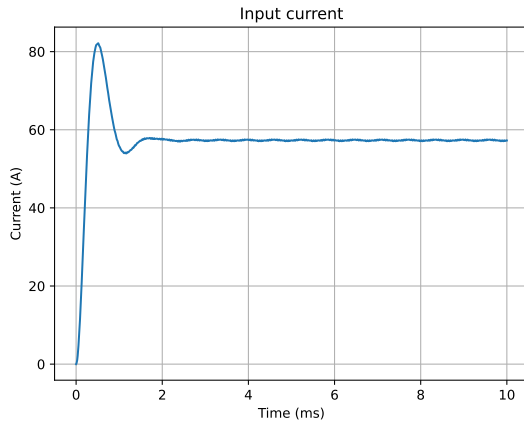
Figure 5.13: Damped LC filter.

The filter has been implemented with the following values:

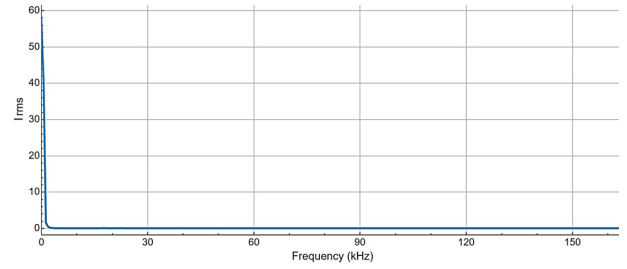
Parameter	Value
L_f	$200 \mu H$
C_f	$80 \mu F$
R_d	1.6Ω
C_d	$240 \mu F$

Table 5.3: LC filter parameters.

The result of the simulation of the input current with the implemented filter is shown in Figure 5.14. The peak at 40 kHz has been reduced from 16.89 to 16 mA, respecting the recommendation and showing the effectiveness of the filter. This filter can be adapted to other switching frequencies by adjusting the cut-off frequency and the damping resistor accordingly.



(a) Input current with filter.



(b) Spectrum of the input current with filter.

Figure 5.14: Input current of a three-phase inverter with an input filter ($V_{BUS} = 70V$, $I = 57 A$, 20 kHz switching frequency).

5.4 Thermal management

The selected transistor is a top-cooled transistor, which means that the heat is dissipated through the top of the component. The heat transfer in this type of transistor is illustrated in Figure 5.15. The heat is transferred from the junction to the case, and then from the case to the sink through a Thermal Interface Material (TIM). This material improves the thermal coupling between the heat-producing component and the heat sink [50]. Then, the heat is radiated from the sink to the environment.

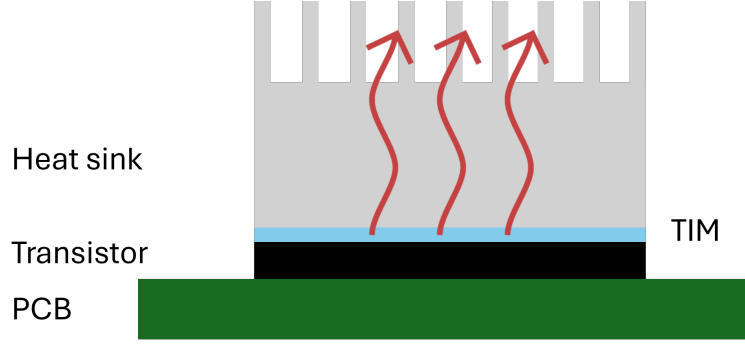


Figure 5.15: Heat transfer in a top-cooled transistor.

The junction temperature can be estimated using the thermal equivalent circuit shown in Figure 5.16. The junction temperature T_J is given by:

$$T_J = T_{surface} + P_D \cdot (R_{junction_to_case} + R_{interface} + R_{sink}) \quad (5.3)$$

with P_D the power dissipated by the transistor.

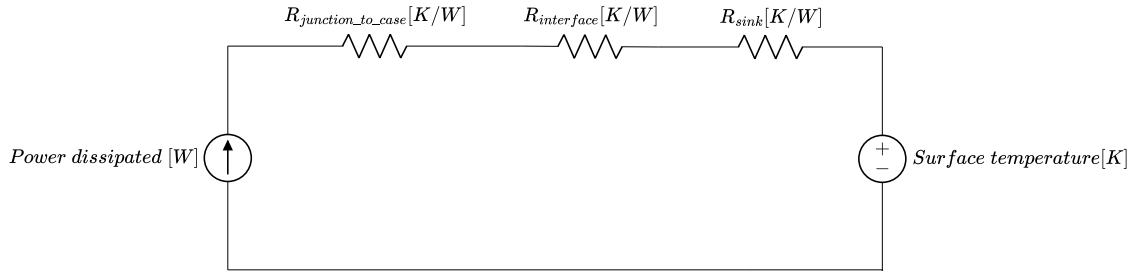


Figure 5.16: Thermal equivalent circuit.

According to Table 5.1 and the component datasheet [30], the junction temperature of the transistors should not exceed 110 °C. Furthermore, electronic components used in space must withstand environmental temperatures of up to approximately 70°C [51]; the surface temperature of the sink can be set to this value. The different thermal resistances can be estimated as follows:

- The junction to case thermal resistance is given in the datasheet of the component, here $R_{junction_to_case} = 0.68 K/W$ [30].
- The thermal resistance of the TIM can be estimated as $R_{interface} = \frac{t}{k \cdot A}$, with t the thickness of the TIM, k its thermal conductivity and A the area of contact between the transistor and the sink. The area of contact is around 180 mm² for the selected transistor. The thickness of the TIM as well as its thermal conductivity depend on the chosen technology. For the experimentation presented in Chapter 6, the TIM is compressed at 1.5 mm and has a thermal conductivity around 5 W/(m · K). Thus, $R_{interface} = 1.7 K/W$.
- The thermal resistance of the sink depends on its geometry. For this prototype presented in Chapter 6, a heat sink with $R_{sink} = 0.9 K/W$ is chosen. The two transistors share

the same heat sink; therefore, the effective thermal resistance seen by each transistor (as represented in the thermal equivalent circuit) is twice this value. In space, convective cooling is unavailable: only radiation dissipates heat, and the thermal resistance of the sink will therefore be higher than in laboratory conditions.

As a result, the global thermal resistance of the prototype on Earth is around 4.2 K/W . Considering this value and the conditions mentioned before, the maximum power that a transistor can dissipate in space is around 9.5 W . The total power dissipation allowed for the leg is thus around 19 W . Note that the thermal resistance of the sink will need to be reevaluated to take into account the absence of convective cooling in space. In the lab, considering an ambient temperature of 25°C , and a maximal junction temperature of 150°C , the maximum power that a transistor can dissipate is around 30 W . This means a maximal power dissipation of around 60 W for the whole prototype.

5.5 Loss estimation

LTspice simulations have been performed with the equivalent circuit presented in Section 5.2.3 (Figure 5.5). To simulate the full load situation, the junction temperature of the transistor is set to the maximum allowable value: 110°C . A DC load current is applied in order to make the isolation of the loss for each level of current easier.

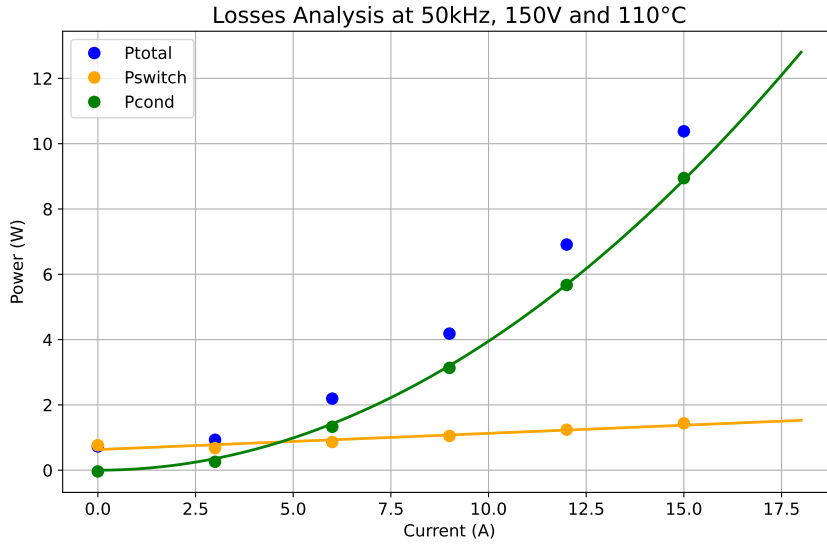


Figure 5.17: Simulation results of losses in a single-leg inverter for a DC bus of 150 V , a DC incoming current, a switching frequency of 50 kHz and a dead time of 50 ns . The dots represent the simulation results, while the continuous lines represent the linear and quadratic regressions for the switching and conduction losses respectively.

The losses have then been extracted for different values of current and switching frequency. Conduction losses are assumed to be independent of switching frequency. Under this assumption, the conduction and switching losses can be separated. In Figure 5.17, the results

of the simulation for a DC bus of 150 V, a DC incoming (from load to inverter) current, a switching frequency of 50 kHz, a duty-cycle of 50% and a dead time of 50 ns are represented by the dots. The switching frequency has been increased to 50 kHz to enable a more significant impact of the switching losses. It can be observed that the switching losses follow a linear trend with the current, while the conduction losses follow a quadratic trend, which is consistent with the model developed in Chapter 3. Linear and quadratic regressions have thus been applied. The results are shown by the continuous curves in the figure.

Based on the regression of the simulation results for incoming and outgoing currents, a model of the losses in a single-leg inverter, taking as parameter the output current value, can be established:

$$P_{loss}(I, f) = P_{switching}(I) + P_{conduction}(I) = f(a + b \cdot I_{sw}) + c \cdot I_{RMS}^2 \quad (5.4)$$

where I_{sw} is the average absolute value of the current, which can be estimated as $I_{sw} = \frac{2\sqrt{2}}{\pi} I_{RMS}$.

The coefficients obtained by simulation are presented in Table 5.4:

Coefficient	70 V	150 V
a	$4.58 \cdot 10^{-6}$	$1.12 \cdot 10^{-5}$
b	$8.92 \cdot 10^{-7}$	$1.02 \cdot 10^{-6}$
c	$3.94 \cdot 10^{-2}$	$4.02 \cdot 10^{-2}$

Table 5.4: Coefficients of the loss model for a single-leg inverter.

The value of the coefficient c is close to the on-resistance of the transistor at 110 °C, which is of 42.5 mΩ according to the datasheet [30].

An estimation of the losses in a single-leg inverter, with a junction temperature of 110°C depending on the output RMS current is shown in Figure 5.18. First, the conduction losses are much higher than the switching losses, since the level of power dissipation for 25 kHz and 50 kHz are quite similar. This result is consistent with the characteristics of the selected device and confirms that increasing the switching frequency incurs only a small additional penalty. Second, the losses are higher for a DC bus of 150 V than for a DC bus of 70 V, but the difference is not significant. This is an incentive to choose a higher DC bus voltage, as it will reduce the current for a given power, and thus reduce the conduction losses, without significantly increasing the switching losses.

For a three-phase inverter, the total losses can be estimated by multiplying the losses in a single leg by three. This model can thus be used directly to design the final inverter, by determining the number of transistors in parallel needed depending on the maximum current and switching frequency, in order to keep the total power dissipation under the maximum limit (represented by the horizontal dashed line in the figure for the designed prototype).

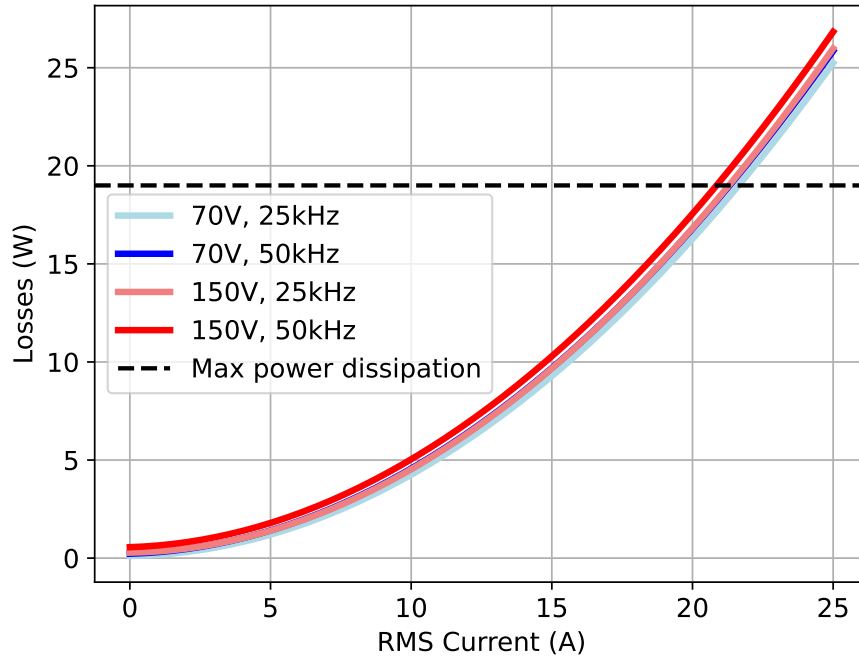


Figure 5.18: Estimated total losses per inverter leg for a sinusoidal output current.

However, these estimations do not take into account the ripple in the output current, which increases the true RMS current and thus the losses. This ripple depends on the switching frequency, the back-EMF and the synchronous inductance of the motor. Further simulations should be performed to account for this effect.

6 Experimentation

The purpose of this chapter is to validate the simulation results presented in Chapter 5 using an experimental prototype. It details the PCB implementation and the measurement setup. The switching waveforms and loss measurements are compared with the simulations, and several hypotheses are proposed to explain the differences.

6.1 Experimental setup

In order to make the experimentation easier to be carried out, a single-leg inverter is designed and implemented. Its simplified schematic is shown in Figure 6.1. The inductor L ensures an almost constant DC output current, while the resistor R , which can be connected to the voltage supply (incoming current) or to the ground (outgoing current), regulates the current and dissipates power. This will make the measurement of the dissipation with an incoming and outgoing current possible, for different switching frequencies. With a duty-cycle of 50%, the value of the DC current can be estimated as $I_{DC} = \frac{V_{BUS}}{2R}$. The DC bus voltage will be set to 70V and 150V, while the load resistance will be varied to obtain different levels of current. The switching frequency is set to 50 kHz, to minimize the output current ripple, and to make the input filtering easier compared to a lower switching frequency. This also reduces the size of the bootstrap capacitor needed for the gate driver.

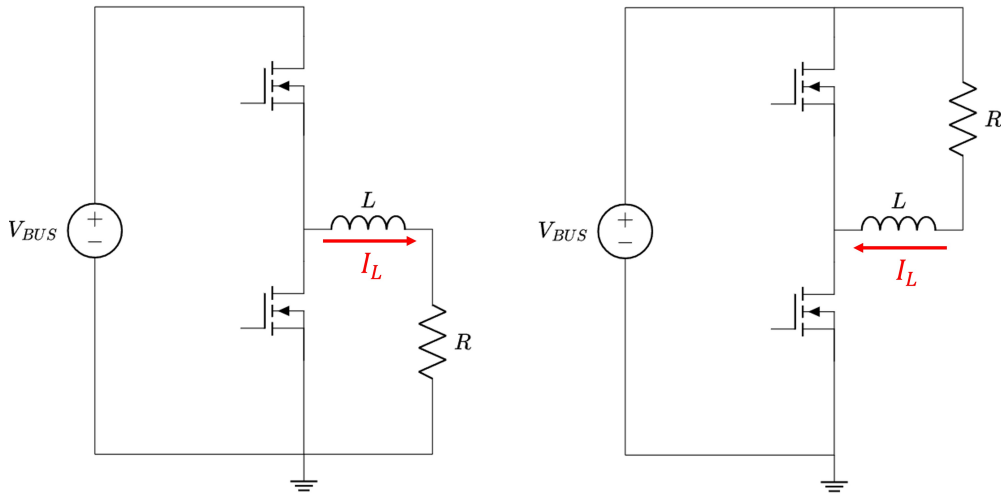


Figure 6.1: Simplified schematic of the single-leg inverter used for experimentation.

6.2 Practical implementation

6.2.1 Circuit schematic

A schematic of the circuit, shown in Figure 6.3, was first produced using the KiCad software. Its purpose is to select all required components and verify that connections are correctly made.

The gate driver used is the EiceDRIVER 2EDB8259Y from Infineon [52], shown schematically in Figure 6.2. It can source up to 5 A and sink up to 9 A. It takes as input the PWM signals, produced by an external microcontroller. The microcontroller selected is a NUCLEO-G491RE development board from STMicroelectronics.

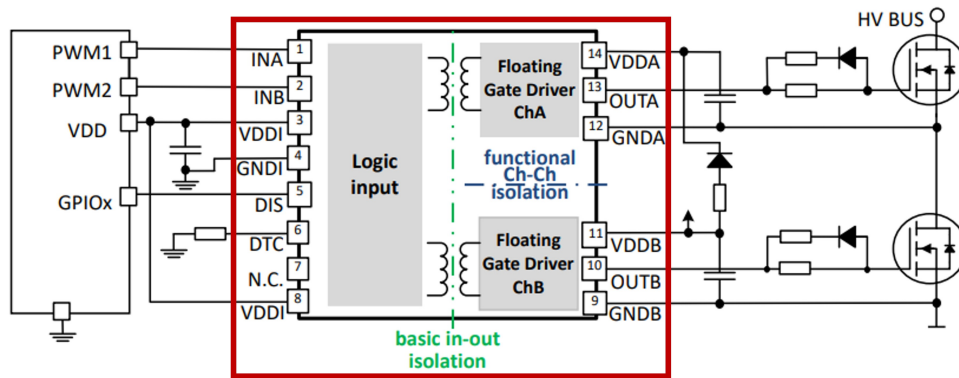


Figure 6.2: EiceDRIVER 2EDB8259Y gate driver schematic [52].

In addition, small decoupling capacitors have been added close to the gates, and close to the drain of the upper transistor, in order to supply the transient current during switching, and to reduce thus the voltage spikes caused by the parasitic inductance of the power loop. To damp the power oscillations between this parasitic inductance and the decoupling capacitors, a damper has been added. This works on the same principle as for the damping of the input filter presented in Section 5.3. The value of the damping resistance have been computed for a parasitic inductance of 5 nH [45].

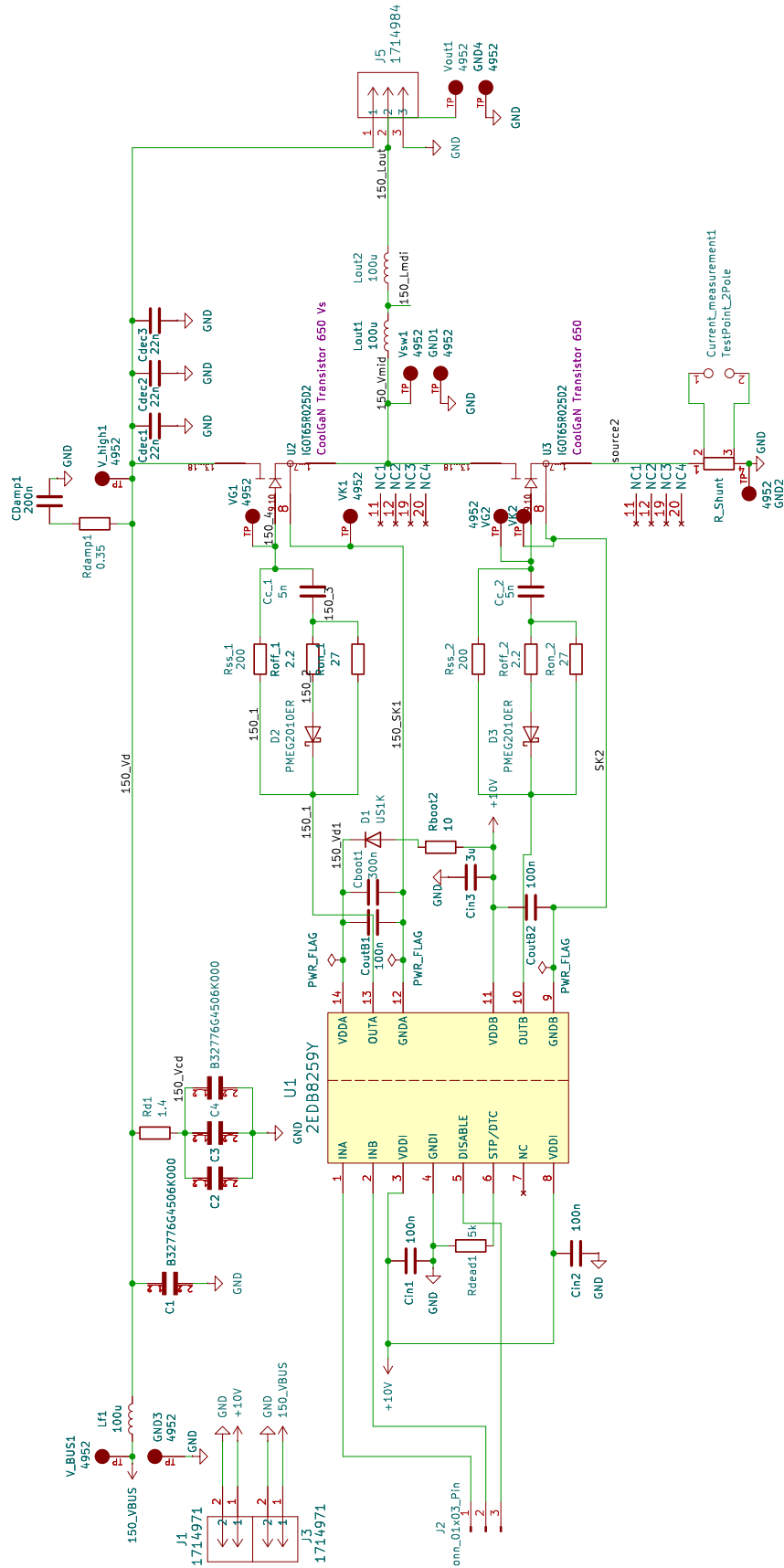


Figure 6.3: KiCad schematic of the PCB.

6.2.2 PCB characteristics

Once the schematic is validated and the component footprints are confirmed, the PCB layout can be designed. Several kinds of board layouts can be chosen. The one selected for this project is a 4-layer PCB, with each layer having a thickness of $35\ \mu\text{m}$. These layers are isolated by dielectrics: $360\ \mu\text{m}$ of PR7628 between the outer and inner layers, and $710\ \mu\text{m}$ of FR4 between the inner layers. A representation of the cross-section of a 4-layer PCB is shown in Figure 6.4. As it can be also seen in the figure, connections between the different layers are made through vias.

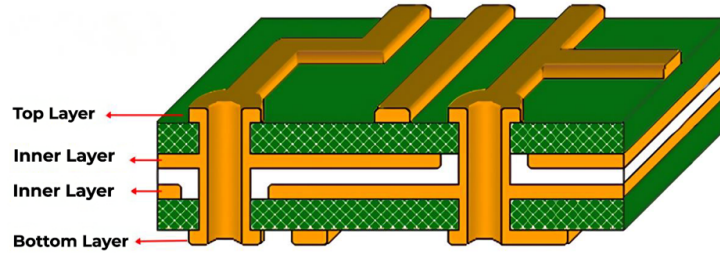


Figure 6.4: Cross-section of a 4-layer PCB, adapted from [53].

Using a multi-layer PCB allows traces to cross each other, and increases the compactness of the design. The amount of current that can be carried depends on the width of the trace, the thickness of the copper layer, and the temperature rise allowed. From IPC 2221, the maximal permissible current in a trace is given by:

$$I = k \cdot \Delta T^{0.44} \cdot (W \cdot H)^{0.725} \quad (6.1)$$

where I is the current in A, ΔT is the temperature rise in $^{\circ}\text{C}$, W is the trace width in mils, H is the thickness of the copper layer in mils, and k is a coefficient that depends on whether the trace is on an inner or outer layer. For an outer layer, $k = 0.048$, while for an inner layer, $k = 0.024$.

Increasing the thickness of the copper layer allows thus more current to be carried, but also increases the cost and complexity of the PCB. Inner layers carry less current than outer layers because of their lower thermal dissipation capacity. To increase the current-carrying capacity, large planes of copper can be used, since it improves the heat dissipation. Parallelizing the current path on several layers and using vias to connect them is also a good solution to increase the current-carrying capacity, and has been made possible thanks to the use of a multi-layer PCB.

During the routing process, limiting the loop area has been the main concern, in order to reduce the parasitic inductances. Both sides of the PCB have been used to place the components, in order to reduce the size of the board and thus its price.

6.2.3 Parasitic inductance mitigation

Power loop

The primary concern is the power loop formed by the transistors and the decoupling capacitors (Figure 6.5). This loop is critical because of the fast current transients that occur during switching.

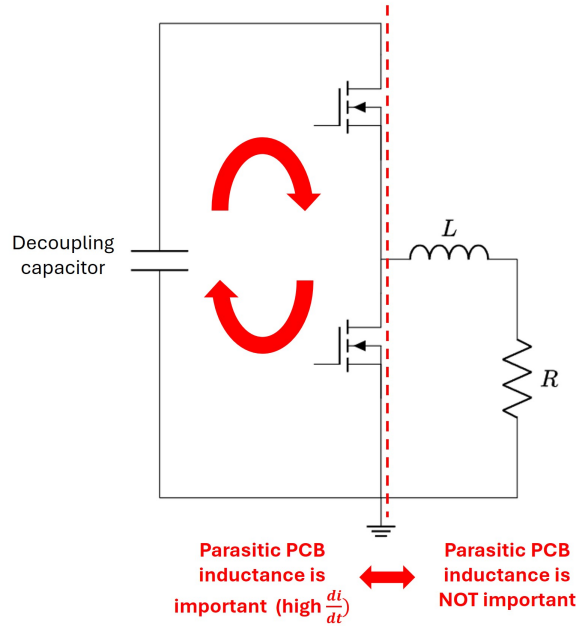


Figure 6.5: Representation of the power loop and its parasitic inductance, adapted from [45].

To mitigate this issue, the layout has been designed to minimize the loop area, by placing the transistors and the decoupling capacitors as close as possible to each other. The path taken by the current during switching is represented by the arrows in Figure 6.6 (green for outgoing current, orange for incoming one). In this figure, only the connections on the bottom layer (in blue) are represented.

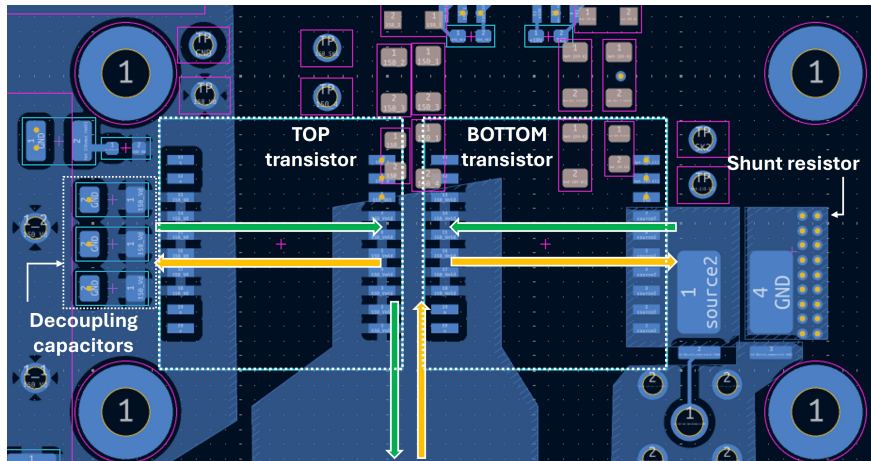


Figure 6.6: PCB layout, bottom layer.

The multi-layer PCB allows the return current to flow beneath the transistors back to the decoupling capacitors, further reducing the loop area. As shown in Equation 6.1, the current-carrying capacity of an inner trace is half that of an outer trace. To mitigate this issue, the return current path is parallelized on both inner layers, as represented in Figure 6.7.

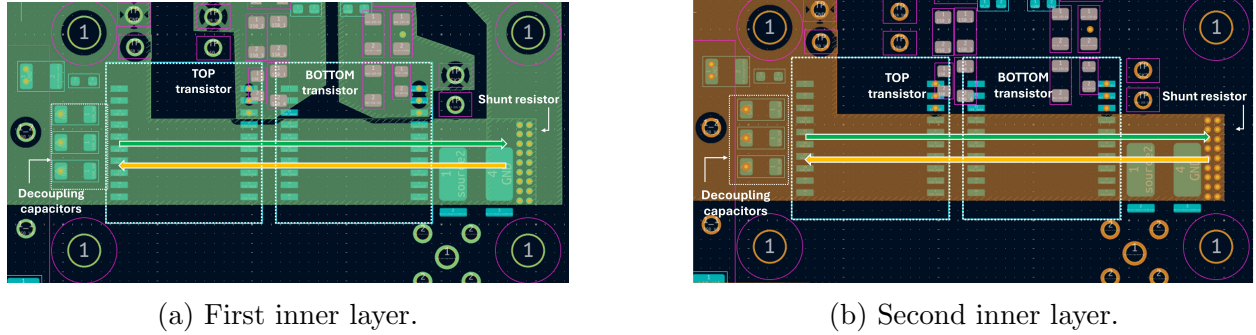


Figure 6.7: PCB layout, inner layers.

However, it has to be noted that the use of the inner layers for the return current path increases the parasitic capacitance present at the source of the upper transistor/drain of the bottom transistor. This capacitance is created by the superposition of the copper plane between the two transistors (which has a large $\frac{dV}{dt}$) and the inner layers (which are at a constant potential). This capacitance will oppose the rapid change of voltage during switching, increasing the switching losses.

Gate driving loop

The same logic applies for the gate driving loop. The gate current of the transistors has also a fast variation during switching, and the parasitic inductance needs thus to be minimized. The layout of the gate driver loop is represented in Figure 6.8.

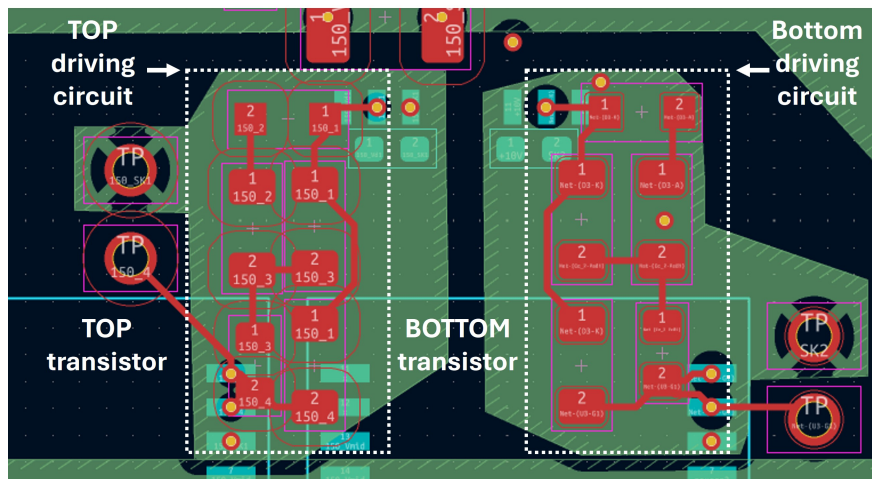


Figure 6.8: PCB layout, gate driver loop.

The components of the driving circuit are on the top of the board (with connections in red), while the return path is on an inner layer (in green) in order to reduce the current loop

area. No copper plane is placed under the return path, to limit parasitic capacitance. This is significant especially for the top transistor, since its source is floating. The entire return path plane is thus going from 0 to V_{BUS} and then from V_{BUS} to 0 at each switching event, which creates a large $\frac{dV}{dt}$ and thus a large capacitive current if the parasitic capacitance is not reduced.

6.2.4 Manufactured PCB

Photographs of the PCB before and after the soldering of the components are shown in Figures 6.9 and 6.10. The PCB has been manufactured by Eurocircuits, and has 180 mm x 100 mm dimensions.

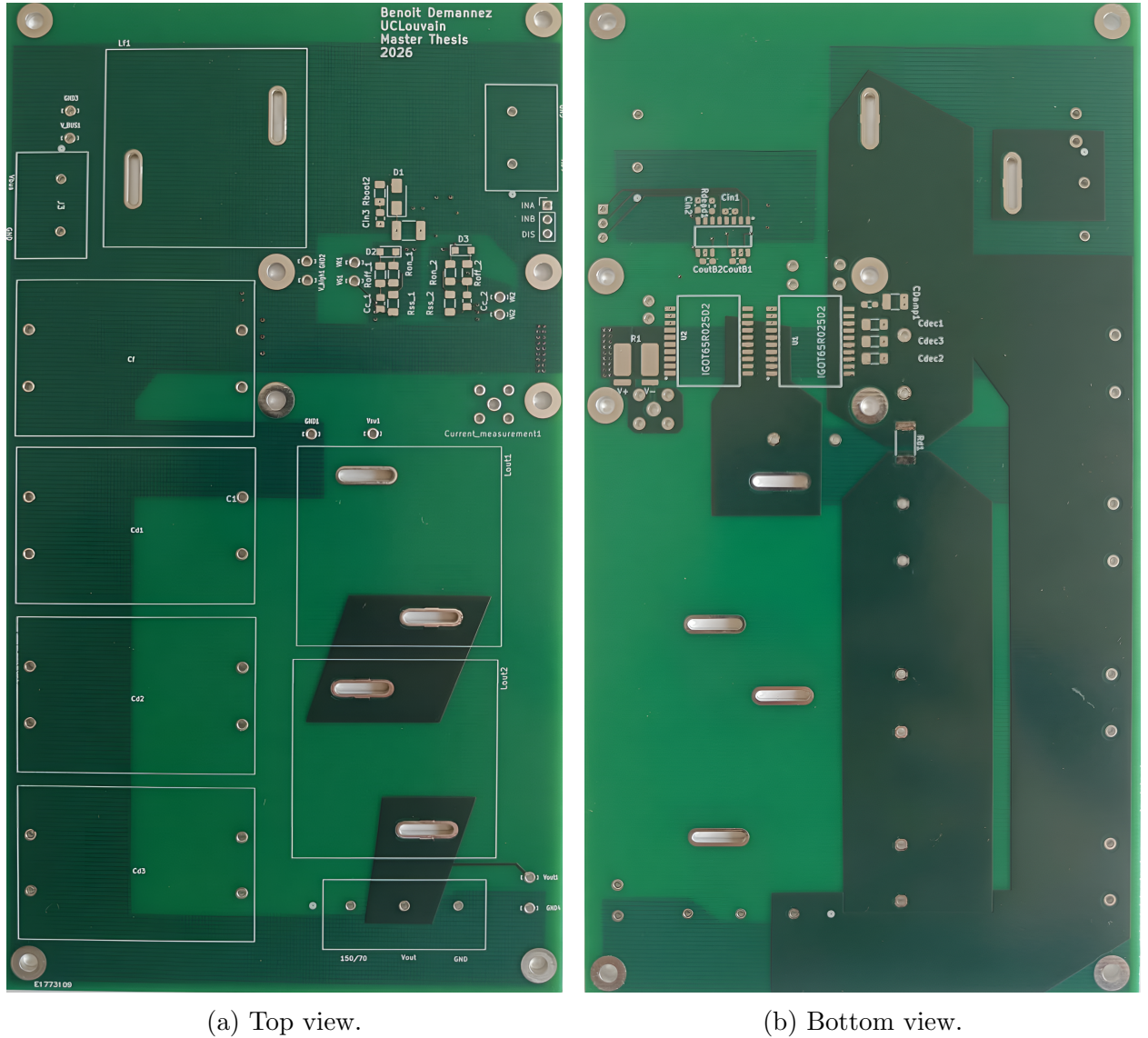
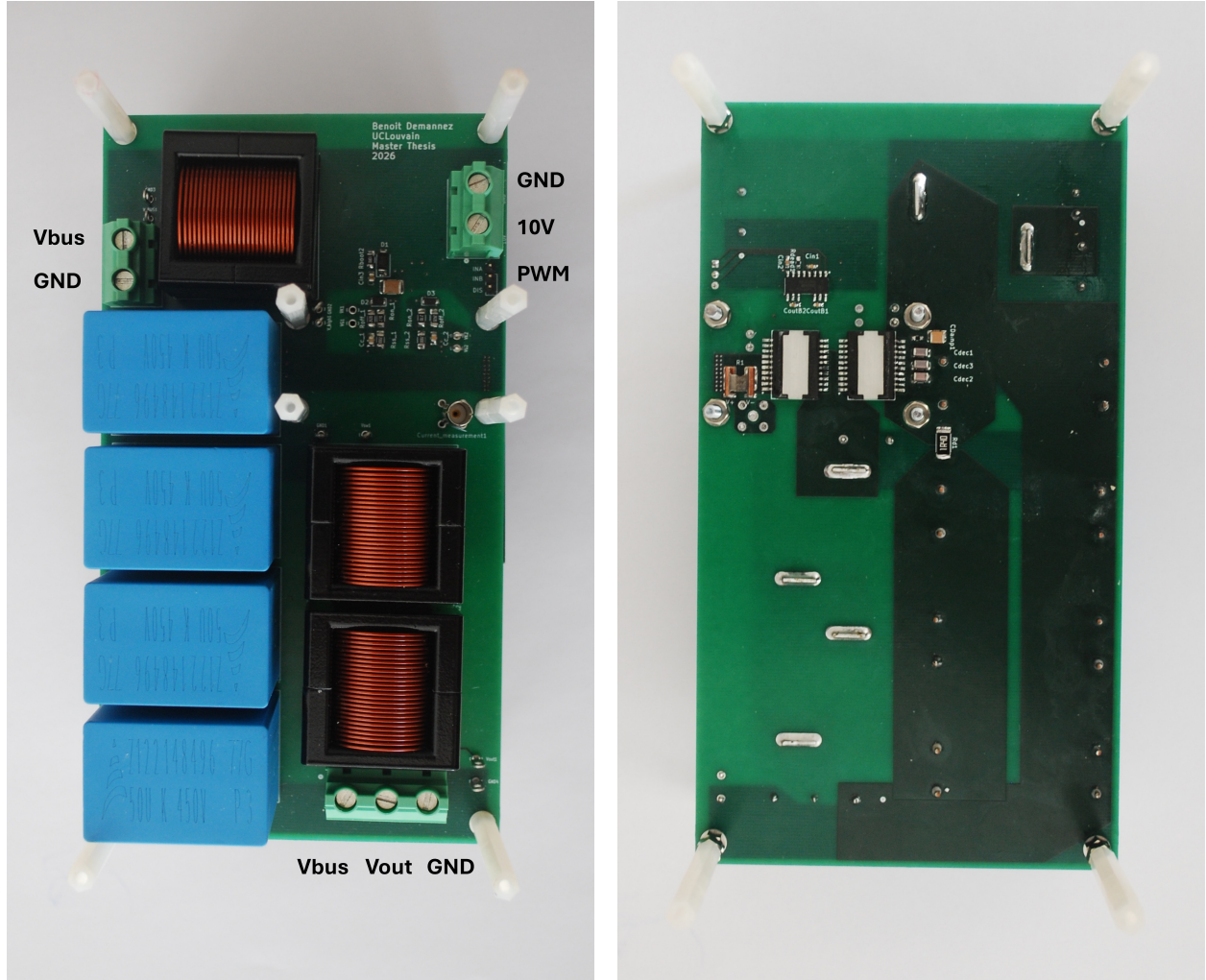


Figure 6.9: PCB photographs before component soldering (180 mm x 100 mm).



(a) Top view.

(b) Bottom view (without heat sink).

Figure 6.10: PCB photographs after component soldering.

6.3 Measurements and results analysis

Several measurements have been performed to characterize the prototype:

- Waveforms observation with an oscilloscope to validate the simulation waveforms
- Estimation of the parasitic elements of the circuit
- Measurement of the power losses of the converter

6.3.1 Set-up description

The measurement set-up is shown in Figure 6.11. The device is powered by two DC power supplies (boxed in yellow). The first supplies the gate drive circuit at a constant 10 V, the second supplies the bus voltage up to 150 V.

The oscilloscope, boxed in black, is used to observe and record the waveforms. The voltage is directly measured with probes, and the current can be visualized by using a current clamp and a current sensor (boxed in blue), which gives an output voltage proportional to the current. The current clamp is placed around the wire of interest and measures the magnetic field generated by the current.

The inverter prototype is boxed in gray, with the microcontroller used to generate the PWM signals for the gate driver.

Large resistive loads (boxed in green) dissipate the power flowing through the inverter. By connecting the available resistors in series and in parallel, different load values are obtained to test different current levels. An electronic load would have allowed easier and more controlled current adjustment, but was unavailable in the laboratory.

To measure the input and output power, multimeters, boxed in brown, are used. They can be put in series with the circuit and work as ammeters, or in parallel and work as voltmeters.

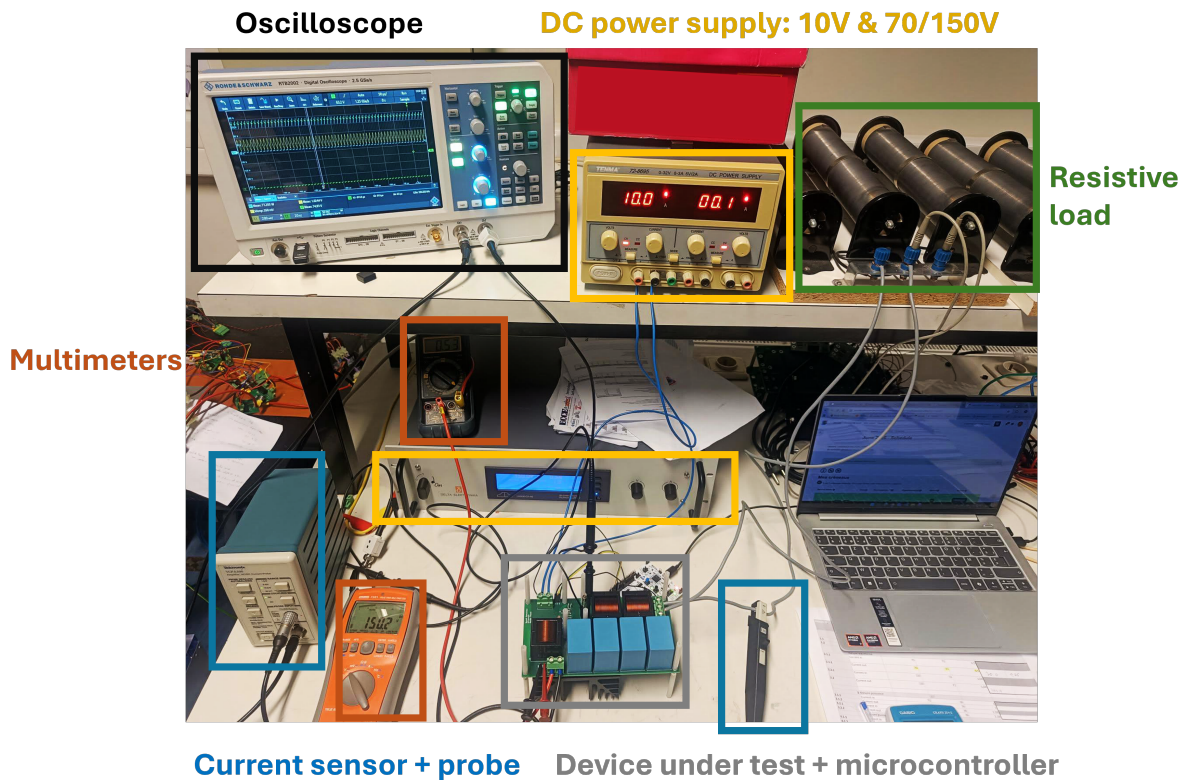


Figure 6.11: Picture of the measurement set-up.

6.3.2 Waveforms measurement and analysis

The measurement of the output waveforms (voltage before the output inductance and current through the load) are shown in Figure 6.12. The load is here connected between the bus voltage and the output of the inverter, which means that the current is incoming (positive).

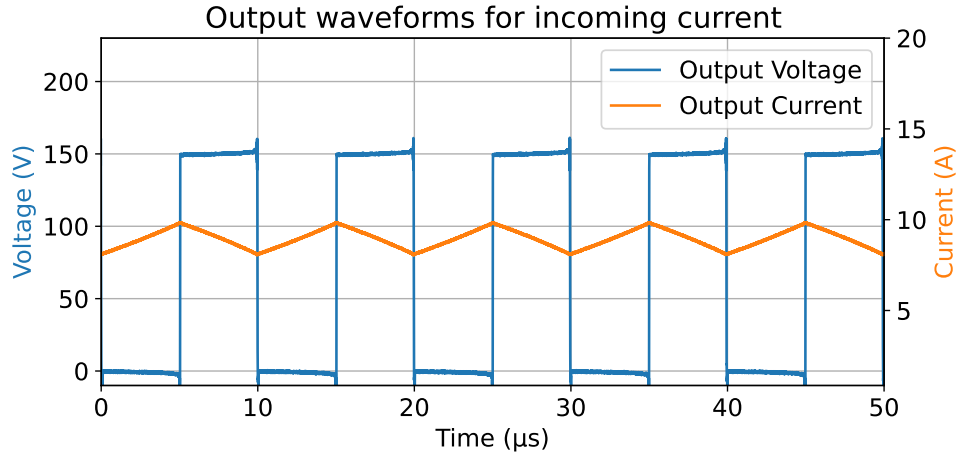


Figure 6.12: Measured output voltage and current waveforms with the resistive load connected between the bus voltage and the output of the inverter (incoming current).

The gate and output voltage switching waveforms, measured around the switching events, are shown in Figures 6.13 and 6.14. The waveforms are compared to the ones obtained with LTspice, in order to validate the simulations. Significant oscillations are visible on the gate voltage waveforms; these have been filtered with a 50 MHz low-pass filter to enable clearer comparison with simulations.

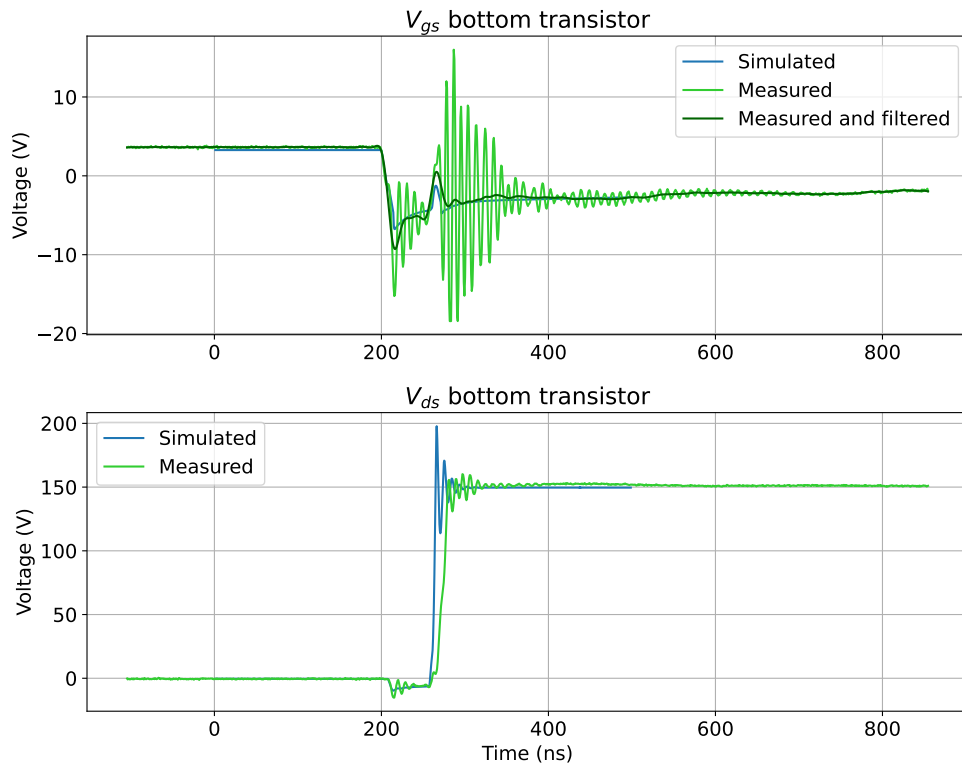


Figure 6.13: Comparison of measured and simulated waveforms during the low-to-high output voltage transition, with an outgoing current.

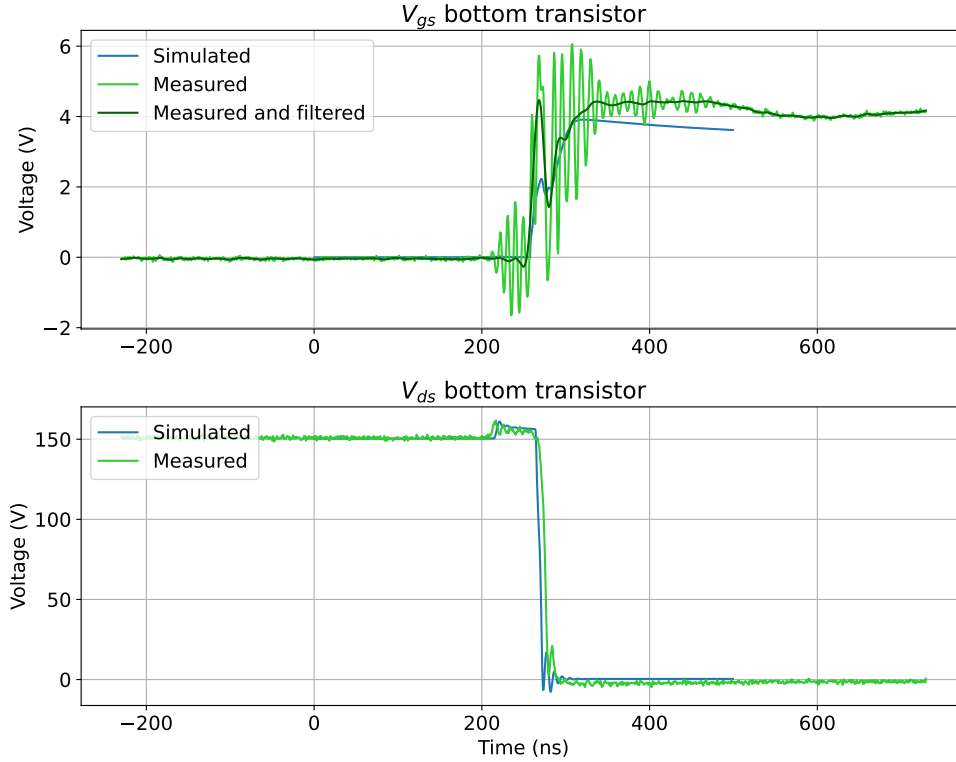


Figure 6.14: Comparison of measured and simulated waveforms during the high-to-low output voltage transition, with an outgoing current.

The frequency of the oscillations observed on the gate voltage is around 100 MHz, and could be explained by several factors, as explained in the next sections [54, 55, 56].

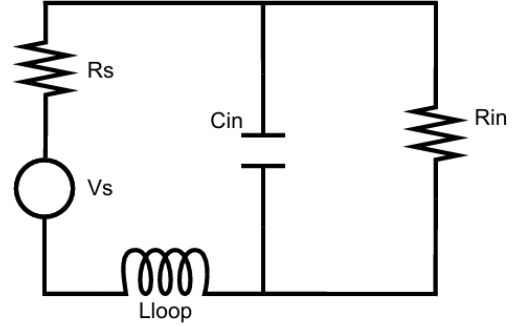
Measurement artifacts

The measurements have been performed with a passive probe and an alligator clip, as illustrated in Figure 6.15. The loop formed by the alligator clip introduces a parasitic inductance, which resonates with the input capacitance of the probe and produces the observed oscillations. Estimating the input capacitance of the probe to be around 10 pF, and the parasitic inductance of the loop to be around 10 nH/cm of perimeter, the frequency of the oscillations can be estimated to be close to 100 MHz, which is consistent with the measurements.

The second effect of this loop is to capture noise from radiated emissions, due to the high current and voltage variations. In fact, it has been observed that reducing the loop area reduced the amplitude of the oscillations.



(a) Alligator clip used for the measurement [55].



(b) Equivalent circuit model of a passive probe [56].

Figure 6.15: Passive probe and its equivalent circuit model.

Parasitic oscillations

Real oscillations can also be present due to the parasitic inductances of the gate driving loop, and the capacitances of the transistors. The PCB layout was designed to minimize this effect, but a gate loop inductance of approximately 2.5 nH is still present [45]. The input capacitance of the chosen transistor is around 1nF [30]. The switching frequency can be computed as $f = \frac{1}{2\pi\sqrt{LC}}$, which gives a frequency of around 100 MHz, also consistent with the measurements.

To summarize, the observed oscillations can be explained by both measurement artifacts and real parasitic oscillations. To reduce the measurement artifacts, several techniques are presented in [54, 55, 56].

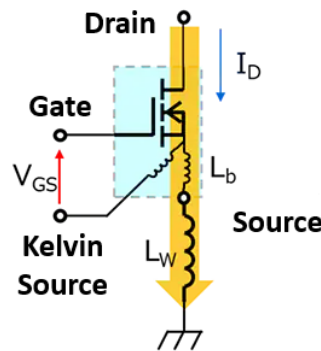


Figure 6.16: Schematic of the connection points of the transistor [57].

Differences between the simulation and the measurements can also be explained by the point where the measurement was taken. In the simulation, the voltage is taken between the gate

and the kelvin source of the transistor, while in the measurement, the gate voltage is referenced to the ground. The kelvin source, represented in Figure 6.16, is a separate connection point on the source of the transistor, which allows to measure the voltage directly at the source of the transistor, without being affected by the voltage drop across the source connection. This can lead to differences in the observed waveforms, especially during switching events where large current variations occur, creating thus large voltage drops across the source connection.

6.3.3 Estimation of the board conduction losses

In addition to the losses in the transistors, power is also dissipated in the traces of the PCB and in the filter inductances. The parasitic resistances of the traces are difficult to estimate analytically because of their irregular geometry. They were therefore measured experimentally by supplying a constant DC current and measuring the voltage drop at several points in the circuit. The schematic of the circuit with only resistive elements is represented in Figure 6.17.

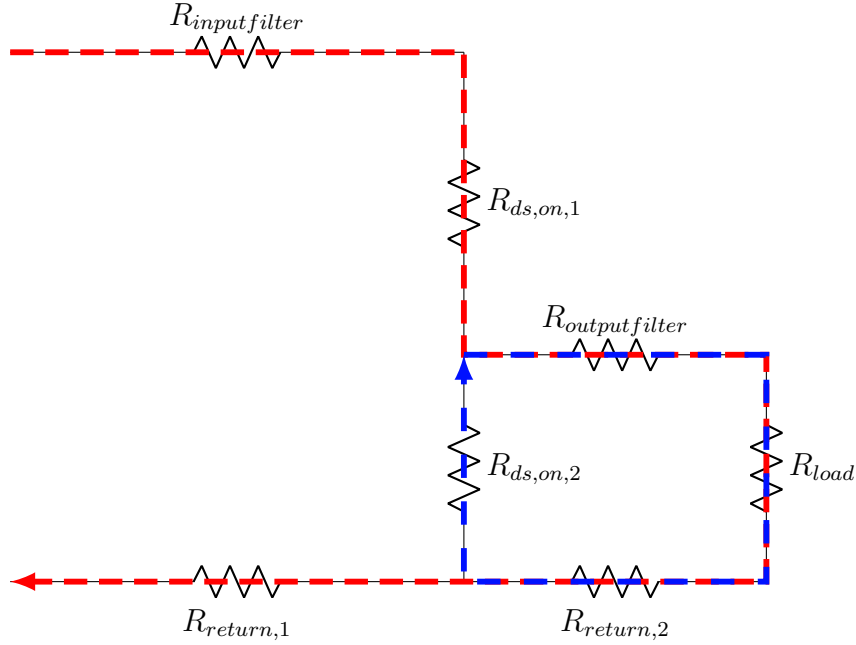


Figure 6.17: Equivalent resistive circuit model of the single-leg inverter for PCB loss estimation.

$R_{inputfilter}$ and $R_{outputfilter}$ represent the losses in the input and output inductances, $R_{ds,on,1}$ and $R_{ds,on,2}$ represent the on-resistance of the transistors. $R_{return,1}$ and $R_{return,2}$ represent the return path resistances, while R_{load} represents the load resistance. The value of these resistances are given in Table 6.1. The arrows represent the current path during an outgoing current. The current follows the red arrow when the upper transistor is on, while the blue arrows represent the current path in the other case. With a duty cycle of 50%, as in our experimental situation, the average resistance seen by the current is thus the average resistance of the two paths. Excluding the transistor on-resistances (already accounted for in the LTspice simulation), the mean parasitic resistance is $R = 16.17m\Omega$.

Resistance	Value ($m\Omega$)
$R_{inputfilter}$	5.93
$R_{outputfilter}$	10.76
$R_{return,1}$	1.45
$R_{return,2}$	1.705

Table 6.1: Measured parasitic resistances of the PCB and filters.

Extra AC losses in the inductors are also present. According to the manufacturer, at 50 kHz and 10 A, this would represent around 200 mW for the output inductors. These losses are not taken into account in the next sections because they are more difficult to estimate, since they depend on the current ripple.

6.3.4 Power losses

Several measurement techniques were investigated to estimate the converter losses with sufficient accuracy.

Output power measurement methods

- **Instantaneous power via oscilloscope math.**

The output voltage was acquired with a voltage probe and the output current with a current clamp. The oscilloscope math function was used to multiply both waveforms and obtain the instantaneous power $p(t) = v(t) \cdot i(t)$, whose mean value yields the active output power. The input power was computed from the mean input current and voltage, measured with multimeters. Although this method is the most direct, it is sensitive to the phase shift introduced between the voltage and current channels by the probes and the current clamp. Even a small phase error leads to a significant error in the computed active power, and thus in the estimated losses [58]. This effect is particularly severe at high efficiency, where the losses represent only a small fraction of the total power.

- **RMS voltage and current with multimeters.**

The RMS output voltage and current were measured with multimeters after the output filter, while the input power was computed as in the upper point. The product $V_{RMS} \cdot I_{RMS}$ yields the apparent power, not the active power, because the inductive behavior of the load introduces a phase shift between voltage and current, resulting in a power factor below unity. Consequently, this method overestimates the real power delivered to the load and leads to unrealistic loss values.

- **Load resistance and RMS current method.**

The load resistance R_{load} was measured with an ohmmeter and the RMS output current I_{RMS} was acquired with a multimeter. The output power was then estimated as:

$$P_{out} = I_{RMS}^2 \cdot R_{load} \quad (6.2)$$

This formulation is insensitive to the phase shift between voltage and current channels and bypasses the apparent power issue of the previous method. Its main limitation is the temperature dependence of the load resistance: as the resistor dissipates power, its resistance drifts, introducing an error in the power estimation. To control this effect, the resistance was measured immediately before and after each acquisition. Despite this precaution, residual thermal drift remains a source of uncertainty. Another limitation is the accuracy of the RMS current measurement. The multimeters claim to measure the true RMS value up to 100 kHz, but likely introduce errors due to the current ripple at the inverter output. However, this method provided the most consistent results and was therefore adopted for the measurements presented in this chapter. Increasing the output inductance would reduce this ripple and thus improve the accuracy of the RMS current measurement.

Results

The measured losses for input voltages of 70 V and 150 V are shown in Figures 6.18a and 6.18b, respectively. A curve including the parasitic resistance of the board computed in Section 6.3.3 have been added in the graphs. The simulations have been performed with a junction temperature of 50°C.

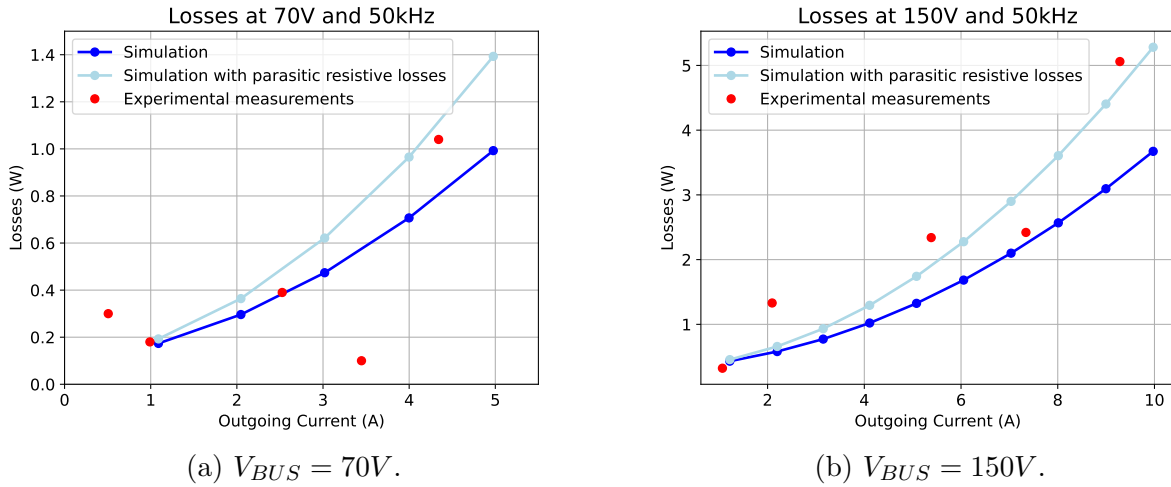


Figure 6.18: Comparison of the losses obtained with the measurements and the model at a switching frequency of 50 kHz and for an outgoing current.

Sources of measurement difficulties

Although the experimental results follow the same trend as the simulated ones, quantitative differences remain. The following points summarize the main sources of uncertainty that limit the accuracy of the loss measurement.

- **High efficiency and small loss magnitude.**

The high efficiency of the converter means that the losses represent a very small difference between two large quantities: the input and output power. Any relative error

in either measurement is amplified significantly when computing their difference, as illustrated in Figure 6.19. For instance, at a bus voltage of 150 V, an input power of 698.2 W and an output power of 693.1 W yield an efficiency of 99.3 %, with losses of only 5.1 W. This fundamental limitation of the electrical input–output method at high efficiency is well documented in the literature [58], and calorimetric measurement methods have been proposed as a more reliable alternative in this regime.

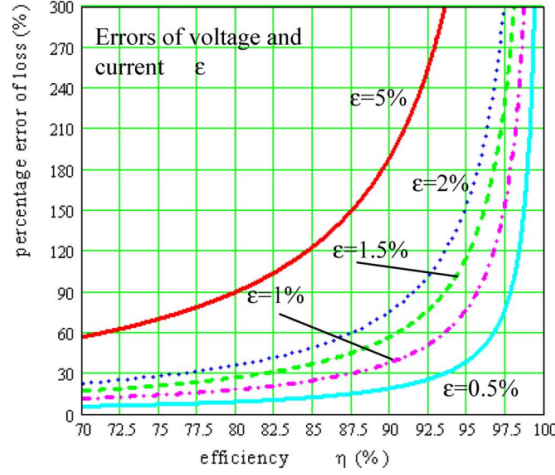


Figure 6.19: Percentage error of loss measurement as a function of converter efficiency, for given errors on the voltage and current measurements [58].

- **Bandwidth limitations of measurement instruments.**

Current clamps and voltage probes have finite bandwidth. GaN HEMTs switch with dV/dt and dI/dt rates that can exceed the measurement bandwidth, causing the instruments to filter out part of the switching transient. This leads to an underestimation of the true RMS current and distorts the instantaneous power waveform, introducing errors in loss calculations.

6.3.5 Discussion

Despite the measurement challenges described above, the experimental results follow the same trend as the simulated ones: the losses increase with current in a manner consistent with the model predictions. The analysis of the waveforms in Section 6.3.2 also supports this close relation between measurements and simulations. This agreement validates the LTspice model as a reliable tool for loss estimation within the expected operating range. The main discrepancy between measurements and simulations can be largely attributed to the parasitic resistances of the PCB and inductors, which are captured by the corrected simulation curve. The remaining gap can be explained by the uncertainty sources identified above.

The LTspice model, as well as the loss estimation for a single-leg inverter shown in Figure 5.18, can therefore be used with confidence to size a full three-phase inverter. However, parasitic elements should be carefully considered, as their impact on losses has clearly been identified in the measurements.

7 Conclusion

This master's thesis proposed and experimentally validated a structured methodology for the design of a three-phase inverter dedicated to flywheel energy storage systems for space applications. The work investigated the trade-offs associated with semiconductor technologies, switching frequencies, DC bus voltages, and modulation strategies, with the objective of identifying suitable design choices for an 8 kW peak-power system.

The different **semiconductor technologies** were introduced in Chapter 3. A conduction and switching loss model was developed in order to compare the different devices using only parameters typically available in component datasheets, summarized in Table 3.2. The comparison, carried out in Chapter 4, showed that the different semiconductor technologies exhibit relatively similar performance at low switching frequencies. However, the performance gap increases significantly as the switching frequency rises. SiC MOSFETs and GaN HEMTs demonstrated excellent switching performance compared to Si MOSFETs, with switching losses representing less than 15% of the total losses at 15 A and 50 kHz. Since SiC devices are not yet widely qualified for space applications, GaN HEMTs appear to be particularly attractive candidates. For these reasons, the IGOT65R025D2 GaN HEMT was selected for the remainder of the study.

The **modulation strategies** were presented in Chapter 2, together with their impact on output voltage quality and maximum current levels. Compared to SPWM, THIPWM reduces the current by approximately 15%. FWM was also investigated, as it further decreases the maximum current by around 10% compared to THIPWM (see Figure 2.14), while simultaneously reducing the switching activity. However, this comes at the expense of significant harmonic distortion close to the modulation frequency, as illustrated in Figure 2.9. Such a strategy could considerably reduce transistor losses, but also modifies the trade-off between conduction and switching losses. Consequently, a device with higher switching losses but lower conduction losses could become more suitable than the selected GaN HEMT. Ultimately, the choice between SPWM and FWM will depend on the motor requirements in terms of efficiency, reliability, and long-term operation.

As shown in Figure 2.4a, increasing the **switching frequency** improves the quality of the output voltage for both SPWM and THIPWM, limits the output current ripple, but also increases switching losses. The optimal switching frequency is therefore driven by the motor sensitivity to voltage harmonic distortion and power quality requirements. Nevertheless, with the selected GaN HEMT, switching losses account for only a small fraction of the total losses, which supports the use of a relatively high switching frequency. Consequently, a switching frequency of 50 kHz was selected for the experimental studies.

The **DC bus voltage** also has a major influence on the current levels involved, as shown in

Figures 2.16 and 2.17. The analysis suggested that a 28 V bus voltage should be avoided, as it only allows a limited synchronous inductance value and requires very high currents. Figure 5.18 shows that increasing the DC bus voltage only increases the inverter losses by approximately 6% at 15 A RMS under SPWM operation. This strongly supports the use of a 150 V DC bus, as it reduces the current amplitude by more than a factor of two. However, a bidirectional DC/DC converter would then be required between the DC bus and the inverter, increasing the number of components and potentially reducing the overall system efficiency.

Beyond the component selection study, this work also established in Chapters 5 and 6 practical design guidelines for the implementation of an inverter. The gate driver stage was designed and validated using LTspice simulations, which provide a useful reference for verifying switching waveforms before committing to a PCB implementation, and comparing with experimental results. An LC input filter was also designed to comply with ECSS recommendations. The same design methodology can readily be extended to other switching frequencies by adjusting the filter cut-off frequency accordingly. Furthermore, the thermal analysis demonstrated that, under ECSS derating rules, each transistor may dissipate up to 9.5 W in space conditions. Finally, the loss estimation presented in Figure 5.18 can be used to determine the number of transistors required for the final inverter design. Although these results are specific to the selected device, the proposed methodology and design tools remain applicable to other semiconductor technologies. The experimental section also provided several practical guidelines for hardware implementation, such as the importance of minimizing parasitic resistances and inductances in the PCB layout, and the challenges associated with accurate power loss measurements at low power levels.

Future work should focus on the integration of the inverter with the final motor drive system, particularly regarding transient operating conditions. A complete three-phase system simulation, including the control stage and the DC/DC interface (for $V_{BUS} = 150V$), could further improve the reliability of the final design prior to hardware implementation. Overall, this work demonstrates the feasibility and relevance of high-frequency GaN-based inverters for future space flywheel energy storage systems.

A Extra simulated switching waveforms

The simulated switching waveforms of the gate driver during the low-to-high and high-to-low transitions are shown in Figures A.1 and A.2, respectively. The waveforms are obtained for an outgoing current of 10 A and a bus voltage of 150 V.

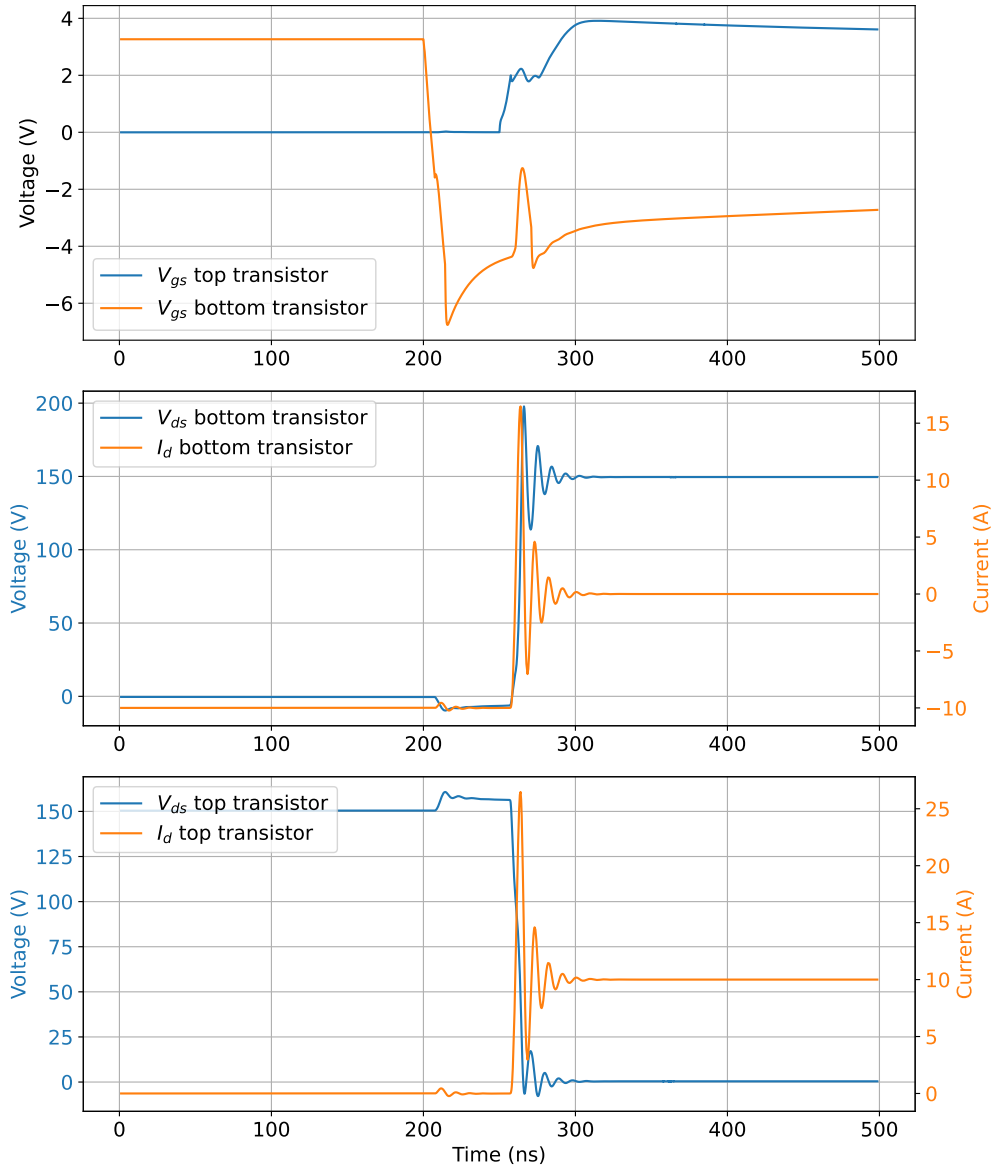


Figure A.1: Simulated switching waveforms during low-to-high transition with an outgoing current of 10 A and $V_{BUS} = 150V$.

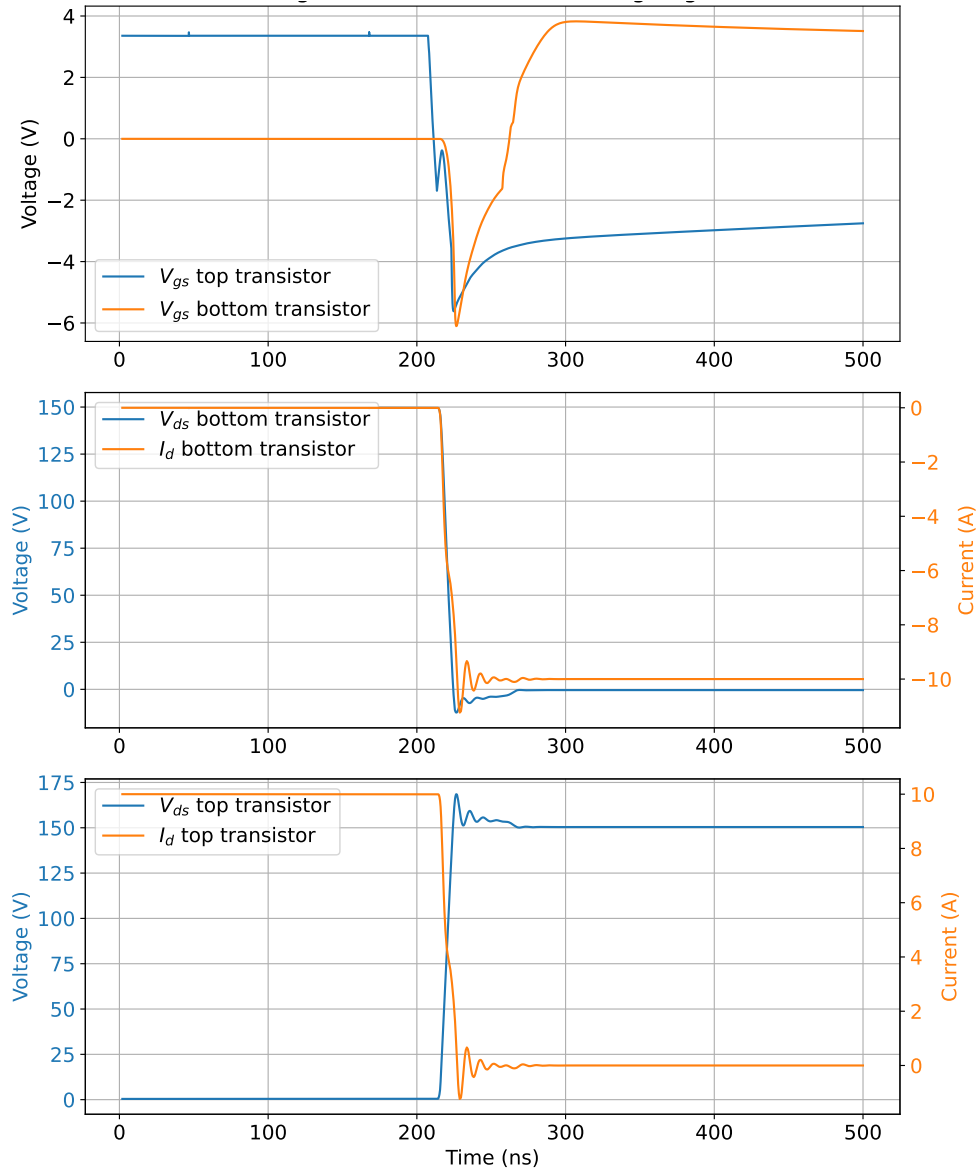


Figure A.2: Simulated switching waveforms during high-to-low transition with an outgoing current of 10 A and $V_{BUS} = 150V$.

B Computation of the maximum RMS current value with flux weakening

The power transferred from the inverter to the motor can be expressed by the following equations (see Section 2.2.2):

$$\begin{cases} P = 3 \frac{V_{inv} E_0 \sin(\delta)}{X_s} \\ P = 3 I E_0 \cos(\psi) \end{cases} \quad (\text{B.1})$$

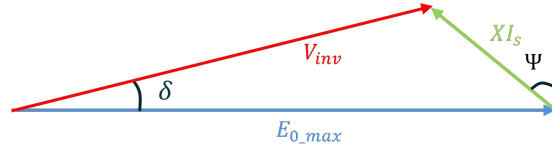


Figure B.1: Phasor diagram of the equivalent circuit used to study the power flow between the inverter and the motor with flux weakening technique

Then, the following equations can be derived geometrically from the phasor diagram in Figure B.1:

$$V_{inv} \cos \delta + X_s I_s \sin \psi = E_{0,max} \quad (\text{B.2})$$

By replacing X_s and I_s by their expression in terms of the power, the following equations can be derived:

$$V_{inv} \cos \delta + \frac{V_{inv} E_0 \sin(\delta)}{P} \cdot \frac{P}{3 E_0 \cos(\psi)} \sin \psi = E_{0,max} \quad (\text{B.3})$$

$$V_{inv} \cos \delta + V_{inv} \sin \delta \tan \psi = E_{0,max} \quad (\text{B.4})$$

The maximum RMS current can then be computed as follows:

$$I_{s,max} = \frac{P}{3 E_{0,max} / 2} \quad (\text{B.5})$$

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