UCLouvain

École polytechnique de Louvain

High quality substrate for high frequency FD SOI technology

Author: **Pieter CARDINAEL**
Supervisor: **Jean-Pierre RASKIN**
Readers: **Denis FLANDRE, Valeria KILCHYTSKA, Martin RACK**
Academic year 2018–2019
Master [120] in Chemical and Materials Engineering

Acknowledgements

This work and the completion of this master's thesis have only been possible with the contribution of valuable people that helped and supported me. I want to thank them here.

First, I want to thank my supervisor, Prof. Jean-Pierre Raskin, for his continuous advice, and for making himself available despite his agenda. He made me feel involved in the work led in the RF SOI group, and offered me great support for future projects.

I would also like to thank Arka Halder, Lucas Nyssens and Massinissa Nabet, for letting me sit in their office during this semester, and for the good atmosphere in everyday work.

More particularly, I would like to thank Martin Rack, for his explanations and the time he spent with me sharing his expertise of Atlas and RF-SOI in general.

I would like to thank Valeriya Kilchytska and Denis Flandre for taking the time to read this thesis.

Finally, I want to thank my family and loved ones for their support and encouragements.

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Chapter 1

Introduction

Following the invention of the first semiconductor devices such as transistors, there has been a strong push towards connecting multiple active components together to perform more and more complex functions. Because of their reduced dimensions, the only way to reliably connect transistors or other devices is to build them on the same support, or substrate, on which all the connections are also placed, forming an integrated circuit (IC). By far, the most widely used material for this purpose is silicon (Si). This semiconductor is abundant, cheap, and allows relatively easy fabrication of most semiconductor devices. Indeed, very pure 300 mm-diameter *wafers* of crystalline Si can be manufactured in large quantities for devices where it is crucial that current carriers can flow in the most unperturbed way. It is also easy to dope by adding small quantities of impurities, to tune its electrical properties in precise regions, and silicon dioxide, SiO_2, can be readily grown on its surface. SiO_2 is necessary for metal-oxide-semiconductor field effect transistors (MOSFETs), the most widely used type of transistor in integrated circuits. For these reasons, silicon

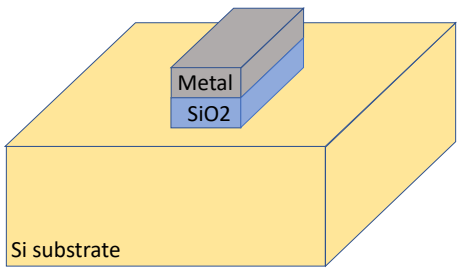


Fig. 1.1: Schematic of a MOSFET, with the silicon dioxide playing a crucial role.

processing and technology is now extremely developed, and has been able to bring devices to dimensions where physical limits of the materials come into play, enabling the integration of an increasing number of transistors on the same chip (Fig. 1.2 a).

A promising candidate for ultimate dimension reduction is silicon-on-insulator (SOI) technology, and more particularly fully-depleted SOI (FD SOI). This technology is based on stacking of a thin Si film on a layer of SiO_2 called the buried oxide (BOX), located on the Si wafer surface (Fig. 1.2 b). This Si film and the BOX can be made as thin as 7 nm and 25 nm, respectively, in what is called the ultra-thin body and BOX (UTBB) technology. Advantages of FD SOI technology include

reduction of short-channel effects, appearing at small dimensions, and operation at very high frequency, making it ideal for high-speed applications [1]. Parallel to the improvement of semiconductor devices, integration of different systems on the same chip (forming a system-on-chip) has been desired to reduce dimensions of multi-chip designs and decrease power consumption. In order for this to be possible, these systems would have to share the same substrate. In particular, integration of digital systems with components operating at radio-frequency is seen as an important step. Radio-frequency integrated circuits (RFICs) are used for communication systems such as antennas, smartphones, or internet-of-things applications. The substrate used for RFICs must satisfy to certain requirements, because its properties influence the functioning of RF devices. Key factors of good-functioning RF blocks are losses, governing power consumption, and linearity, guaranteeing the integrity of an electrical signal after its treatment by the circuit [2]. It is possible to assess the electrical properties of substrates using simple passive structures called coplanar waveguide (CPW) transmission lines (Fig. 1.3). In these lines, also used as interconnects in RFICs, the propagation of a signal is strongly influenced by the underlying substrate, as a large portion of the electric field between two of its electrodes crosses it, and thus by electrical measurements of the line one can extract material information such as effective resistivity or permittivity. Substrates meeting the requirements of RFICs exist, but historically only specialized and expensive substrates such as silicon-on-sapphire or gallium arsenide (GaAs) have been used, impeding their integration with CMOS Si technology (Fig. 1.2 c).

Thus, silicon-based substrates have been investigated as candidates for RF applications, as they could enable integration of RF and digital systems on the same chip. Silicon is however a lossy material by nature, having a certain electrical conductivity, and is also a non-linear material, since the carrier distribution can vary with applied voltage as a result of the field-effect. In 1997, SOI technology using a low-doped, high-resistivity (HR) Si substrate was first shown to present promising RF performance [4]. Indeed, the BOX provides a shielding from the substrate and thus allows a reduction of losses, which are already reduced by using a substrate with high resistivity. However, an important obstacle prevents the integration of RFICs on HR-SOI, namely the existence, at the substrate surface below the BOX, of an inversion electron-rich layer creating a highly conducting path despite the presence of the BOX, drastically increasing losses and non-linearity. These mobile charges are attracted by fixed charges at the SI/SiO_2 interface.

In 2005, it was discovered by Prof. J-P Raskin's group that a thin layer of polysilicon deposited below the BOX suppressed this effect, exploiting the large density of defects at grain boundaries, which capture free carriers and prevent them from participating in parasitic conductance (Fig. 1.2 d). The so-called trap-rich substrate, commercialized by Soitec, is nowadays present in all smartphone front-end modules [5]. Integration with FD SOI technology, however, poses a potential problem to the trap-rich substrate. Indeed, this technology heavily relies on the implantation below the BOX of a heavily-doped *ground plane implant*, which enables better control on the MOSFET channel and increases analog performance [6]. Potentially, the quality of this implant could be compromised, if it were to be defined in polysilicon, rather than in the typical crystalline Si of standard SOI wafers.

In this work, an alternative solution to the parasitic surface conductance and thus for integrating RFICs on the SOI platform and taking the spot (e) in Fig. 1.2 is

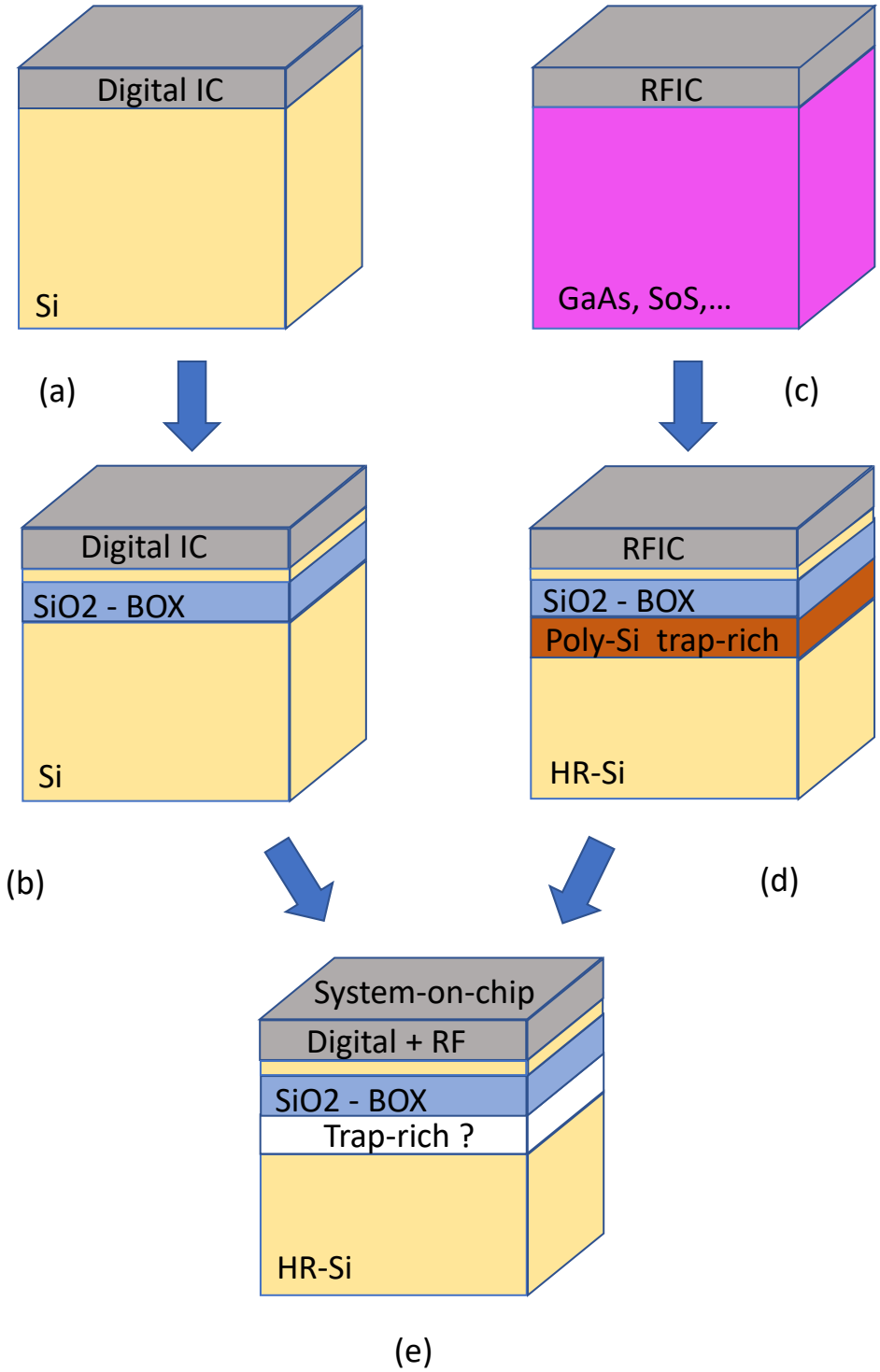


Fig. 1.2: Evolution of substrate technologies for digital and RF technologies, and their union in system-on-chip integration. (a) is standard silicon technology, and (b) represents the advanced digital FD SOI technology. On the RFIC side, (c) shows the non-Si based substrates, and (d) the trap-rich substrate. Ultimate integration, in (e), brings the two platforms on a single, high performance substrate.

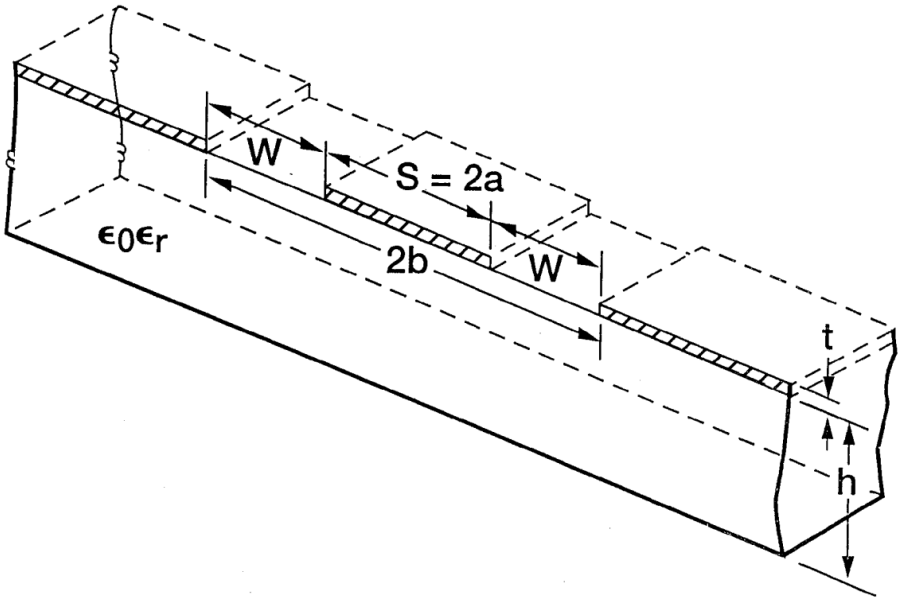


Fig. 1.3: Cross-section of a CPW line (from [3])

explored. It consists of the implantation below the BOX of a series of alternatively P and N doped implants, instead of the polysilicon layer (see Fig. 1.4). These implants

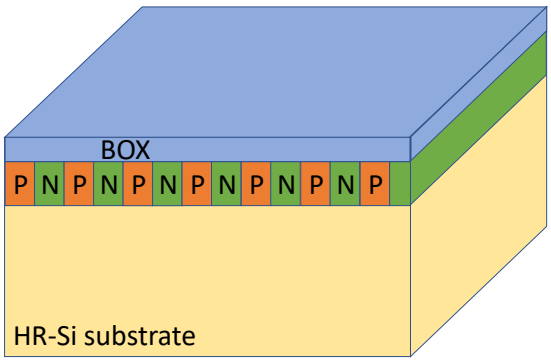


Fig. 1.4: Schematic of the P-N buried implant layer under the BOX.

naturally form PN junctions, and subsequently depletion regions between them. These regions, having a poor carrier concentration, present a very high resistivity and interrupt the parasitic surface conductance layer.

Chapter 2 is dedicated to a state of the art review of literature as well as an investigation of the quality of ground plane contacts in polysilicon. Chapter 3 presents the buried implant substrate in more details. Numerical simulations allows to understand the origin of the RF performance of this solution. In chapter 4, extensive use is made of the TCAD software Silvaco Atlas, to simulate and understand the effect of various parameters of the buried implants on the small- and large-signal performance. This allows to pave to way for an optimization of the design. It ends by characterizing the UCLouvain sample at high temperature for assessing its possible use in this domain. Finally, a conclusion summarizes results and gives future perspectives.

Chapter 2

State of the art

Before presenting the substrate technology developed in this work, a literature study of the state of the art of radio-frequency integrated circuits is done. The current most widely-used approach to substrate design is also presented.

2.1 Transmission Lines

In this section, transmission lines are introduced, and discussed. Two main topologies are investigated, and the coplanar waveguide (CPW) line is discussed in more detail.

2.1.1 Introduction

In monolithic microwave integrated circuits (MMIC), devices are interconnected using metallic conductors. At the frequencies used in RF ICs, the signal wavelength becomes of the same order of magnitude as the physical length of the wire, which can thus not be considered as an equipotential. The signal has to be treated as a wave, propagating in what is called a *transmission line*. As a rule of thumb, wave aspects have to be considered once the interconnect reaches a length of 1/20th of the wavelength. The wavelength λ is linked to the signal frequency :

$$v_{ph} = f\lambda \tag{2.1}$$

Where v_{ph} is the phase velocity. From this equation, it is clear that the critical length is smaller the higher the frequency. For example, at 10 GHz, the wavelength in silicon is of the order of 1 mm.

The goal of a transmission line is to assure integrity of the signal when it is transmitted from one point to another. Two main criteria are used to quantify the quality of a transmission :

Insertion losses A transmission line should maximize the amount of power transferred, and thus minimize the losses in the signal path. Insertion losses are usually classified in two categories, depending on their origins. *Conductor losses* are due to the finite metal resistivity, skin effect and surface rougness. *Dielectric, or substrate losses* are dependent on the properties of the substrate.

Linearity In order for the signal to be usable after transmission, the line must induce only linear attenuation of the signal. In other words, the shape of

the signal must not be altered. To quantify the linearity of a transmission, a pure sine wave is transmitted, and the harmonic components created by a nonlinear line are measured. The *harmonic distortion* is defined as the ratio of the power of the harmonic components to the power of the fundamental component. Generally, the second or third harmonic is considered. The total harmonic distortion metric considers all components.

2.1.2 Theory of transmission lines

A transmission line can be characterized by a set of electrical constants : R (resistance), L (inductance), C (capacitance) and G (conductance), all defined per unit length, as shown on Fig. 2.1. The line can be represented as a succession of infinitesimal two-port networks. Signals propagating along such lines obey the

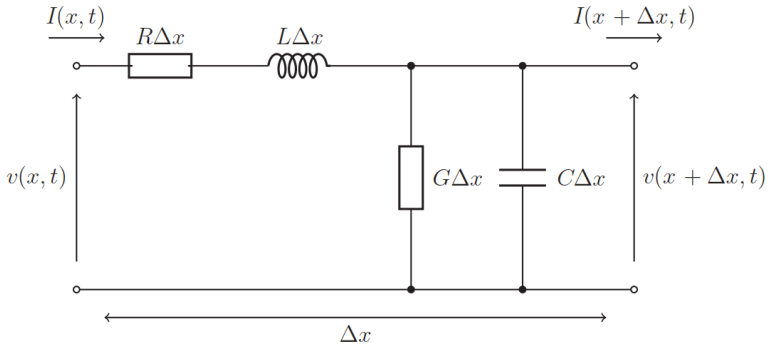


Fig. 2.1: Lumped element equivalent circuit of an infinitesimal section of a transmission line (from [7]).

Telegrapher's equations :

$$\frac{\partial V(x)}{\partial x} = -(R + j\omega L)I(x) \tag{2.2}$$

$$\frac{\partial I(x)}{\partial x} = -(G + j\omega C)V(x) \tag{2.3}$$

The general solution for these equations is, for $V(x)$:

$$V(x) = V^+ \exp(-\gamma x) + V^- \exp(\gamma x) \tag{2.4}$$

Where γ is called the propagation constant :

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta \tag{2.5}$$

The real part of γ is the loss factor, responsible for attenuation of the wave. The imaginary part is called the phase factor. In Eq. 2.4, $V(x)$ contains two waves propagating in opposite directions. Indeed, in many cases, the transmission line contains a incident wave and a reflected wave, traveling in the opposite direction. This is due to a mismatch in impedances, and is the reason why the characteristic impedance of a transmission line is such an important quantity.

Characteristic impedance is an inherent property of a transmission line, independent on its length but on its other dimensions, geometry and material. It can be

defined as the input impedance of an infinite line, or as the ratio between voltage and current at any point in the line. Its expression can be derived from the Telegrapher's equations :

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.6}$$

It is crucial to know and to control Z_0 in a transmission line, for power transmission reasons. Indeed, maximal power transfer between a source with impedance Z_S and a load with impedance Z_L is achieved when the following relationship is satisfied :

$$Z_L = Z_S^* \tag{2.7}$$

This condition is called impedance matching. When a transmission line is connected between source and load, the same condition holds between source and line, and between line and load. When impedances are matched, reflection is canceled and the energy that is not dissipated in the lossy line is transmitted to load. In practice, most elements in MMICs have impedances of $50\,\Omega$, and this is the value that the characteristic impedance of transmission lines will have as well.

2.1.3 Different types of transmission lines used in RF ICs

For integration on printed circuit boards, the transmission lines used in MMICs need to be compatible with the fabrication techniques used to fabricate these circuits, and thus need to have a planar form. Planar transmission lines come in two main topologies : microstrip lines and coplanar waveguide (CPW) lines.

The thin film microstrip line (TFMS) is a two-conductor transmission line. The signal conductor is separated from the ground plane by a thin slab of dielectric material, as seen in Fig. 2.2. If the TFMS line is built using the back-end of line (BEOL) layers, the silicon substrate lies below the bottom conductor. This allows effective shielding of the substrate losses by the ground plane, and the insertion losses in the TFMS line topology are dominated by the conductor losses ($\alpha = \alpha_{sub} + \alpha_{cond} \approx \alpha_{cond}$). The characteristic impedance of a TFMS line is dominated by two parameters : the width w of the signal conductor, and the thickness h of the dielectric. In particular, the ratio h/w determines Z_c. Other parameters are the dielectric permittivity ε_r and the conductor thickness t. An approximate closed-form expression for $Z_{microstrip}$ was derived by Wheeler [8]. Dielectric thickness and permittivity are usually fixed by the process, leaving the signal conductor as the only adjustable parameter to obtain the desired characteristic impedance. For a 50-Ω TFMS line, w needs to be on the same order of magnitude than h [9].

A CPW line consists of a central signal conductor and two ground-planes on each side, as shown in Fig. 2.3. The conductors are directly in contact with the substrate (or the BOX, in RF-SOI technology), and the electric field penetrates into the substrate, which causes non-negligible substrate losses. To obtain the desired impedance, both the signal conductor width S and the spacing W can be adjusted. Indeed, when the substrate thickness is higher than twice the slot width, Z_c can be written only in terms of the ratio $S/(S + 2W)$ [3]. Wide signal conductors can thus be selected to minimize the conductor losses of a CPW line.

The advantages and drawbacks of these two topologies have been studied in [10]. TFMS lines allow better shielding from the substrate, but present high conductor

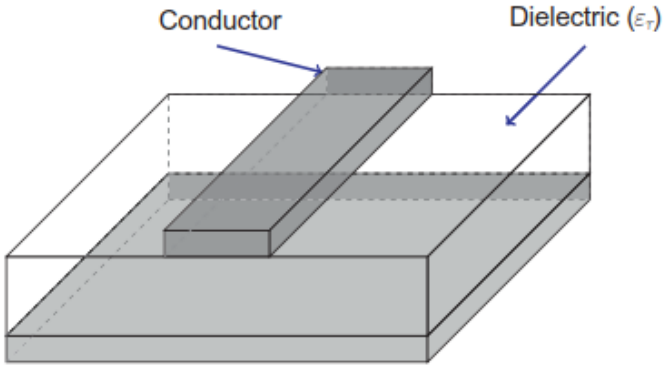


Fig. 2.2: Schematic of a TFMS line (from [7])

losses. Indeed, technological constraints limit the dielectric thickness and thus the conductor dimensions. On the other hand, the dimensions of the conductors composing a CPW line are not limited in theory, and metallic losses can be reduced. Furthermore, adequate substrate technologies can limit the substrate losses, and their development is crucial to the performance of the MMIC.

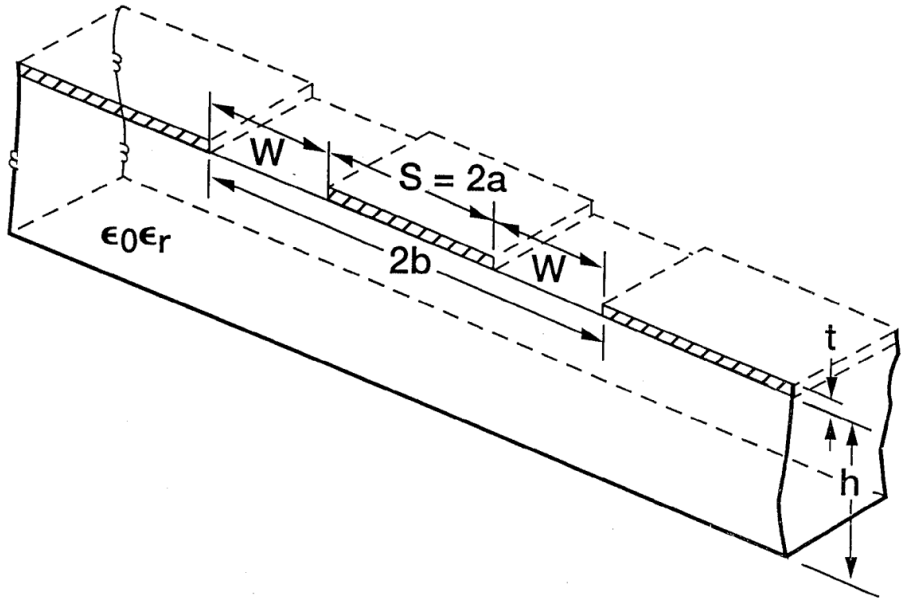


Fig. 2.3: Schematic of a CPW line (from [3])

2.1.4 Coplanar waveguide and its use for substrate characterization

Aside from its advantages as interconnect, the CPW topology is also a powerful tool to probe electrical properties of the substrate. Indeed, the filling factor q, which represents the proportion of electric field lines passing in the substrate, is close to 0.5 for a CPW line, implying that a large portion of field lines sense the substrate properties, as shown on Fig. 2.4. The substrate properties, such as effective resistivity and permittivity will thus define to a large extent the transmission line constants C and G, whereas L and R are dominated by the dimensions and conductor properties.

Implementing a CPW line on a substrate is thus a practical way to obtain its electrical characteristics, by extraction of the transmission line equivalent conductance and capacitance. Furthermore, for the same reason, nonlinearities originating from the substrate will have a large influence on the harmonic distortion along the line, and measuring the CPW line allows extraction about the voltage dependence of the substrate properties as well.

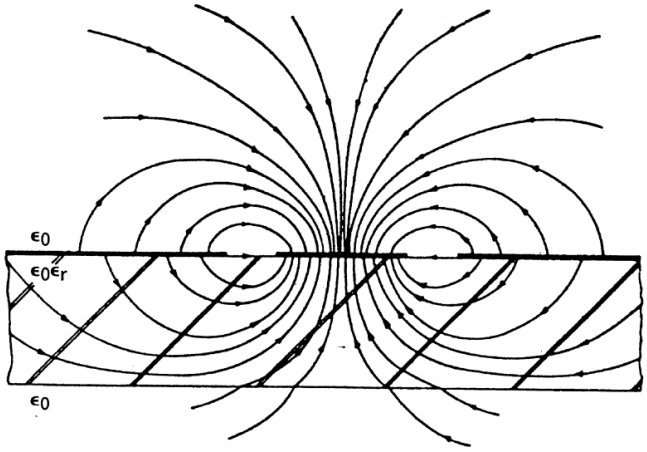


Fig. 2.4: Electric field lines distribution in a coplanar waveguide structure. A large portion of field lines penetrate into the substrate, allowing the CPW line to probe its properties (from [3]).

Even though the CPW line is an attractive interconnect, substrate losses must be controlled in this topology, as well as linearity. This is achieved by adequate technology, as will be shown in the following sections. Indeed, harmonic distortion for CPW lines on Si originates directly from the substrate [11], and line losses are dominated by α_D on standard Si substrates due to the lossy nature of this materials. Dielectric losses are described by the following expression for the loss factor :

$$\alpha_D = \frac{q\varepsilon_r \tan\delta}{\varepsilon_{eff}\frac{\lambda_0}{\sqrt{\varepsilon_{eff}}}} \tag{2.8}$$

Where q is called the filling factor, and ε_{eff} the effective permittivity. Oftentimes, α_D is dominated by $\tan\delta$, the loss tangent, which is a material property. This parameter is defined with help of the complex permittivity of the material : $\varepsilon = \varepsilon' + j\varepsilon''$. The ratio of the imaginary and real parts is the loss tangent :

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} = \frac{\sigma}{\omega\varepsilon'} \tag{2.9}$$

And is a measure of how much energy is dissipated in the material.

2.2 The Parasitic Surface Conductance Effect

Co-existence of digital, analog and RF devices on the same chip is necessary to further reduce size and power consumption while increasing speed, as all elements are close to each other. Integration is also a way to reduce cost because only one

chip is produced. Of course, in this approach, all devices and passive elements share the same substrate, and in particular, RF and digital functionalities. Historically, the CMOS process used for digital circuits was, and is still based on Si substrates. However, due to its semiconducting properties, Si has relatively high electrical conductivity ($\sigma_{Si} = 1.56 \times 10^{-3}\,\mathrm{S\,m^{-1}}$), making it a lossy substrate not well suited to RF applications. Therefore, RFICs have been built on substrates such as GaAs or silicon-on-sapphire (SOS), and more recently using SOI technology, which is subject to performance degradation due to the parasitic surface conductance effect.

2.2.1 Substrates for RF applications

Various substrates can be used, and are used, for their RF performance [2]. A good substrate, in this sense, must be linear, to prevent any harmonic distortion from originating and propagating through the substrate, perturbing other devices. This property is achieved when the substrate electrical properties, represented by an equivalent capacitance and conductance, are linear, i.e. are independent on the applied voltage. This is not the case for silicon, in which carrier concentration, and thus impedance, is voltage-dependent, in what is known as the field-effect. Insertion losses must be low in order to reduce energy consumption. Furthermore, for high speed applications the carrier mobility must be high.

III-V materials such as GaAs are attractive because of their high mobility. They also present low loss and high linearity. However, integration with CMOS technology is problematic, because these substrates present higher contamination risks. Furthermore, III-V substrates are fabricated on small wafers, making the process cost per chip high. As a result, digital functionalities are not directly integrated, but GaAs solutions are coupled to CMOS circuits.

SOS substrates are a part of the family of silicon-on-insulator substrates. They consist of a thin film of Si, grown epitaxially on a Al_2O_3 (alumina) substrate. Alumina is a very low loss material ($\tan\delta = 0.0006$ [7]), and the silicon film enables compatibility with CMOS processes. The main drawback of SOS is that, because of dimension mismatch between Al_2O_3 and Si crystal lattices, dislocations are created and deteriorate the mobility in the silicon thin film. Al atoms can also contaminate the film. These challenges are being addressed by using a SoS technology known as bonded SoS [2].

SOI technology is the most widespread approach, because it has the advantage of using exactly the same platform than digital SOI technology and CMOS process, and of being based on the cheap Si technology. As seen in Fig. 2.5, a SOI substrate is composed of a bulk Si substrate, on which a layer of SiO_2 is grown (of thickness scaling with device scaling). The active silicon thin film is located on top of this buried oxide (BOX). The main purpose of the BOX in RFICs is to electrically isolate each device from each other, and to suppress substrate coupling, as was shown for the first time in [4]. Compared to SoS, the insulator in SOI technology is the native SiO_2, which has the crucial advantage of being accepted in standard Si foundries (no contamination risks).

A SOI substrate can be produced in various ways, categorized into wafer bonding followed by etch-back and oxygen implantation. In the wafer bonding process (Fig. 2.6), two oxidized wafers are brought into contact, instantly bonding to each other (at room temperature) : the hydroxyl groups and H_2O molecules attract each

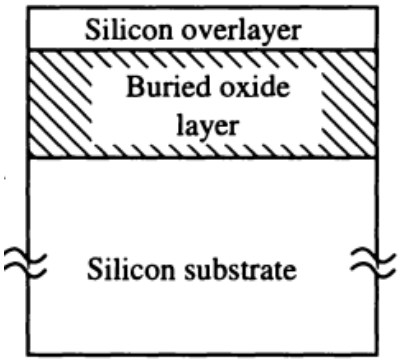


Fig. 2.5: Schematic of a SOI substrate (from [12]).

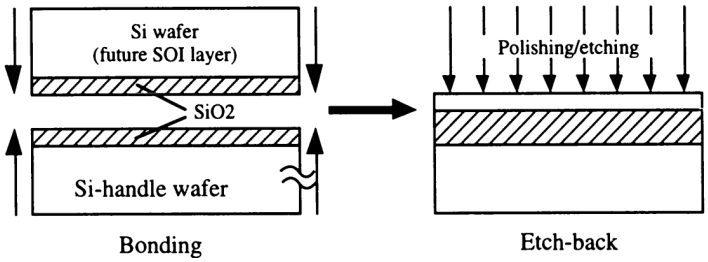


Fig. 2.6: The wafer bonding and etch-back process (from [12]).

other and form hydrogen bonds. An annealing step is executed to strengthen the bonds. Then, one of the two wafers is etched until the desired thickness of active silicon layer is obtained. At the bonding, it is possible that particles present on the surface become trapped between the two wafers. For a precise definition of the active layer thickness, etch-stop techniques have to be used.

In the oxygen implantation process (separation by implanted oxygen - SIMOX), a very high dose of oxygen ions is implanted below the surface of a bulk Si wafer, until the ratio of oxygen to silicon is 2 to 1, creating a new material, SiO_2, of desired thickness.

A combination of both techniques called Smart-Cut™uses a process described in Fig. 2.7. First, H^+ implantation is done at a controlled depth in an oxidized wafer

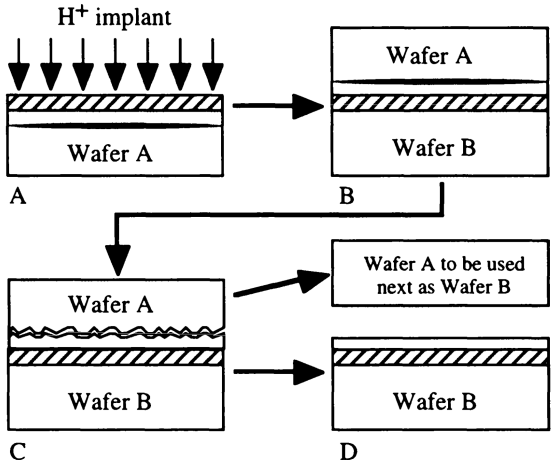


Fig. 2.7: The Smart-Cut™process (from [12]).

A. Following the wafer bonding technique, this wafer is attached to another wafer, labeled B. Then, instead of etching wafer A until the desired thickness is achieved, a heat treatment splits wafer A where the hydrogen was implanted, and this wafer A can be re-used as wafer B in a next cut. Because the etching step is suppressed (only a polishing step remains at the end), this method is much less costly that others.

In what follows, the focus will be on SOI technology, for economical aspects but also because of its maturity, and the advanced development of integration with the CMOS process.

2.2.2 Parasitic surface conductance and effective resistivity

The electrical insulation achieved using SOI technology is not perfect, and the underlying Si is still a lossy, conductive substrate. For this reason, high-resistivity (HR) silicon has been used to further reduce substrate losses. HR-Si is achieved by using a low dopant concentration ($1 \times 10^{13}\,\mathrm{cm}^{-3}$, whereas $5 \times 10^{16}\,\mathrm{cm}^{-3}$ is used for standard Si), lowering the density of free carriers in the substrate. Standard silicon has a resistivity of the order of $10\,\Omega\,\mathrm{cm}^{-1}$, while a HR substrate has ρ as high as $10\,\mathrm{k}\Omega\,\mathrm{cm}^{-1}$. This value is high enough for the substrate to appear lossless. Indeed, when ρ exceeds approximately $2\,\mathrm{k}\Omega\,\mathrm{cm}^{-1}$, conductor losses dominate α, and further improvement of the substrate resistivity will yield no significant benefit [13].

Independently of the fabrication method, positive fixed charges are present in the BOX (typical density : $1 \times 10^{11}\,\mathrm{cm}^{-2}$). In [14], measurements of a metal-oxide-semiconductor structure have shown that an inversion layer (for a P-type substrate) is formed on the substrate surface. The electrons in this inversion layer are attracted by the oxide fixed charges. Carrier concentration is thus locally increased in the first few micrometers below the BOX, and this situation causes an decrease of resistivity in this region (see Fig. 2.8) : a layer of *parasitic surface conductance* (PSC) is created, and observed losses increase dramatically in comparison with bulk HR-Si, where the absence of the BOX also prevents any fixed charges.

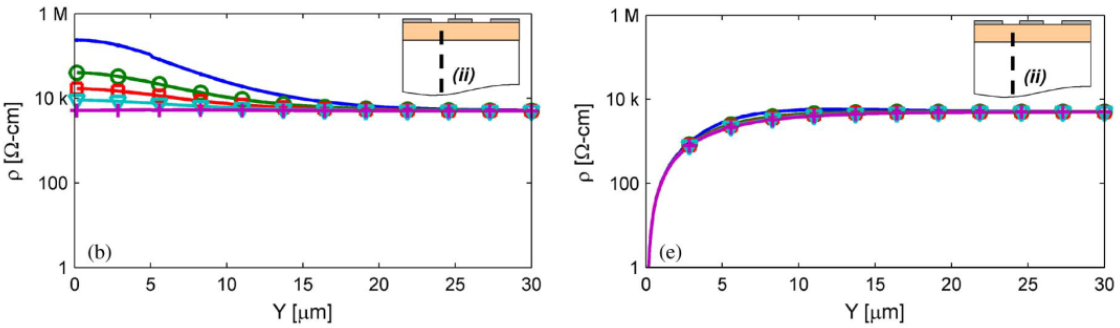


Fig. 2.8: Simulated resistivity profiles in the slot between two condutors of a CPW line, without (left) and with (right) the presence of fixed charges (from [11]). The PSC layer in the first few micrometers is clearly seen on the right-hand side.

Because of the PSC effect, ρ is not uniform for the entire substrate thickness and SOI wafers with very high nominal resistivity behave abnormally. In order to compare different substrates based on a single figure of merit, the *effective resistivity* ρ_{eff} was developed and introduced in [15]. ρ_{eff} is the resistivity that a homogeneous Si ($\varepsilon_r = 11.78$) substrate would need to have to behave like the in-homogeneous

substrate considered, i.e. to have the same RF losses : $\alpha_{inh} = \alpha_{eff}$. It can be extracted from measured line parameters C_{tot} and G_{tot} :

$$\rho_{eff} = \frac{1}{\sqrt{\varepsilon_{r,eff}}} \left(\frac{\varepsilon_{r,eff} - 1}{\varepsilon_{r,Si} - 1} \right) \frac{\sqrt{C_0}}{\varepsilon_0} \frac{\sqrt{C_{tot}}}{G_{tot}} \tag{2.10}$$

Where $\varepsilon_{r,eff}$ and C_0 are the effective dielectric constant and the air-filled capacitance of the effective structure, both of which can be computed following a method developed by Heinrich [16]. Because ρ_{eff} depends on the line capacitance and conductance, it also depends on frequency. When the frequency is high enough, so that the majority carriers in the substrate cannot follow the excitation of the line, resistivity drops. If the substrate is represented as in Fig. 2.9, the capacitance C_{tot}

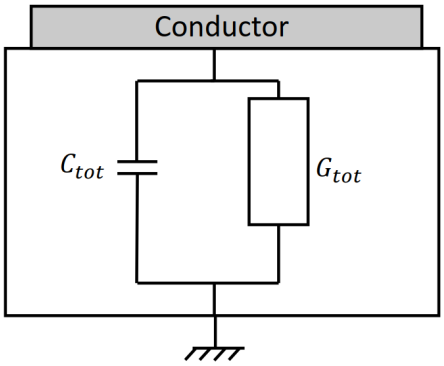


Fig. 2.9: Equivalent lumped element circuit of a SOI substrate.

becomes short-circuited at high frequencies. The critical frequency is given by the relaxation time of majority carriers [4]:

$$\tau = \rho_{si} \varepsilon_{Si} \tag{2.11}$$

At frequencies higher than the relaxation frequency, resistivity can drop by more than one order of magnitude from the value of ρ_{DC}.

Apart from RF losses, the PSC layer also has a detrimental effect on substrate linearity. This was shown in [11] using again CPW lines, highlighting the use of such structures to probe surface properties. The electric field lines going from signal to ground electrode in a CPW line pass through the various regions of the substrate, including the PSC layer. A parallel equivalent circuit, coherent with the usual RLCG description of a transmission line, is shown in Fig. 2.10. In this circuit, both the

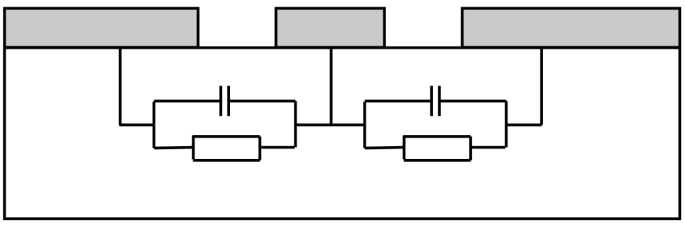


Fig. 2.10: Equivalent circuit between signal and ground electrode of a CPW line.

capacitance C and the conductance G are dependent on the electrode DC bias. When the line is biased in large-signal conditions and the applied voltage changes

substantially, the voltage-dependent substrate properties will introduce harmonic distortion into the signal. When a PSC layer in present, the value of G increases by more than one order of magnitude [11], which in turn increases the power of the generated harmonics.

2.2.3 Suppressing the PSC effets

Many strategies have been proposed to suppress or attenuate the effect of the low-resistivity layer at the substrate surface. The most effective approach is to induce a high density of traps in this region, so that the oxide fixed charge is compensated not by free carriers, but by fixed trapped charges. Furthermore, such traps decrease the carrier mobility in this region, leading to an increase in resistivity. This has the double benefit of bringing RF losses and effective resistivity back to an acceptable level and also reducing the variation of substrate conductance with applied bias, which lowers the level of harmonic distortion.

2.3 Trap-Rich Substrate to limit the PSC effect

The trap-rich substrate, developed in a collaboration of UCLouvain with Soitec, is the most widely used technology for suppression of the PSC effect. It consists in the deposition, under the BOX, of a thin layer of polysilicon. Grain boundary lattice defects trap free carriers and effectively suppress the PSC layer. It is a cheap method which is also compatible with Si foundries processes, making it a very attractive solution, used today in virtually all smartphones on the market [17].

2.3.1 Fabrication

The trap-rich layer implementation step is the first step in the fabrication of the substrate. Because no sensitive devices or functionalities are present on the substrate at that point of the process, the integrity of such precise layers does not have to be taken into account, allowing the use of cheap and fast techniques. A typical fabrication process is described in [18].

A layer of amorphous silicon (α-Si) is deposited using low-pressure chemical vapor deposition (LPCVD), under temperatures of 500-600°C. After this step, the substrate undergoes rapid thermal annealing (RTA) for 120s at 900 °C. This has the effect of crystallizing the α-Si. Another approach consists of a direct deposition of Poly-Si using LPCVD at 625 °C without RTA. The difference lies in the grain size, which is smaller using the crystallization of α-Si. Indeed, the RTA step produces high thermal stresses in the Poly-Si film, leading to small round grains, instead of large columnar grains in as-deposited Poly-Si [18]. Because the traps are originating from the dangling bonds at the grain boundaries, a smaller grain size generates a higher density of traps, and allows to use a thinner passivation layer to achieve the same results (280 nm for crystallized α-Si versus 435 nm for Poly-Si)[19]. A typical thickness of Poly-Si is 350 nm.

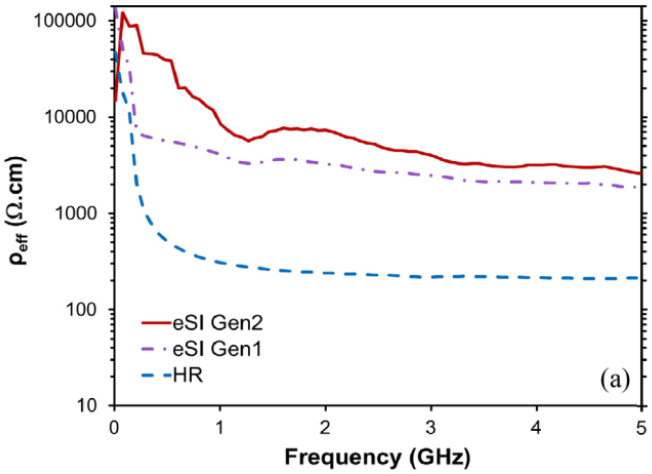
Following the polysilicon layer, the BOX is deposited using low-temperature plasma-enhanced chemical vapor deposition (PECVD), or wet thermal oxidation following the reaction $Si + 2\,H_2O \longrightarrow SiO_2 + 2\,H_2$ at 950 °C. Both steps can be combined : wet thermal oxidation followed by PECVD.

When a substrate undergoes these steps, it is stable enough to go through an entire CMOS process (at temperatures exceeding 900 °C) without losing its integrity or deteriorating its effective resistivity.

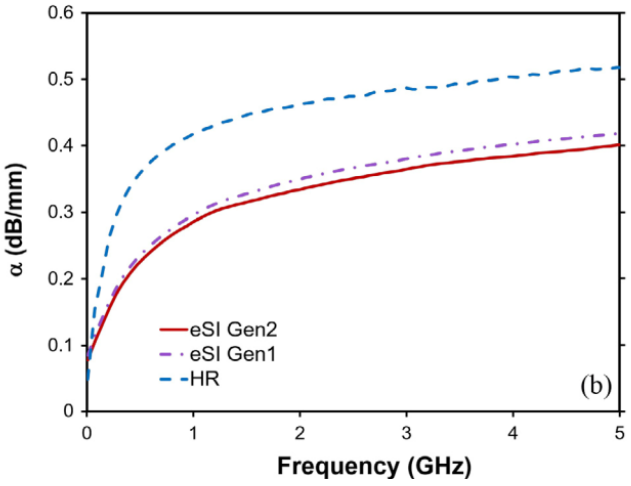
Since the invention of the trap-rich substrate, the technology has been patented and is now made commercially available by Soited under the name "Enhanced Signal Integrity" (eSI™).

2.3.2 Performance

The outstanding performance of the trap-rich technology has been proven for all important figures of merit in RF applications. In figure Fig. 2.11, it can be



(a)



(b)

Fig. 2.11: Effective resistivity (a) and RF loss factor (b) of HR SOI, and two generations of the eSI substrate. Gen 1 (2) has a BOX thickness of 400 nm (200 nm), and Gen 2 has higher nominal resistivity. From [20].

seen that even at high frequencies, the trap-trich technology allows to maintain an effective resistivity of at least $2\,\mathrm{k\Omega\,cm^{-1}}$, which is a sufficiently high value to consider the substrate lossless, as seen on page 17. This high effective resistivity enables losses as low as $0.4\,\mathrm{dB\,mm^{-1}}$ at 5 GHz. Similar results have been found in [10]. The

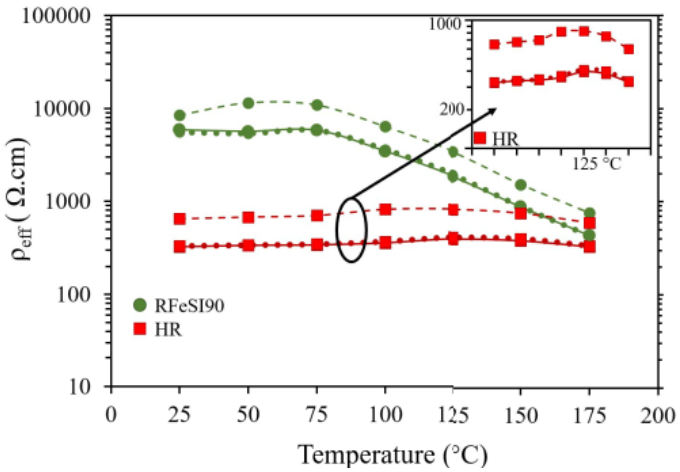


Fig. 2.12: ρ_{eff} variation with temperature, for unpassivated HR and trap-rich subtrates (labelled RFeSI90) (from [10]). Values are for $f = 900\,\text{MHz}$.

temperature behavior of α and ρ_{eff} was also investigated (Fig. 2.12). It can be seen that although there is no significant variation of ρ_{eff} for the HR substrate, a drop in resistivity occurs in the trap-rich substrate after 125 °C. This drop indicates an increase in intrinsic carrier concentration, and is not present in the HR substrate because in the PSC layer, the carrier concentration is already very high. Therefore, a drop is still observed for HR, but at a higher temperature of about 140 °C.

Aside from small-signal parameters, harmonic distortion and crosstalk was also investigated. In Fig. 2.13, it is clear that a reduction of around 25 and 35 dB is

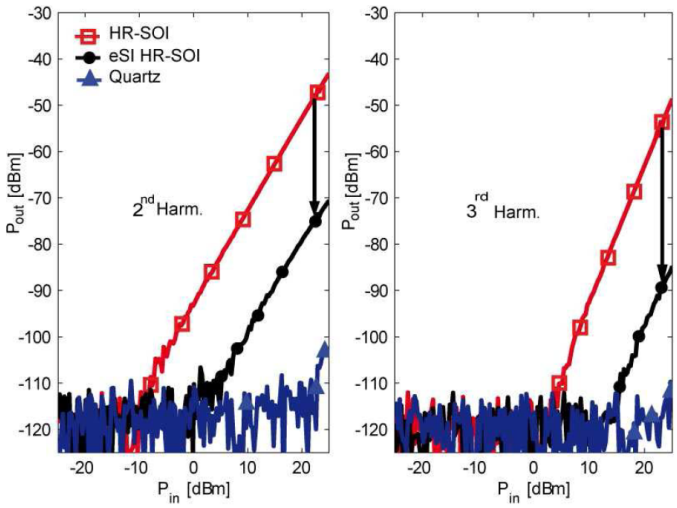


Fig. 2.13: Second and third harmonic output power as a function of first harmonic output power, for HR and TR substrates. Quartz (lossless) substrate measurements indicate the noise floor. From [21].

achieved for the second and third harmonic, respectively, when replacing the HR substrate with the TR. Indeed, the modulation of the carrier distribution by the bias voltage is suppressed with the trap-rich layer, and the substrate behaves like a HR substrate without any PSC layer.

It has been shown in [11] that there is a strong correlation between ρ_{eff} and the

harmonic distortion level : a low effective resistivity is associated with high harmonic distortion. Thus, the temperature dependence of nonlinearities follows that of ρ_{eff}. Indeed, an increase of harmonic level is seen after 125 °C in [10].

2.3.3 Further challenges

In the future, trap-rich technology will have to be scaled to enable integration with advanced technologies such as fully-depleted silicon-on-insulator (FDSOI). In this technology, the BOX is as thin as 25 nm, and the oxide will have to be grown on Poly-Si, which has not yet been done. A specific aspect of the FDSOI MOSFETS is the use of a back-gate contact to control the threshold voltage. This contact is fabricated in the form of a heavily-doped region below the BOX. It is not known if the definition of a quality back-gate contact in trap-rich polysilicon is possible. This will be explored in the following section.

Furthermore, characterizing the trap-rich layer, in terms of trap density and energy distribution, is a difficult task. Polysilicon characterization techniques exist but have been developed for low-trap density materials, whereas the trap density is willingly very high in trap-rich substrates.

2.4 FD SOI technology on a trap-rich substrate

Future developments of MMICs could lead to co-integration of RF and digital functions on the same chip. In recent years, ultra-thin body and buried oxide (BOX) fully depleted SOI (FD SOI) technology is seen as a promising approach to further reduce device dimensions and fulfill the International Technology Roadmap for Semiconductors (ITRS) [22]. In UTBB FD SOI, the BOX is as thin as a few tens of nanometers, and the top silicon thickness is usually below 10 nm (see Fig. 2.14). This allows MOSFETs built on this platform to function in volume inversion. FD SOI transistors do not show any kink effect, as opposed to partially-depleted SOI (PD SOI) MOSFETs. The body effect parameter is close to 1, limiting this effect as well. Furthermore, its steep subtreshold characteristics are excellent for digital uses. UTBB also reduces the short channel effects, and presents excellent analog RF performance [1, 23].

One attractive property of FD SOI technology is the presence of a ground plane (GP), of thickness comparable with BOX thickness (around 10 nm)contact located under the buried oxide, as seen in Fig. 2.14. This quasi double-gate architecture allows a dynamic threshold voltage, and an improvement of analog performance [24, 25, 26], by biasing the back-gate (port 3 in Fig. 2.15) as a function of the front gate :

$$V_{bgn} = k \cdot V_g \tag{2.12}$$

Where k can be as high as 25. The GP contact, a heavily doped region, creates a parasitic PN junction with the substrate accompanied by a nonzero leakage current flowing to the substrate. This PN junction is shown in Fig. 2.15, and is always reverse biased in order to isolate the device from the substrate [27]. For integration on RF-SOI substrates with trap-rich technology, this GP contact would have to be implemented in the trap-rich polysilicon layer, as represented in Fig. 2.16. While the GP contact has been proven to improve the I_{on}/I_{off} ratio on conventional substrates

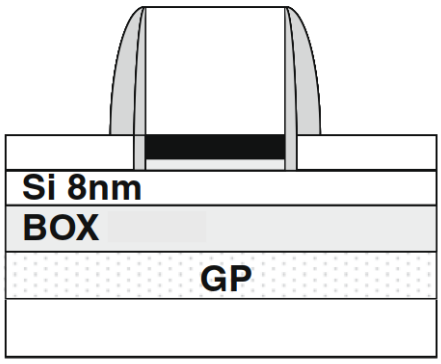


Fig. 2.14: Schematic of a UTBB FDSOI MOSFET with ground plane contact (from [24])

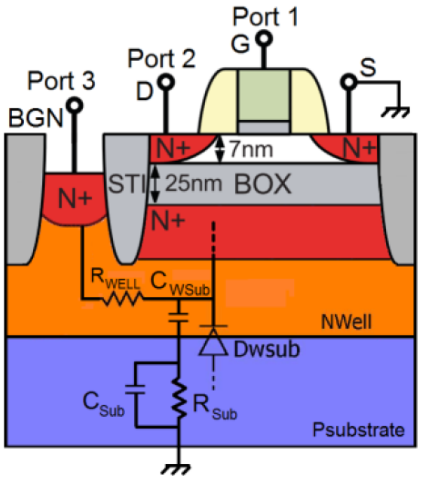


Fig. 2.15: Cross-section of a NMOS FD SOI transistor, where the location of the parasistic PN junction between substrate and ground plane is shown (from [6])

[25], there has been no study of its effect on digital performance when used with a trap-rich substrate. In this section, a literature review based on leakage current in

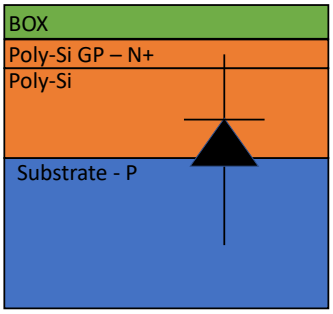


Fig. 2.16: Representation of the parasitic PN junction between GP implant and the substrate, when a layer of trap-rich Poly-Si is present below the BOX.

thin-film transistors (TFT) is presented, as well simulation results of PN junctions built in polysilicon.

2.4.1 Leakage current in TFTs

To understand the leakage mechanism in FD SOI devices when the GP is implemented in Poly-Si, the focus is shifted to TFTs. An example of TFT architecture is shown in Fig. 2.17.

The fabrication process of a TFT is as follows. First, a thin film of Poly-Si is deposited on a quartz substrate by low-pressure chemical vapor deposition. The gaseous precursor is silane SiH_4, which decomposes into Si and H_2 at high temperatures, typically 600 °C. The thickness of this film is of the order of 100 nm. Then, the polysilicon is oxidized to form the gate oxide, and the gate electrode is grown on top. Source and drain regions are doped at the end of the process, then

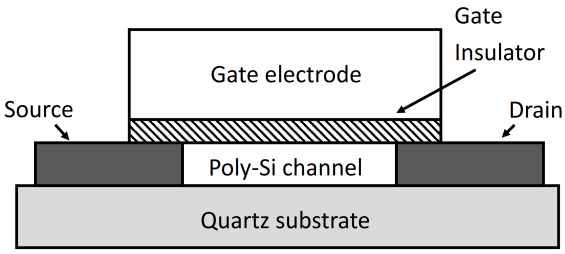


Fig. 2.17: Schematic of a thin-film transistor.

annealed. Typical doses are $3 \times 10^{15}\,\mathrm{cm}^{-2}$ with energies of 100 keV [28]. The active channel is left undoped, or slightly n- or p-doped.. TFTs behave in the same way as MOSFETs, but using polysilicon allows TFTs to be fabricated on glass substrates and on very large areas, making them attractive for use in display panels.

Because their use in display applications, the mechanisms of off-leakage current of TFTs have been widely investigated [28, 29, 30, 31]. When biased in off regime while high voltage is applied at source/drain electrodes, the electric field around the drain region becomes important. This creates a pseudo-PN junction between channel and drain with intense electric field near the drain. The mechanisms behind the current in this region probably also come at play in a polysilicon diode, as the situations are similar. Besides intense electric field, the high trap density in polysilicon grain boundaries also plays an important role, as will be seen in what follows.

As seen in Fig. 2.18, it has been observed that the leakage current is temperature-dependent (because the generation rate of carriers is), and can be fitted to an Arrhenius law :

$$I_{off} \propto \exp \frac{-E_a}{k_B T} \tag{2.13}$$

Where E_a, the activation energy, is the slope of an Arrhenius plot such as the one in Fig. 2.18. It provides information about the conduction mechanism, because it reflects the energy needed for carriers to participate in electrical current. Material parameters were not specified in [29], but typical doping levels for drain regions in TFT are of the order of $1 \times 10^{19}\,\mathrm{cm}^{-3}$, while the channel is very lightly doped (around $1 \times 10^{11}\,\mathrm{cm}^{-3}$) - or even left undoped. It is clear from Fig. 2.19 that E_a is bias-dependent. This indicates that as the bias changes, electrons (holes) are more or less easily promoted to the conduction (valence) band.

Phonon-assisted tunneling with Poole-Frenkel barrier lowering is the most widely accepted mechanism governing the reverse current in TFTs. It consists in the tunneling of an electron from a trap state to the conduction band. Because the trap states are located in the bandgap, the tunneling probability is higher from a trap state than from a state in the valence band (the energy barrier is lower). Because of the high density of traps in Poly-Si, trap-assisted tunneling is predominant, as opposed to cristalline silicon where this situation does not occur easily. In this mechanism, the tunneling probability depends on the band structure, which in turn depends on bias. In Fig. 2.20, situation A corresponds to a small bias, where the band structure is only weakly bent. The generation rate of the electron-hole pair, activated from the trap state, is proportional to $\exp -E_a/k_B T$, where the activation energy E_a corresponds to the bandgap. When a high drain bias is applied (reverse bias, B in Fig. 2.20), the band in the drain region becomes lower and the energy difference between trap states located at midgap and the conduction band becomes

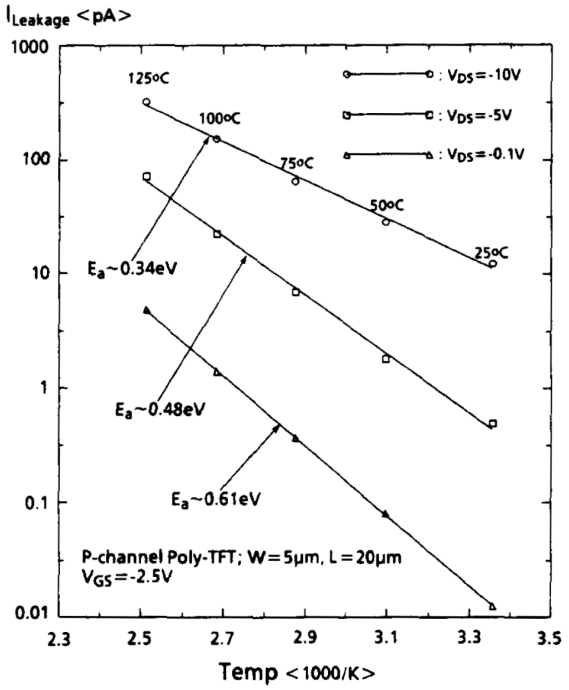


Fig. 2.18: Arrhenius plot of leakage current for a p-channel Poly-Si TFT (from [29]).

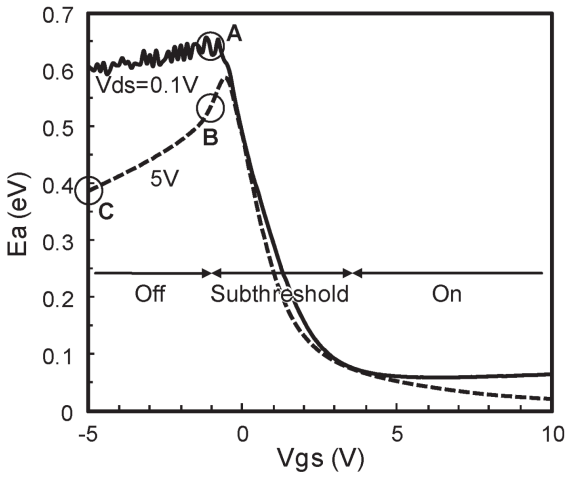


Fig. 2.19: Drain and gate bias dependence of I_{off} activation energy (from [31]).

lower. As a result, the tunneling probability is higher. This description also implies that the tunneling probability varies with the energy distribution and density of traps in the bandgap [29, 32].

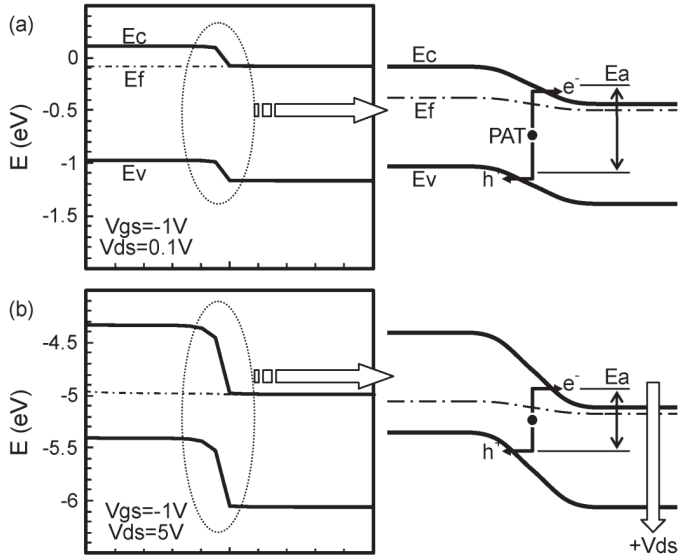


Fig. 2.20: Band diagram in the drain-channel region of a reverse-biased TFT (from [31]).

Furthermore, the Poole-Frenkel (PF) effect comes into play. At high electric fields, the potential barrier through which the electrons have to tunnel is lowered, and this effect is quantified by :

$$\Delta E_{pf} = \left(\frac{q^3 E}{\pi \varepsilon}\right)^{1/2} \tag{2.14}$$

Where E is the electric field, q is the electron charge, and ε is the permittivity of the material [32]. It was shown in [32] that inclusion of the PF effect is necessary in materials such as Poly-Si, where this effect increases the generation rate by nearly one order of magnitude.

2.4.2 Leakage current in polysilicon diodes

These two elements (phonon-assisted tunneling from a trap state and the PF barrier lowering) have been applied to model PN junctions in polysilicon [33]. Generally, the Shockley-Read-Hall (SRH) model is used to describe generation and recombination of carriers in semiconductor devices. However, due to the presence of a large number of traps in polysilicon devices and the considerable influence of high electric fields in the space-charge region of PN junction, other models are needed and were developed [34]. The model in [33] is based on an analytical expression of

the carrier emission rate, taking into account tunneling and the PF effect :

$$e'_n = e_n \left\{ \exp\left(\frac{\Delta E_i}{k_B T}\right) + \frac{1}{k_B T} \int_{\Delta E_i}^{E_i} \exp\left[\frac{E}{k_B t} - \left(\frac{E}{k_B T}\right)^{3/2} \times \frac{4\sqrt{m^* k_B T}}{3qhF} \left(1 - \left(\frac{\Delta E_i}{E}\right)^{5/3}\right)\right] dE \right\} \tag{2.15}$$

In this case, the electric field is denoted F, m^* is the effective mass, h the Planck constant, k_B the Boltzmann constant, and E_i is the ionization energy of traps ($E_i = E_c - E_t$, where E_t is the energy level of the considered trap state). The barrier lowering due to the PF effect is taken into account by ΔE_i. It is clear that this expression is only valid for a single trap energy, and not very useful for a continuous distribution of traps in materials such as Poly-Si. However, the effect of trap energy level only becomes significant at electric fields higher than $1 \times 10^6\,\mathrm{V\,cm^{-1}}$ (see Fig. 2.21), so in [34], it is assumed that E'_n/e_n is independent of trap energy. For these moderate fields, which will not be exceeded in PN junctions, Eq. 2.15 can

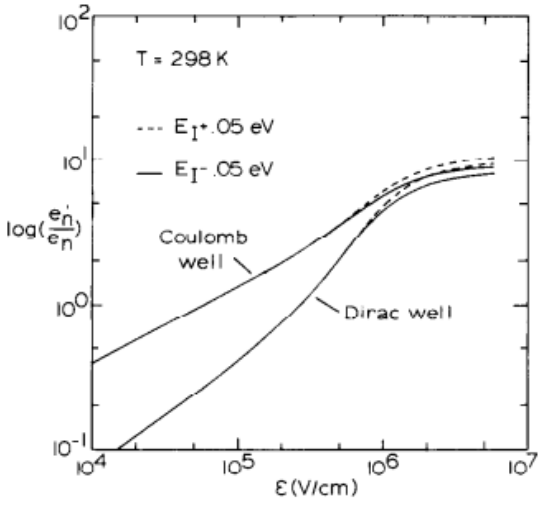


Fig. 2.21: Dependence of carrier emission rates on trap energy. Here, E_i is for a trap at mid-gap ($E_i = E_g/2$) (from [34]).

be approximated by :

$$\frac{e'_n}{e_n} = \exp\left(\frac{F}{F_0}\right)^n \tag{2.16}$$

Where F_0 and n are fitting parameters. This expression proves itself useful, because it can be used to adapt the SRH model by changing the carrier lifetime.

In the SRH model, the net recombination rate is written as :

$$U = \frac{np - n_1 p_1}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{2.17}$$

Where $n_1 = N_D \exp\left(E_C - E_{tD}\right)/k_B T$, with E_{tD} the trap energy, and $\tau_{n,p}$ is the carrier lifetime, usually expressed as :

$$\tau_{n,p} = \left(\sigma_{n,p} v_{th} N_t\right)^{-1} \tag{2.18}$$

Where the capture cross-section, the thermal velocity, and the density of traps appear. The field effect will change (increase) the trap capture probability, and thus decrease the lifetime (by increasing the cross-section and emission rate). This can be written as :

$$\tau_{n,p} = \tau_{0n,p} \exp\left(-\frac{F}{F_0}\right)^n \tag{2.19}$$

By fitting the parameters F_0 and n as a function of temperature only, good agreement with experimental values for reverse bias was obtained in [33]. However, their results are obtained considering a density of grain boundary traps N_t of $5 \times 10^{12}\,\mathrm{eV\,cm^{-2}}$. It is not clear if this model holds well for the very high density of traps in trap-rich Poly-Si, where the mid-gap trap level approximation is perhaps too strong and the continuous energy distribution of the trap energy has to be taken into account.

2.4.3 Simulation of PN junctions in a polysilicon layer

In the case of trap-rich integration in FD SOI technology, the PN junctions at the backgate would be heterojunctions, with trap-rich polysilicon on one side and cristalline silicon on the other side. In order to understand how these junctions behave, and especially characterize their leakage current, Silvaco Atlas current-voltage simulations on simple PN junctions have been done. The following models were used by Atlas in the following simulations :

- Bandgap narrowing
- Klaassen mobility model. This complete model takes into account the doping concentration influence on mobility, as well as carrier concentration.
- Field-dependent mobility was also taken into account.
- A modified Shockley-Read-Hall recombination model was used, which takes into account band-to-band tunnelling as well as the Poole-Frenkel effect. Auger recombination was also included.
- Impact ionization, although it is not expected to take place since the electric field is low.

Initially, I-V simulations with bias ranging from -2 to +2 V are done for four different configurations, represented on Fig. 2.22. The trap and doping parameters for these initial simulations are given in Table 2.1. The trap distribution parameters are those usually used in trap-rich simulations, and have been proven to match measurements of different fabricated substrates in [35]. Back-gate doping usually has a peak concentration between 1 and $5 \times 10^{18}\,\mathrm{cm^{-3}}$ [36]. It was fixed at $1 \times 10^{18}\,\mathrm{cm^{-3}}$ but as will be seen, it is so important compared to the substrate doping that small variations are not significant.

For these parameters, the reverse bias currents are shown in Table 2.2. Clearly, the introduction of polysilicon on one or both sides of the junctions increases the reverse current by two orders of magnitude thanks to additional mechanisms such as band-to-band tunneling due to large trap density, as expected.

Because the reverse current is largely due to traps, it was also investigated if the trap distribution had an influence on the amplitude of the current. A single trap

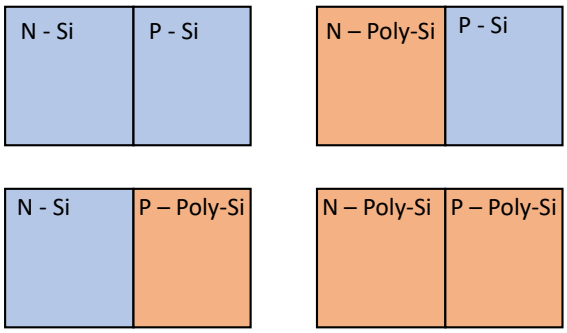


Fig. 2.22: Different configurations of simulated P-N junctions.

Parameter	Value
Doping (same on both sides)	$1 \times 10^{18}\,\mathrm{cm}^{-3}$
Trap distribution	Tail
Density of acceptor-like states at conduction band edge	$1 \times 10^{22}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$
Density of donor-like states at valence band edge	$1 \times 10^{22}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$
Characteristic decay energy (acceptor and donor-like states)	$0.033\,\mathrm{eV}$

Table 2.1: Initial simulation parameters.

Configuration	Reverse current
N (Si) - P (Si)	$1.09 \times 10^{-16}\,\mathrm{A\,\mu m}^{-1}$
N (Si) - P (Poly-Si)	$1.26 \times 10^{-14}\,\mathrm{A\,\mu m}^{-1}$
N (Poly-Si) - P (Si)	$1.16 \times 10^{-14}\,\mathrm{A\,\mu m}^{-1}$
N (Poly-Si) - P (Poly-Si)	$2.18 \times 10^{-14}\,\mathrm{A\,\mu m}^{-1}$

Table 2.2: Reverse currents for different configurations of PN junction, at a bias of $-2\,\mathrm{V}$.

level (donor and acceptor) was defined, and its energy level was varied from the conduction band or valence band to midgap for acceptor or donor traps, respectively. Results are shown in figure 2.23. Midgap traps are the most efficient at facilitating

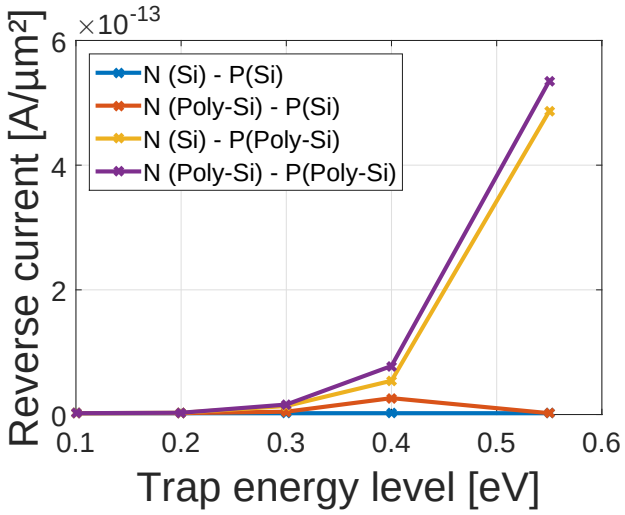


Fig. 2.23: Reverse current of PN junctions biased at $-2\,\mathrm{V}$. A symmetrical doping of $1 \times 10^{13}\,\mathrm{cm}^{-3}$, and trap density of $1 \times 10^{16}\,\mathrm{cm}^{-3}$ were used. Trap level is measured from the conduction band for acceptor traps and from the valence band for donor traps.

trap-assisted tunneling, and indeed the reverse current associated with these traps is higher than for traps closer to the bands. Even though the variation is small, the trap distribution has an influence of current, and these PN junctions could perhaps be investigated as trap distribution characterization tools. Furthermore, the type (N or P) of the polysilicon is seen to have an influence as well, which could be explained by better efficiency of the various mechanisms for holes or electrons.

In a practical case, the doping levels would however not be symmetrical. Indeed, the high-resistivity substrate has a very low P doping concentration (around $4.8 \times 10^{12}\,\mathrm{cm}^{-2}$ for a $3\,\mathrm{k\Omega\,cm}$ substrate) whereas the N implant for the backgate is very heavily doped. The consequence of this non-symmetric geometry is that the depletion junction will mainly extend on the P doped side, the substrate, which has the lowest doping. Because it is in the depletion region that recombination mechanisms occur and that the electric field is high, it is also there that the physical properties matter. Simulation results are displayed in Table 2.3. As expected, the

Configuration	Reverse current
N (Si) - P (Si)	$5.61 \times 10^{-14}\,\mathrm{A\,\mu m}^{-2}$
N (Poly-Si) - P (Si)	$5.42 \times 10^{-14}\,\mathrm{A\,\mu m}^{-2}$
N (Si) - P (Poly-Si)	$5.60 \times 10^{-13}\,\mathrm{A\,\mu m}^{-2}$
N (Poly-Si) - P (Poly-Si)	$5.60 \times 10^{-13}\,\mathrm{A\,\mu m}^{-2}$

Table 2.3: Reverse currents for different configurations of PN junction, at a bias of $-2\,\mathrm{V}$. The doping is $1 \times 10^{17}\,\mathrm{cm}^{-3}$ for the N zone, and $4.8 \times 10^{12}\,\mathrm{cm}^{-3}$ for the P zone. A tail distribution with parameters of Table 2.1 was used for polysilicon.

material in the P doped region defines the reverse current, because it is in this region that electric field is high.

From these first simulations, it appears thus that defining the backgate contact in polysilicon is not a problem in terms of leakage current, as long as substrate doping is low. However, in these simulations interface phenomena have not been considered, and could be of importance. Furthermore, the entire thickness of polysilicon is defined as doped here, which is not the case in real substrates as the GP implant is only 10 nm thick, but this in not expected to have a significant influence.

Chapter 3

Buried P-N junctions

As an alternative solution for the reduction of parasitic surface conductance effects, a new method was proposed very recently by the RF SOI group in [37]. It consists of the implantation, below the BOX, of alternating P-N implants. The concept is represented on Fig. 3.1. Highly resistive depletion regions are created

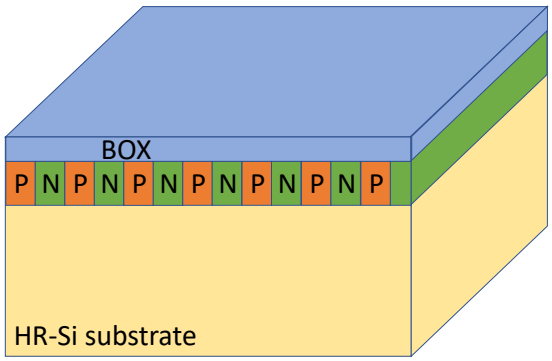


Fig. 3.1: Schematic of the P-N buried implant layer under the BOX.

at the boundaries of the implants, making the formation of the inversion layer at the substrate surface more difficult. This solution has the advantage of being fully compatible with CMOS technology, by relying solely on crystalline Si and ion implantation. In this chapter, the method is developed in detail, and the carrier behavior in such a substrate is analyzed thoroughly. Experimental results are also shown, confirming the potential of this concept.

3.1 PN Junctions : Generalities

When a P doped semiconductor is brought in contact with a N doped piece of the same material, a PN junction is created. The N region is characterized by a high density of free electrons (in the conduction band) due to a high donor impurities concentration, whereas a high concentration of holes in the valence band are present in the P doped region. Because these two regions are in contact, diffusion forces will induce a flow of electrons towards the P doped region, and similarly in the opposite direction for the holes. These opposite flows of carriers lead to important

amounts of recombination near the interface between the two regions, the so-called metallurgical junction. When electrons and holes recombine and cancel out their electric charge, they leave behind ionized impurities (see Fig. 3.2). The impurities are positively charged in the N region, and negatively charged in the P region. They are immobilized as part of the lattice, and thus remain charged in the absence of a mechanism for charge compensation. The region where a fixed charge exists and in which the concentration of free carriers is low is called the *depletion*, or *space-charge* region, to emphasize the fact that a net charge is present.

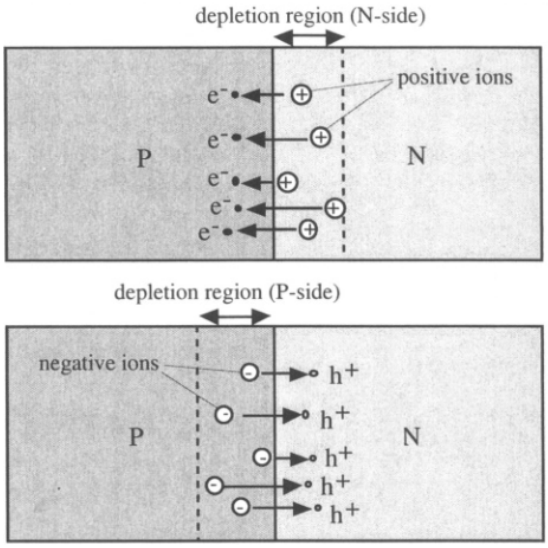


Fig. 3.2: Creation of a depletion region in a PN junction (from [38]).

3.1.1 PN junction at equilibrium

Because the sign of the electrical charge at both sides of the depletion region is different, an electrical field is induced across the junction. This field, at equilibrium, counterbalances the diffusive flow by creating a junction potential, equal to the band curvature. Indeed, because the Fermi level must be homogeneous in a material at equilibrium, conduction and valence bands curve across the junction, as shown in Fig. 3.3. The junction potential is given by the difference between the original Fermi levels of the P and N doped materials, $E_{FP} - F_{FN}$:

$$\phi_0 = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{3.1}$$

Where N_A and N_D are the doping levels (in cm^{-3}) and n_i is the intrinsic carrier concentration.

Characterization of a PN junction is done by solving Poisson's equation, which reads (in one dimension):

$$\frac{d^2\phi(x)}{dx^2} = -\frac{q}{\varepsilon_s}\left(p - n + N_D^+ - N_A^-\right) \tag{3.2}$$

Where p and n are the free carriers concentration, and N_D^+ and N_A^- are the unbalanced ionized impurities concentrations. The Poisson equation can only be solved

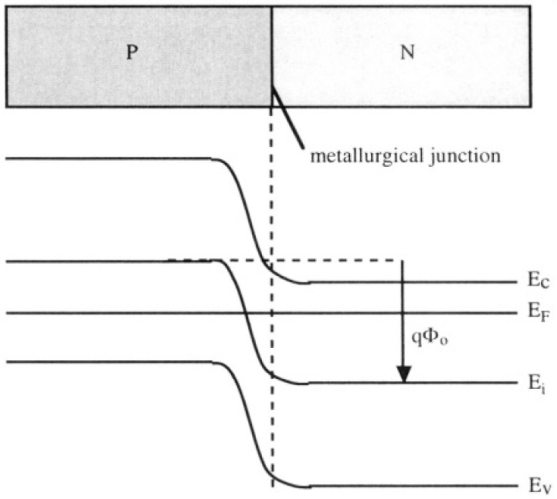


Fig. 3.3: Curvature of the energy bands in a PN junction (from [38]).

analytically under approximations. The depletion approximation states that the charge in the depletion region is only due to ionized impurities and that the contribution of free carriers is negligible. Furthermore, it supposes that the charge is a step function : far in the N and P regions, the charge density is 0 (these regions are called the *quasi-neutral regions*). The depletion region on the N-side has uniform charge density qN_D, and on the P-side, qN_A. The depletion region has a fixed length, $l_{n0} + l_{p0}$, where l_{n0} and l_{p0} is the extension on the N and the P side, respectively. Under the depletion approximation, the length of the depletion region on both sides can be computed :

$$l_{p0} = \sqrt{\frac{2\varepsilon_s}{q}\frac{\phi_0 N_D}{N_A(N_A+N_D)}} \tag{3.3}$$

$$l_{n0} = \sqrt{\frac{2\varepsilon_s}{q}\frac{\phi_0 N_A}{N_D(N_A+N_D)}} \tag{3.4}$$

The extension of the space-charge region is thus a function of the doping level, as would be expected : for a fixed charge to be compensated on the other side, the length of material to be depleted has to be larger if it is lowly doped. This is verified by taking, for example, $N_D \gg N_A$:

$$l_{p0} \cong \sqrt{\frac{2\varepsilon_s}{q}\frac{\phi_0}{N_A}} \tag{3.5}$$

$$l_{n0} \cong \sqrt{\frac{2\varepsilon_s}{q}\frac{\phi_0}{N_D}} \tag{3.6}$$

Clearly, $l_{p0} > l_{n0}$, and the depletion region extends more into the lowly-doped region.

As a consequence of the depletion approximation, the electric field is nonzero only in the depletion region, and its maximal value is at the metallurgical junction.

3.1.2 Biased PN junction

Applying a continuous potential difference across a PN junction will change the band curvature and thus the carrier behavior in the material. The junction potential when a voltage V_a (positive if a positive voltage is applied to the P side) changes as a result :

$$\phi = \phi_0 - V_a \tag{3.7}$$

The voltage is considered to be entirely applied on the depletion zone (i.e., there is no voltage drop across the quasi-neutral regions). Using this updated expression of the potential, the depletion lengths, also bias dependent, can be adapted :

$$l_p = \sqrt{\frac{2\varepsilon_s}{q}\frac{(\phi_0 - V_a)N_D}{N_A(N_A + N_D)}} \tag{3.8}$$

$$l_n = \sqrt{\frac{2\varepsilon_s}{q}\frac{(\phi_0 - V_a)N_A}{N_D(N_A + N_D)}} \tag{3.9}$$

$$l_p + l_0 = \sqrt{\frac{2\varepsilon_s}{q}\frac{(\phi_0 - V_a)(N_A + N_D)}{N_A N_D}} \tag{3.10}$$

The depletion length as expressed in Eq. 3.10 is bias dependent : a reverse bias ($V_a < 0$) will increase it, while a forward bias will reduce it.

Forward biasing the junction ($V_a > 0$) also allows a current through the junction. Indeed, if the potential barrier is lowered, the diffusion is not totally counterbalanced by the electric field, and carriers can flow from one side of the junction to the other. In this situation, holes (electrons) are injected and diffuse into the N (P) doped region, where they undergo recombination with electrons (holes), the majority carriers in these regions. Majority carriers are continuously supplied by the bias electrodes.

3.1.3 Equivalent capacitance

When the PN junction is subjected to an alternative small-signal voltage, the depletion charge changes over time, giving rise to a capacitive effect. The equivalent *transition capacitance* per unit cross-section can be derived using the definition of a capacitance :

$$\begin{aligned} C_T = \left|\frac{dQ}{dV_a}\right| = \left|\frac{d(ql_nN_D)}{dV_a}\right| &= qN_D\sqrt{\frac{2\varepsilon_s}{q}\frac{N_A}{N_D(N_A+N_D)}}\frac{1}{2\sqrt{\phi_0 - V_a}} \\ &= \sqrt{\frac{q\varepsilon_s}{2}\frac{N_AN_D}{N_A+N_D}}\frac{1}{2\sqrt{\phi_0 - V_a}} \end{aligned} \tag{3.11}$$

We can insert Eq. 3.10 to write C_T as a parallel plate capacitance :

$$C_T = \frac{\varepsilon_s}{l_n + l_p} \tag{3.12}$$

The charge variations used to define C_T are due to majority carriers moving in and out of the depletion zone : this capacitance can thus be considered to be frequency independent.

Furthermore, when the junction is forward biased, excess injection of minority carriers in the quasi-neutral zone takes place. These charges create another capacitance, called *diffusion capacitance* C_D, made of the sum of the 2 capacitances in the 2 quasi-neutral regions. For reverse bias as well as small forward bias, the transition capacitance dominates, but when the injection is significant, at strong forward bias, $C_D \gg C_T$

3.2 Carrier Distribution

The substrate structure was simulated using the TCAD Software Silvaco Atlas [39], which solves semiconductor equations in user-defined structures with finite-element methods. A typical SOI substrate was simulated, with the addition of the buried implants below the BOX. On top of the BOX, a CPW line is defined as simple electrodes (i.e. as perfect conductors), and a backside metallization is also included. The backside metallization is combined with a high lumped biasing resistance. Indeed, as the simulated substrate is thinner than a practical one (the observed phenomena occur close to the surface), undesirable effects of the backside must be avoided. In Fig. 3.4 the electron distribution is shown, for the simulation parameters displayed in Table 3.1. The doped implants were defined by first creating a uniformly P doped layer, then defining the N-doped implants where the junctions are desired. The

Parameter	Value
Substrate thickness	$100\,\mu m$
BOX thickness	$400\,nm$
Oxide/silicon interface fixed charges	$1 \times 10^{11}\,cm^{-2}$
Bulk doping level (P)	$4.8 \times 10^{12}\,cm^{-3}$ ($\sim 3\,k\Omega\,cm$)
Width of 1 implant	$1\,\mu m$
Depth of the buried doped layer	$100\,nm$
N implant doping level	$1.5 \times 10^{17}\,cm^{-3}$
P implant doping level	$1.5 \times 10^{17}\,cm^{-3}$
Extension under signal electrode	$0\,\mu m$
Extension under ground electrode	$0\,\mu m$
CPW signal electrode width	$26\,\mu m$
CPW electrode spacing	$12\,\mu m$
CPW ground electrode width	$75\,\mu m$
Metal workfunction	$4.7\,V$

Table 3.1: Initial simulation parameters

alternatively doped regions can clearly be seen below the spacing between electrodes. In a 3 dimensional structure, the implants would extend parallel to the electrodes, such that the field lines are always perpendicular to the doping profile. Because the electric field is most important in the space between the electrodes, the implants were first simulated in that zone only, where it is most important to counteract the PSC effect. On figure Fig. 3.5, carrier concentration along a horizontal cutline is shown. The depletion regions can clearly be seen, however their size is limited due to the high doping level.

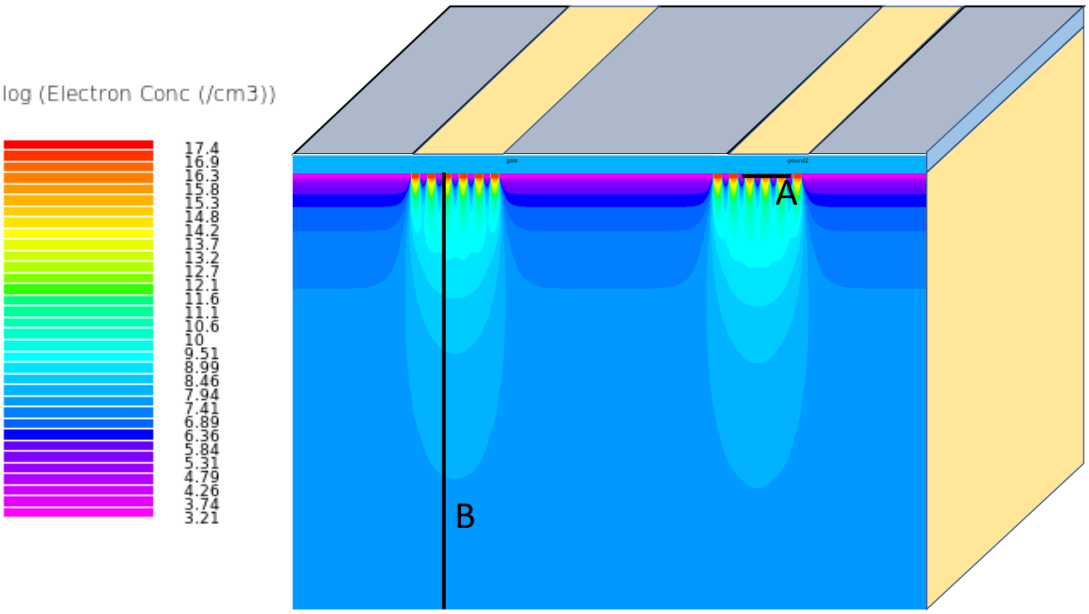


Fig. 3.4: Electron concentration profile in a buried-implant substrate. The represented zone is 10 µm deep and 80 µm wide. Cutlines A and B are represented on Fig. 3.5 and Fig. 3.6, respectively.

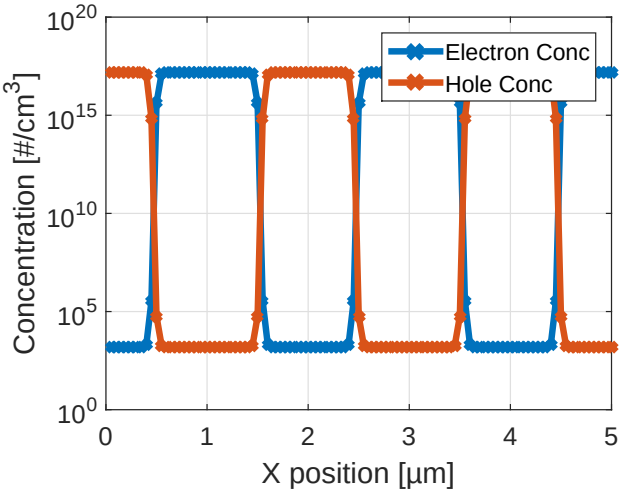


Fig. 3.5: Carrier concentration profile perpendicular to the implant profile (A in Fig. 3.4).

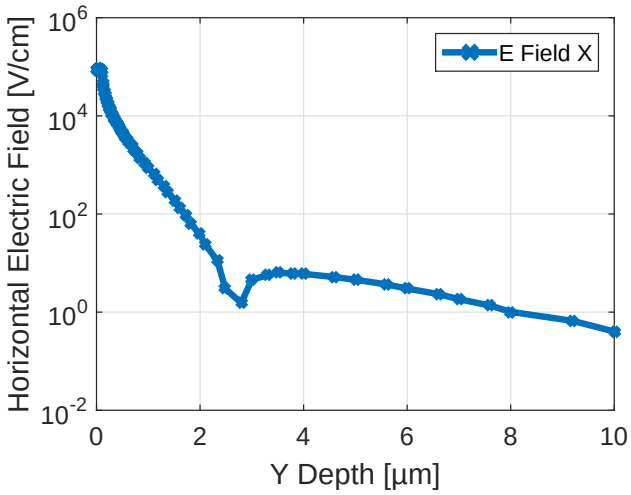


Fig. 3.6: Horizontal electric field as a function of substrate depth (cutline B in Fig. 3.4).

The influence of the buried implants is not limited to the implant region, as seen on Fig. 3.4. Indeed, because of boundary effects, the (horizontal) electric field is not only strong in depletion regions, but also below them, as shown on the cutline in Fig. 3.6, where the field is seen to be decreasing rather slowly with depth.

3.3 Doping Level

Following the theory of PN junctions, the depletion width should vary with the doping level. When both P and N doping levels are equal, equation Eq. 3.10 becomes, for an unbiased junction :

$$l_p + l_n = \sqrt{\frac{2\varepsilon_s}{q}\frac{2\phi_0}{N_{A,D}}} \tag{3.13}$$

Thus by lowering the doping level, depletion regions should become larger. However, the size of the implants is limited, and total depletion length should not exceed it. Indeed, if $l_n + l_p > 1\,\mu\text{m}$ no quasi-neutral regions can exist and the junctions disappear. As seen on Fig. 3.7, the critical doping level lies between $1 \times 10^{15}\,\text{cm}^{-3}$ and $1 \times 10^{16}\,\text{cm}^{-3}$. Aside from pure dimensional restrictions, the doping level also has to be high enough to prevent the formation of an electron-rich layer at the substrate surface. These theoretical guidelines are confirmed by simulations, where already at $N_{A,D} = 2 \times 10^{16}\,\text{cm}^{-3}$ the hole concentration never recovers its nominal value in the center of the P implants. For these reasons, a dopant concentration of $1.5 \times 10^{17}\,\text{cm}^{-3}$ was used in the simulations of chapter 4.

3.4 Effect on resistivity

To gain a better understanding of how buried implants help to counter the PSC effect, local resistivity can be calculated in the substrate. Resistivity is defined as the inverse of the conductivity σ [40]:

$$J = \sigma E \tag{3.14}$$

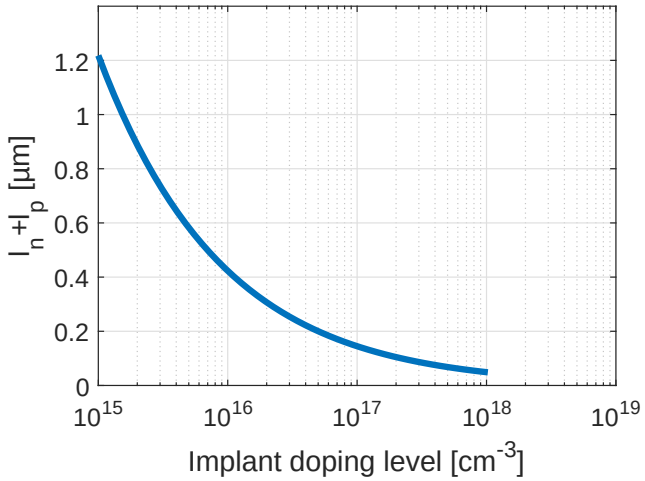


Fig. 3.7: Theoretical depletion length variation with doping level, calculated with Eq. 3.13.

Where J is the current density and E the electric field. J is given by $J = -qnv_n + qpv_p$ where n, p are the electron and hole concentrations, and v_n, v_p are the electron and hole drift velocities. Drift velocities can be expressed as :

$$\begin{aligned} v_n &= -\frac{q\tau_n}{m_e^*}E = \mu_n E \\ v_p &= \frac{q\tau_p}{m_h^*}E = \mu_p E \end{aligned} \tag{3.15}$$

Where $m_{e,h}^*$ are effective masses and $\tau_{n,p}$ are carrier relaxation times. The quantity μ is mobility, linking drift velocity to electric field. Combining Eq. 3.15 and Eq. 3.14 an expression of σ is obtained :

$$\sigma = \rho^{-1} = q(n\mu_n + p\mu_p) \tag{3.16}$$

This important equation shows that there are two approaches to increase local resistivity : reducing mobility or reducing carrier concentration. The second mechanism is used here, where a depletion zone forces both n and p to be low. In Fig. 3.8, a resistivity profile was computed for the carrier concentrations in Fig. 3.5. Mobilities (not uniform over space) are also extracted from the same Atlas simulation. As expected, the implants themselves have very low resistivity, on the order of 100 mΩ cm. They are separated by depletion regions where hole and electron concentrations are low. These zones have resistivity as high as 1 MΩ cm.

From these considerations, it can be expected that an increase of the depleted space below the BOX leads to an overall more resistive substrate. This could be done by making the implants smaller, or by artificially increasing the depletion width by reverse biasing the junctions.

3.5 Equivalent Circuit

As explained earlier, the succession of implants is characterized by low resistivity quasi-neutral regions put in series with very highly resistive depletion regions. The

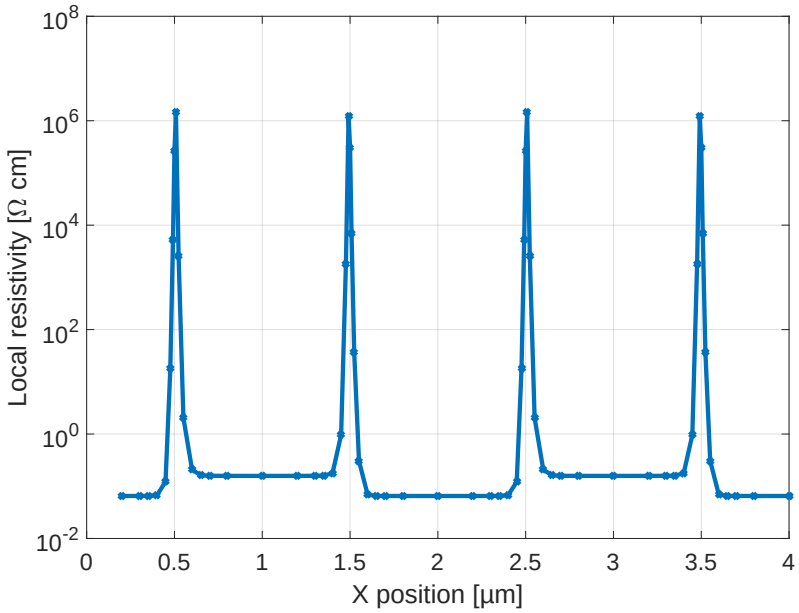


Fig. 3.8: Resistivity profile calculated with Eq. 3.16 perpendicular to the implant doping profile (cutline A in Fig. 3.4).

conductive regions can be modeled as a lumped conductance of resistivity ρ_{QN} (Eq. 3.17), and the space charge regions can be represented as capacitances (see subsection 3.1.3).

$$\rho_{QN} = (q(n\mu_n + p\mu_p))^{-1} \tag{3.17}$$

In Eq. 3.17, either n or p will be 10 orders of magnitude larger than the other, and ρ_{QN} will be very low. The impedance of the capacitive regions will be given by :

$$Z = (j2\pi f C_T)^{-1} = \frac{l_n + l_n}{j\varepsilon_s 2\pi f} \tag{3.18}$$

Thus, the depletion length has a direct influence on the impedance of C_T.

In Fig. 3.9 the equivalent circuit between signal and ground electrode is shown. The substrate capacitance and conductance are put in parallel with a series succession of depletion capacitances and quasi-neutral zone conductances (grey zone). In a classical HR substrate, the PSC layer would be represented by a high conductance below the BOX.

This circuit allows a prediction of small-signal behavior. At low frequencies, the impedance of C_T is high, and the CPW line sees the substrate properties (C_{sub}, G_{sub}), and ρ_{eff} is expected to be high At higher frequencies, the impedance of the depletion capacitances becomes smaller and the conductance of the highly doped implants is seen by the line, in parallel with the substrate capacitance and conductance. A decrease of ρ_{eff} is the expected behavior. In terms of linearity, the transition capacitance is dependent on the applied bias, but as the potential difference is divided over all the junctions, the bias on each individual junction can expected to be quite small compared to the junction potential.

Methods for better performance can also be foreseen. Indeed, a high density of junctions under the BOX would reduce the equivalent capacitance formed the C_Ts and reduce the size of the conductive region thus increasing their resistance.

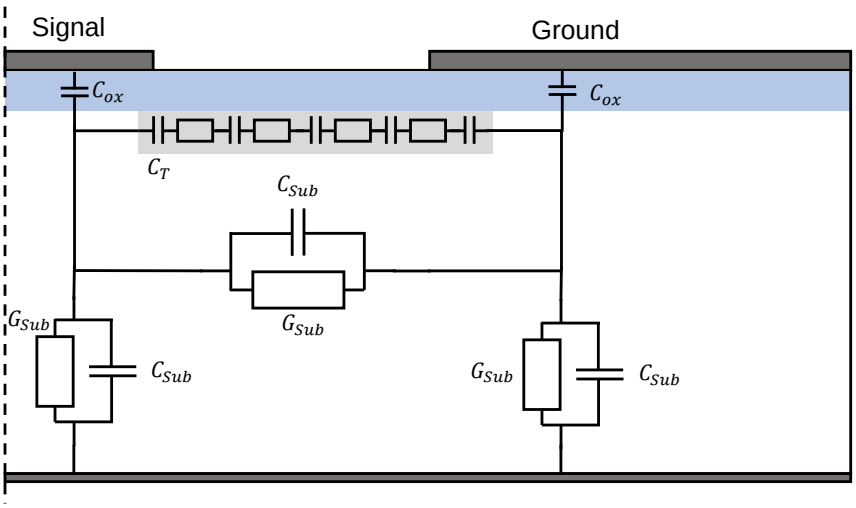


Fig. 3.9: Lumped element equivalent circuit seen by half of a CPW line built on a substrate with buried implants in the light grey zone.

3.6 Fabrication Aspects

Implantation of the buried implants can be done before all further process steps, without risking to damage the BOX, the Si active zone or any possible devices fabricated on the substrate. In order to use only one mask, the samples in [37] first underwent uniform implantation of P to create a N+ layer. Then, a photolithography mask is used to pattern the B implants, with a higher dose than the N doping, before annealing is done to activate dopants. Using a mask allows precise patterning of the doping regions, to match the needs of the passive components layout. Implant width is limited by the lithography resolution, defining the critical dimensions of the P+ implants. Furthermore, doping diffusion during the annealing or further process steps must occur on distances much smaller than the implant width, to preserve the clear definition of the doping profile

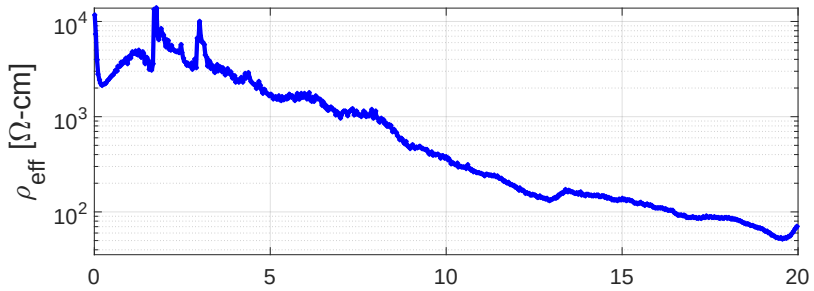
The fabrication process is further investigated with the use of the Silvaco Athena simulator in section 4.4.

3.7 Experimental results

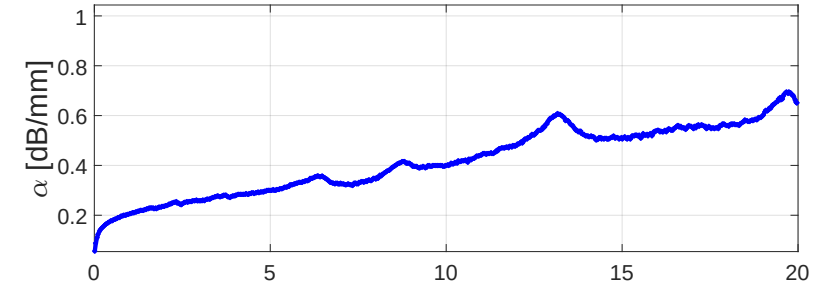
Room temperature small and large-signal measurements have been performed on the UCLouvain-fabricated sample used in [37].

3.7.1 Small-signal measurements

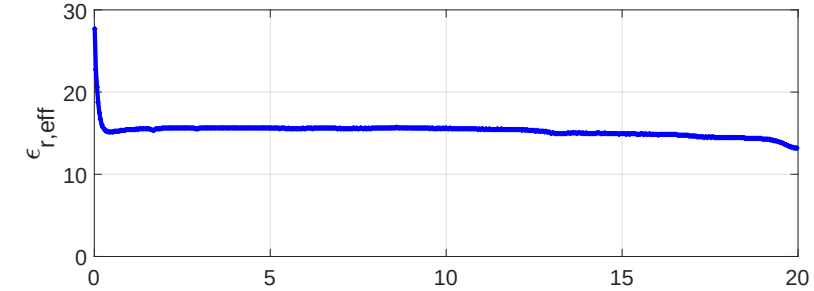
CPW lines as described in [37] were measured using a PNA-X vector nework analyzer from Keysight Technologies, connected to Ground-Signal-Ground RF Z probes from Cascade Microtech. The measurement procedure is further explained in chapter 4. The line dimensions are chosen to obtain a characteristic impedance of 50 Ω, with a signal electrode width of 26 µm, spacing of 12 µm and ground electrode width of 160 µm. The measured line is 2 mm long. RF loss factor, effective resistivity and permittivity as well as characteristic impedance were extracted using a method described in [15], after de-embedding.



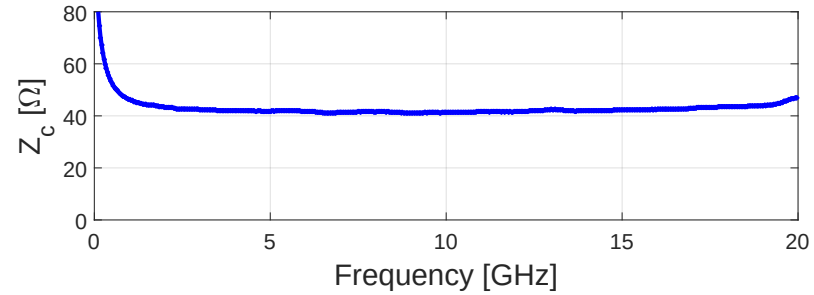
(a)



(b)



(c)



(d)

Fig. 3.10: Extracted effective resistivity (a), total loss factor (b), effective permittivity (c) and characteristic impedance (d), from RF measurements on a CPW line.

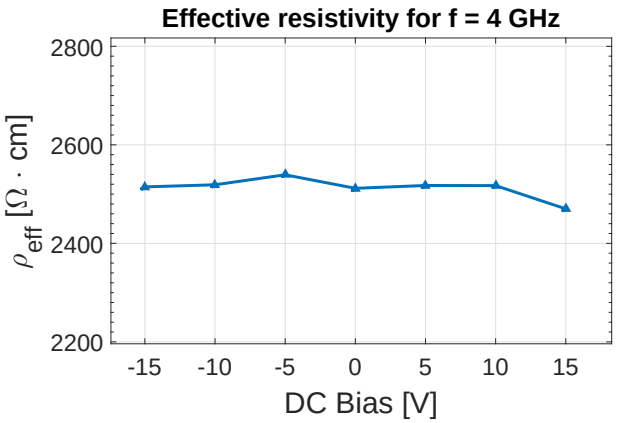


Fig. 3.11: DC bias dependence of effective resistivity, extracted from measurements at 25 °C.

Results are displayed on Fig. 3.10. As expected, effective resistivity is high, with values above 1 kΩ cm until 8 GHz. At higher frequencies, ρ_{eff} drops, but this substrate still represents a significant improvement compared to HR. Correlated with ρ_{eff} is the loss factor, which stays under 0.8 dB mm^{-1} for the entire frequency range. Irregularities appear for ε_{eff} and Z_c. Indeed, the 50 Ω-designed CPW line shows a characteristic impedance of only 40 Ω. Because dimensions are those of a 50 Ω-line, it is the effective permittivity that is different from $\varepsilon_{r,Si} = 11.78$. Indeed, as seen in Fig. 3.10c, ε_{eff} has a almost constant value of around 15.6. This increase in effective dielectric constant is due to the important concentration of electric field in the depletion regions, where it is more than 10^3 times higher than in the quasi-neutral regions. These highly dielectric zones concentrating the field lines have the effect of increasing the effective permittivity seen by the line, and to change its characteristic impedance.

The DC bias dependence of effective resistivity was also investigated, with results shown in Fig. 3.11. No significant variation can be see, as ρ_{eff} is a constant for the considered DC bias range.

Values measured on the studied substrate are now compared to small-signal measurements of trap-rich and HR-Si substrates, performed in [10] or [20] for example. In terms of effective resistivity, the substrate with buried implants presents intermediate results between trap-rich, having a resistivity above 1 kΩ cm for the entire frequency range, and HR, with its low ρ_{eff} already close to 100 Ω cm at 1 GHz.

3.7.2 Large-signal measurements

Large-signal measurements were done on the same CPW line to extract second and third harmonic level. The procedure is described in [11]. In order to suppress the effect of line losses along the line on the overall power level, harmonics are plotted with respect to the fundamental tone level at output. This also allows to fairly compare different substrates in terms of linearity. Results are shown on Fig. 3.12. In contrast with results on other substrates [21, 10], where H2 dominated the harmonic distortion, H3 appears to be as important as H2 at high powers. Furthermore, a slope change is noticed for H2.

Again, by comparing with other works, harmonic distortion levels are intermediate

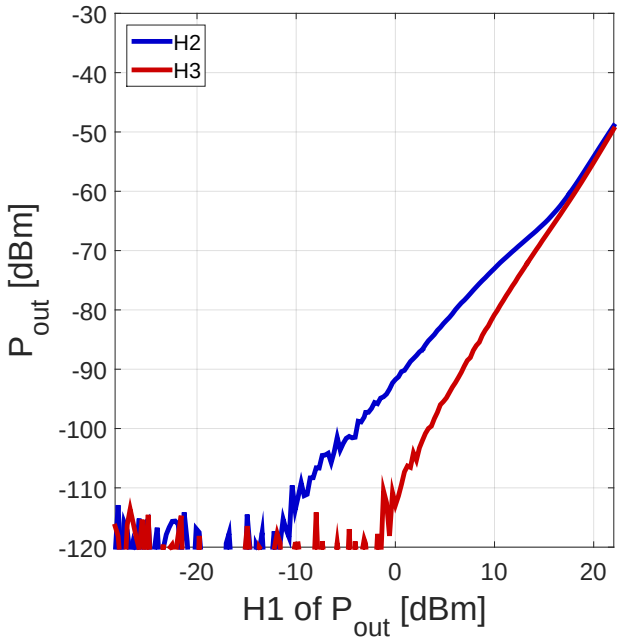


Fig. 3.12: Harmonic components H2 and H3 measured on a CPW line on a substrate with buried junctions.

between trap-rich and HR-Si.

3.8 Conclusion

In this chapter, an alternative solution to trap-rich technology was presented, consisting in an alternation of P and N doped implants below the buried oxide. The origin of its ability to counteract the PSC effect was explained, and proven by RF on-wafer measurements. These experiments prove that this novel substrate indeed presents an intermediate solution, outperforming the HR-Si substrate, but not quite as effectively as the trap-rich technology at higher frequencies, for reasons explained by introducing a small-signal equivalent circuit.

Chapter 4

Simulations and characterization

The promising concept of buried PN implants below the buried oxide as a way to reduce parasitic surface conductance and improve the RF performance of high-resistivity (HR) Si has been introduced in the previous chapter, with first experimental results proving its possible use as an intermediate solution between trap-rich and HR. This passivation method has the benefit of preserving the cristalline silicon below the BOX, enabling integration of FD SOI technology where a quality back-gate implant is necessary (which is potentially problematic if fabricated in polysilicon). In this chapter, further improvements are explored in order to optimize the design of the substrate. They are based on physical considerations, and will be confirmed using the TCAD software Atlas Silvaco. This finite-element simulation tool solves semiconductor equations and can also perform small-signal and transient analysis.

The fabrication process is also simulated using the software Athena, and finally high temperature small and large-signal measurements are made to assess the potential of this technology in these extreme applications.

4.1 Silvaco Atlas as a RF simulation tool

The CPW line is a widely used interconnect in RFICs and is also a simple passive test structure to probe substrate properties, as shown earlier. Because of its simplicity and practical use, it is often implemented and measured on test substrates. For this reason, the CPW line will be the simulated structure is the rest of this chapter. Good understanding of underlying physical principles and material properties can then be assessed by comparing simulation results with practical CPW line measurements.

Once a structure has been defined on a particular mesh, Atlas allows various types of numerical solving to take place. A static solution can be calculated, where bias on all electrodes is fixed. Atlas then solves for physical parameters such as band bending, carrier concentration, mobility, or electric field. Various physical models can be specified by the user and used by Atlas atop the basic set of semiconductor equations [39]. Small-signal simulations are also supported, which allows extraction of effective substrate parameters if a CPW line is simulated. In that case, further extraction methods have to be used, because Atlas outputs overall G-C parameters, which have to be converted to substrate parameters. Being a 2-D simulator, line resistance and inductance have to be determined from the line dimensions, effective resistivity and permittivity extracted using the method described in [15]. For large-signal simulations, transient step-by-step solutions are done to provide a few large-signal

periods. Because a large number of timesteps must be computed, these simulations are the most time-consuming.

4.1.1 Equations and models

In this section, the basic set of equations solved by Atlas is presented, along with the different physical models implemented that further specify the basic equations. The first equation describing the relation between charge density ρ and electric potential ϕ in space is Poisson's equation :

$$\nabla^2\phi = -\frac{\rho}{\varepsilon} \tag{4.1}$$

Next, the carrier continuity equation links the evolution of carrier concentrations to transport (current density), generation and recombination processes :

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n + G_n - R_n \tag{4.2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot J_p + G_p - R_p \tag{4.3}$$

For current densities and generation/recombination rates, various models exist. Improvements to carrier distribution statistics that are used in the following simulations are listed hereafter.

Bandgap narrowing For high doping concentrations, which are approached in buried junctions, the intrinsic carrier concentration becomes doping dependent and thus, space-dependent. This variation is due to a change in bandgap as doping increases. It can be expressed as :

$$n_{i,BGN}^2 = n_i^2 \exp\frac{\Delta E_g}{k_B T} \tag{4.4}$$

Where the bandgap variation is linked to doping concentration.

Recombination The Shockley-Read-Hall (SRH) model is used for recombination rates. It describes the recombination process as a phonon transition in presence of a trap state in the bandgap. Auger recombination, involving 3 carriers, is also included because its rate depends on carrier concentrations, which can be high.

Mobility Carrier mobility is an important parameter in the description of all transport processes. It can be modeled in various ways depending on the situation. In the low-field case, μ does not depend on the electric field, but can be described as dependent on the doping concentration, or even the carrier concentration when it is high. At higher fields, the effect of velocity saturation comes into play. Indeed, carriers have more energy when E is high, and can undergo more scattering processes , leading to a constant drift velocity at high fields, modeled as a reduction of mobility. Furthermore, a dependence on transverse electric field exists and must be taken into account when dealing with inversion layers. Here, a complete model, the Lombardi CVT model, tanking all dependencies into account was used.

4.1.2 Meshing

In order to make the calculation time as low as possible while keeping accurate results, an optimized mesh has to be defined. The precision of the mesh is judged sufficient when solutions converge, i.e. when a mesh produces the same results as a finer mesh. The first important parameter to consider is the extension of the mesh above and below the studied CPW line. Indeed, there is no need to simulate the physical height of a practical substrate if the studied phenomenon take place in the first few micrometers below the electrode. From static simulations and electric field

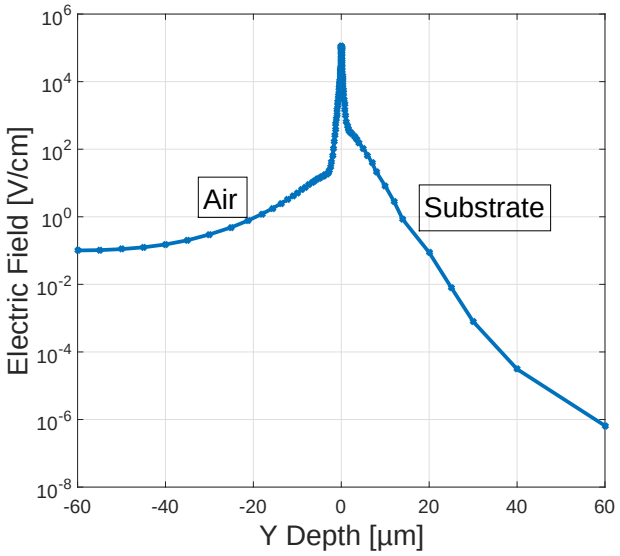


Fig. 4.1: Electric field amplitude along a vertical cutline between signal and ground electrode, where E is most intense.

distribution (see Fig. 4.1), it is clear that further than 20 µm above the electrodes, the electric field is 10^5 times smaller than its peak value, and varies slowly. The same distance holds for the substrate, however, for the extraction model to be valid, a substrate with backside metallization must have a thickness h such that :

$$h \geq 2(W + 2S) \tag{4.5}$$

In the case of a 26/12 CPW line, this translates to a minimal thickness of 100 µm. It is also possible to remove the backside metallization and make the substrate thinner, leaving a floating boundary at the backside.

Once the dimensions of the simulated structure have been defined, spacing between mesh points must be decided. The mesh must be dense where variation in quantities is abrupt, but can be coarse where there is less variation in space. For a CPW line, the mesh will be dense around the electrode edges, and in the first few micrometers of air and substrate. To correctly model the PN junctions, enough mesh points must be put in the expected depletion regions. However, in the quasi-neutral zones, the density can be somewhat looser. Further time gain can be achieved by using only half of the symmetric structure for small-signal simulations.

Reducing the dimensions of the CPW line while preserving a 50 Ω-design is however not an option. Indeed, dimensions and in particular, electrode spacing dictates the penetration depth of electric field lines into the substrate. For an

inhomogeneous substrate, the CPW line will thus see a different proportion of each material depending on its dimensions. As a result, effective resistivity will change, as showed in [35]. For this reason, all CPW line simulated and measured in what follows will have the same dimensions : signal electrode width of 26 µm, and electrode spacing of 12 µm.

4.2 Small-Signal Simulations

In this section, small-signal simulation results are presented and analyzed. This kind of simulation considers that an alternative signal of small amplitude (much smaller than the DC bias) is injected into a structure. In small-signal regime, non-linear components can be approximated by linear ones, which are the first-order approximation of the non-linear elements. The quantities of interest in small-signal simulations are ρ_{eff}, $\varepsilon_{r,eff}$, Z_c (characteristic impedance) and α (RF losses).

Extracting effective substrate parameters from Atlas small-signal simulations is not straightforward. Indeed, being a 2D simulator, only a cross-section is considered and the simulated line has no length. The quantities simulated by Atlas are signal-ground lineic conductance G and lineic capacitance G. Using C, G, dimensions of the line and substrate thickness, effective parameters (resistivity, permittivity) can be extracted using a procedure described in [15], and an analytical model is used to compute lineic resistance and inductance, allowing extraction of the characteristic impedance and the RF loss factor [16], which can both be expressed in terms of the line RLGC parameters. This technique has proven to be in good agreement with on-wafer RF measurements for various substrates such as HR Si, trap-rich, and porous silicon [41], and for various dimensions [35].

The simulation parameters are displayed in Table 4.1. It should be stressed that a FD SOI substrate is simulated in what follows, with a very thin BOX. The models used for simulations are :

- Bandgap narrowing
- SRH Recombination
- Auger Recombination
- CVT Model for mobility

Key parameters were varied while keeping all others constant. First, extension below the signal and ground electrodes is varied. Then, it is shown that a higher density of PN junctions could allow a gain of effective resistivity. The buried implant layer thickness is also varied, and finally the junctions are reverse biased to explore the possibility of artificially increasing the depletion width without necessarily using a higher resolution lithography.

4.2.1 Extension of the PN layer below the electrodes

To gain a deeper understanding of the way electric field is distributed below the CPW line in the passivated substrate, different extensions of the layer are simulated. In a traditional CPW line, electric field lines are concentrated between the signal and ground electrodes, as seen in Fig. 2.4. However, these electrodes have a nonzero

Parameter	Default Value
Substrate thickness	60 µm
BOX thickness	25 nm
Oxide/silicon interface fixed charges	$1 \times 10^{11}\,\mathrm{cm}^{-2}$
Bulk doping level (P)	$4.8 \times 10^{12}\,\mathrm{cm}^{-3}$ ($\sim 3\,\mathrm{k\Omega\,cm}$)
N implant doping level	$1.5 \times 10^{17}\,\mathrm{cm}^{-3}$
P implant doping level	$1.5 \times 10^{17}\,\mathrm{cm}^{-3}$
Buried implants layer thickness	100 nm
P and N implant width	1 µm
Implant layer extension below signal electrode	0 µm
Implant layer extension below ground electrode	0 µm
CPW signal electrode width	26 µm
CPW electrode spacing	12 µm
CPW ground electrode width	75 µm
Metal workfunction	4.7 V
DC bias on signal electrode	0 V

Table 4.1: Initial simulation parameters

width, and thus all field lines do not originate from the conductor edge. As a result, some fringing lines are present under the electrodes. This phenomenon is illustrated in Fig. 4.2, where it can be seen that horizontal electric field is present below the electrodes. Fig. 4.2 gives information about the regions where resistivity needs to be high to increase ρ_{eff}. Indeed, the CPW line only sees the regions in which field lines are. It appears that electric field is indeed concentrated in the electrode spacing, but also present below a large portion of the signal electrode, and below a smaller region of the ground electrode.

Fig. 4.3 shows the simulated CPW line. Buried implants implemented below the spacing region only are expected to capture most of the field lines and give high effective resistivity, with some improvement when extending the layer below the source electrode, and to a lesser extent below the ground electrode. Signal (0 µm, 6 µm, 10 µm and 12 µm, where 12 µm is equivalent to a total coverage of the signal electrode width) and ground (0 µm, 4 µm, 6 µm and 10 µm) extensions were considered separately. Results for the ground extension can be seen in Fig. 4.4. As expected, a small improvement in ρ_{eff} can be made if a small extension is added. However, the benefit of a wider extension is not significant. RF loss factor, ε_{eff} and characteristic impedance are not affected by these modifications. Similar results for signal extension can be seen in Fig. 4.5. In this case, resistivity increases with extension until the entire width below signal electrode is filled with implants. This is consistent with field line distribution from Fig. 4.2, where electric field is present below most of the conductor. Again, other small-signal parameters do not show any significant variation. At 4 GHz, the simulated substrate shows a relative effective permittivity of 12.76 and a characteristic impedance of 45.29 Ω, which is lower than designed, for reasons explained in section 3.7.

Although gains are only of about 500 Ω cm, extending the buried implants layer under the CPW line conductors is beneficial for small-signal parameters, and entire

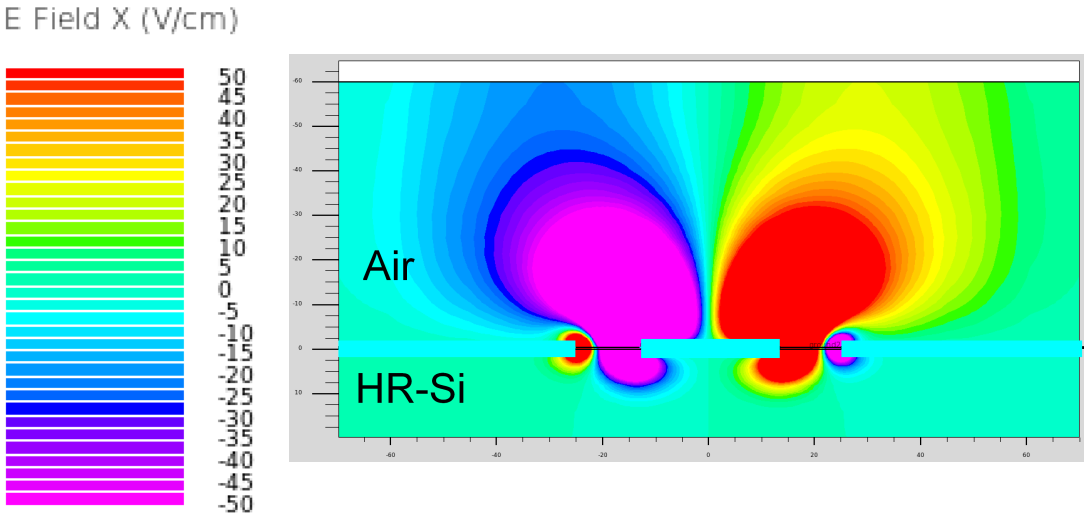


Fig. 4.2: Horizontal electric field in a CPW line structure on HR-Si with a 400 nm BOX. The signal conductor is biased at 1 V. There are no oxide fixed charges or buried implants.

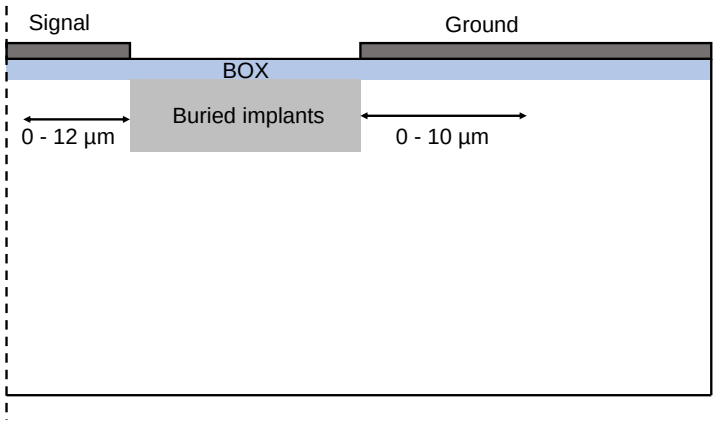


Fig. 4.3: Schematic of the simulated half CPW line, with extensions of the buried PN layer below signal and ground electrodes (not to scale).

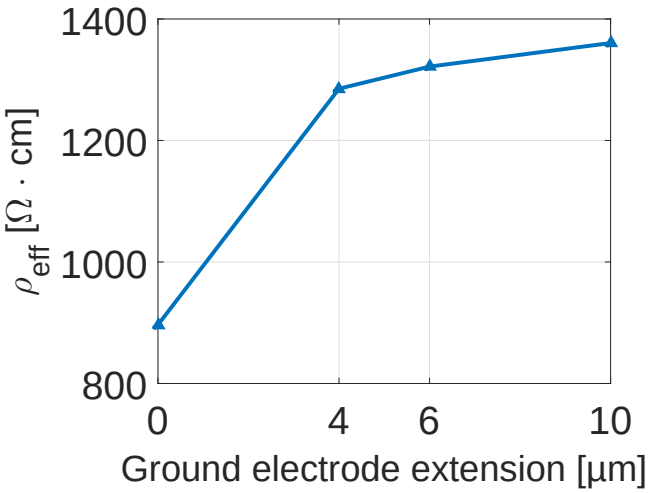


Fig. 4.4: Effective resistivity at 4 GHz extracted for different ground extensions of the buried implants layer.

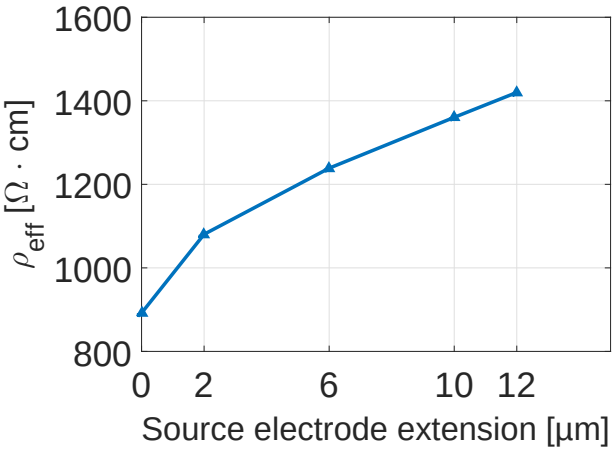


Fig. 4.5: Effective resistivity at 4 GHz extracted for different signal electrode extensions of the buried implants layer.

coverage of the line footprint with implants should be preferred when designing the substrate. Full extension also has the benefit of rendering the process easier, as it removes any alignment issue at the metal patterning step. Furthermore, as a mask is necessary in all cases, no significant cost reduction can be done by reducing the extension. However, because ground extension is only significant for the first few micrometers, simulations can be optimized. Indeed, a very fine mesh is needed to correctly simulate the depletion regions, and it is shown here that without any significant precision loss, a fully extended buried implant layer can be approximated by a layer extending 4 µm below ground electrode. Total coverage under the signal electrode is required for correct simulations.

4.2.2 Junction density

To increase the equivalent resistance of the buried implant layer, the proportion of high resistivity depletion regions in the total width has to be as high as possible. One way to achieve this is to increase the density of junctions for a given layer width. By doing this, the conductive quasi-neutral regions become smaller, and the layer is overall more depleted.

To simulate the variation of the junction density, different implant widths were defined in atlas : 1 µm, 0.6 µm, 0.4 µm and 0.2 µm. Because more depletion regions are considered when the implants are narrower, a finer mesh is needed in more regions, leading to a overall higher number of mesh points to simulate. Because Atlas puts a limit on the amount of points per simulation structure, implants were only considered in the spacing between signal and ground electrodes, with no extensions, in these junction density simulations. Indeed, this allows a coarser mesh below the conductor and thus, an acceptable number of mesh points. Results for these simulations are thus not completely representative of a fully-extended layer, but they show the expected trend.

A resistivity profile is shown in Fig. 4.6 for the narrowest implants. Clearly, in

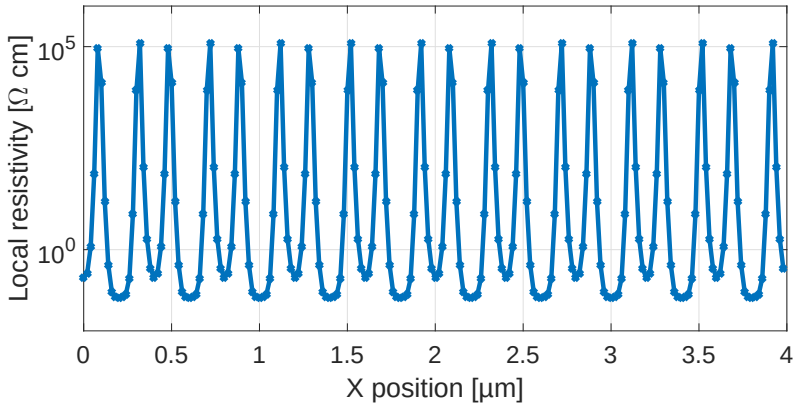


Fig. 4.6: Variation of local resistivity along the doping profile between signal and ground electrode at depth 50 nm, for an implant width of 0.2 µm.

comparison with Fig. 3.8, the local resistivity is high for a larger portion of the layer. Small-signal results for simulated CPW lines confirm what is expected : in Fig. 4.7, it is seen that ρ_{eff} increases with decreasing implant width. It is also seen that the effect of junction density becomes more important at high frequencies : at 1 GHz, all

substrates have the same ρ_{eff}, whereas a factor 5 improvement is possible at 30 GHz To understand this behavior, the equivalent circuit seen by the CPW line (Fig. 3.9

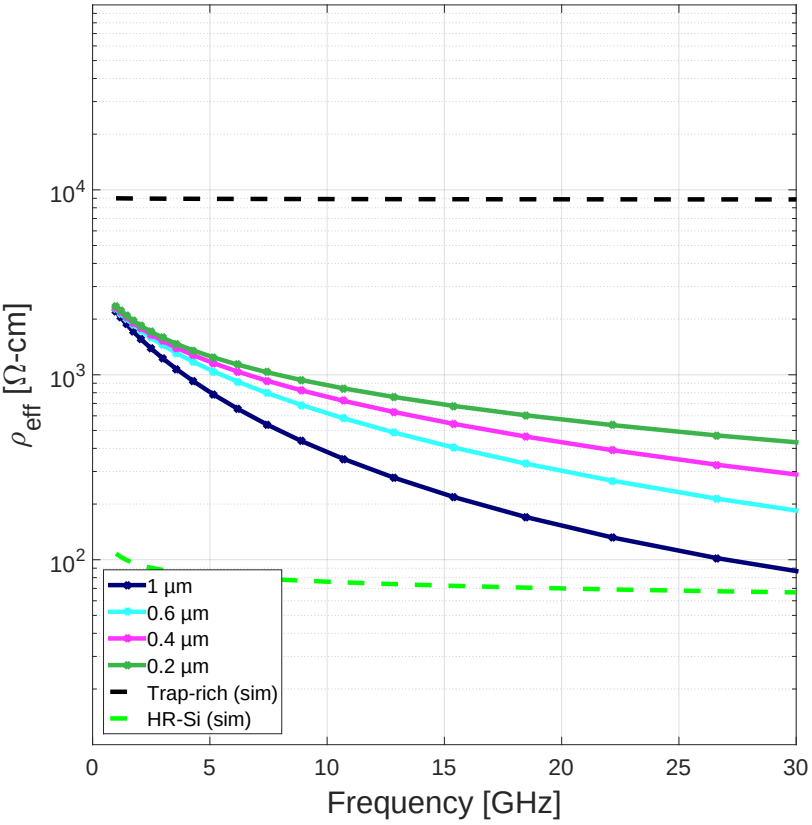


Fig. 4.7: Extracted effective resistivity of a simulated CPW line on a 3 kΩ cm, 25 nm BOX SOI substrate with implants of varying widths.

on page 39) is useful, as well as the expression for the impedance of a capacitance :

$$Z_C = \frac{1}{j2\pi fC} \tag{4.6}$$

At zero frequency, the capacitance C_{ox} acts a an open circuit. When frequency increases, the CPW line starts to see the substrate properties. At moderate frequencies of around 1 GHz, transition capacitances C_T have a very high impedance, and the conductances in series are negligible. The CPW line sees the parameters G_{sub} and C_{sub}, which is why at those frequencies ρ_{eff} is close to the nominal resistivity of the HR-Si substrate (3 kΩ cm). Then, at high frequencies, the impedance of C_T decreases. The CPW line now sees the G_{sub} and C_{sub}, in parallel with the buried implant layer, where the impedance of C_T becomes comparable with the impedance of the conductive regions. These conductances represent the quasi-neutral regions, and are smaller when these regions are narrower, which is the case when the implant width is decreased. Another reason for the increase of resistivity is to remember that capacitances in series add up as :

$$\frac{1}{C_{T,eq}} = \sum_{i=1}^{N} \frac{1}{C_{T,i}} \tag{4.7}$$

When the junction density increases, N increases, but the value of each individual $C_{T,i}$ does not change. The equivalent capacitance is thus smaller, and as a result has a higher impedance at a given frequency.

Practically, the reduction of implant width is possible only if patterning of the corresponding mask is possible. The mask is patterned by lithography, and its smallest possible feature size depends on the resolution of the equipment. With high-end modern EUV lithography machines, the resolution is advertised as low as 13 nm [42], which would allow the fabrication of implant profiles even narrower than the narrowest implants simulated here. If the trend seen in Fig. 4.7 can be extrapolated to smaller widths, a high ρ_{eff} even at frequencies above 10 GHz can be expected. However, two limitations exist.

1. The implant width is limited by the depletion width. Indeed, a quasi-neutral zone needs to exist between two space-charge regions in order to recover the equilibrium high carrier concentrations of the N and P zones. If no quasi-neutral zone can exist, the concentration gradient will disappear and a uniform carrier concentration profile will replace the alternating P N profile.

2. Because the substrate will undergo further process steps at high temperature after the implantation as part of the CMOS process for example, dopants could diffuse in the substrate. This diffusion will have the effect of smearing out the doping profile. If the characteristic horizontal diffusion length is larger than roughly half of the implant width, the carrier concentration profile will tend to be flat, again preventing the depletion regions to set up properly.

4.2.3 Junction biasing

The second approach to increasing the junction depletion width is to apply a DC bias to put the junctions in a state of reverse bias. A negative voltage has to be applied on the P side, and a positive voltage on the N side.

In practice, the junctions would be biased by a contact located outside the area occupied by the CPW line, or any other device. As Atlas is a 2D simulator taking into account only a cross-section of the CPW line, it is not possible to reproduce this contact method. Instead, small conducting electrodes were defined on top of each implant, as shown in Fig. 4.8. Ideally, these electrodes should only bias the junctions

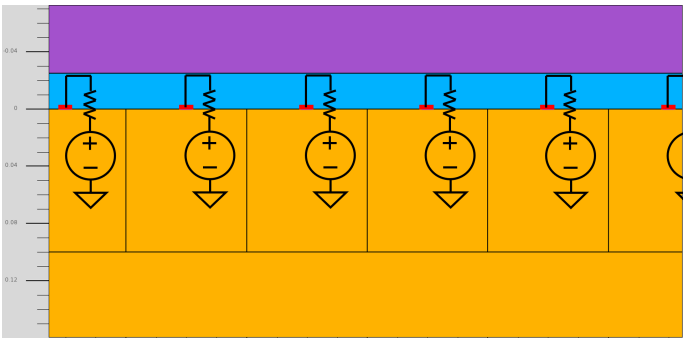


Fig. 4.8: Location of the biasing electrodes. They are 200 nm wide, and infinitely thin.

without anyhow having an influence on the electrical behavior of the CPW line.

However, by defining only a DC bias on the electrodes, they will act as a small-signal ground and absorb a large portion of the signal. Therefore, a large bias resistance of $1 \times 10^{10}\,\Omega$ was defined to prevent any small-signal ground to arise. Furthermore, the electrode width was reduced to the smallest possible value (it contains 3 mesh points in the horizontal direction) in order to minimize the effect of defining an actual electrical contact. Because a wide depletion zone is expected, the mesh was also adapted to be fine in a larger region. Finally, the only implant width considered is 1 µm, because of the intrinsic limitation of the number of electrodes in Atlas.

A first important result is shown in Fig. 4.9, where the potential difference between P and N implants is −10 V. Comparing with previous resistivity profiles, it

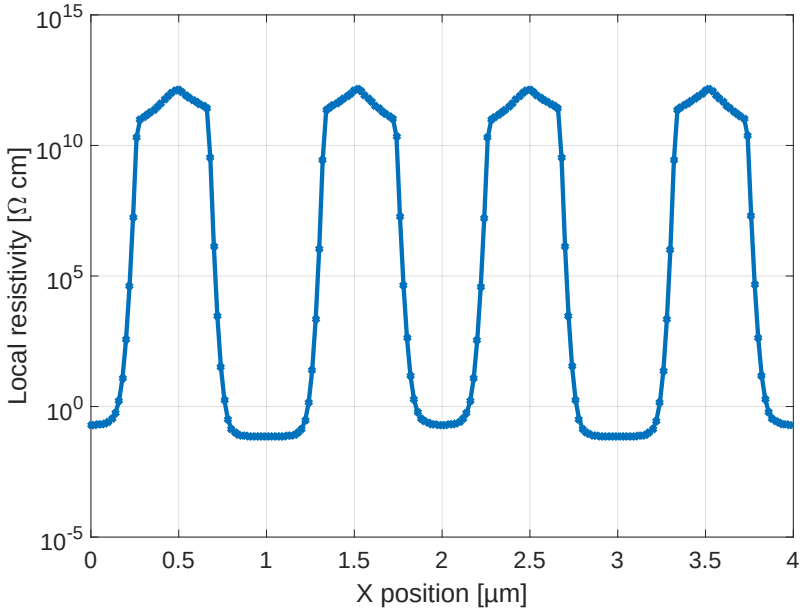


Fig. 4.9: Resistivity profile at depth 50 nm along the buried implant layers for 1 µm wide implants and junctions biased at 10 V reverse bias ($V_N = 5\,\text{V}$ and $V_P = -5\,\text{V}$).

is clear that the average depletion width has drastically increased. In contrast with the unbiased layer (Fig. 3.8), where the depletion width is estimated to be around 150 nm, the depletion width of Fig. 4.9 is around 650 nm. These depleted widths were measured for different bias conditions and put relative to the total implant width in Table 4.2.

Junction bias [V]	Relative depleted width
0	15 %
-2	30 %
-6	50 %
-10	65 %

Table 4.2: Total depleted width relative to layer width increase by junction biasing.

Effective resistivity extracted from small-signal simulations is shown in Fig. 4.10 for the entire frequency range, and in Fig. 4.11 at 4 GHz. From these simulations, it is clear that ρ_{eff} increases with reverse bias amplitude. An improvement of a

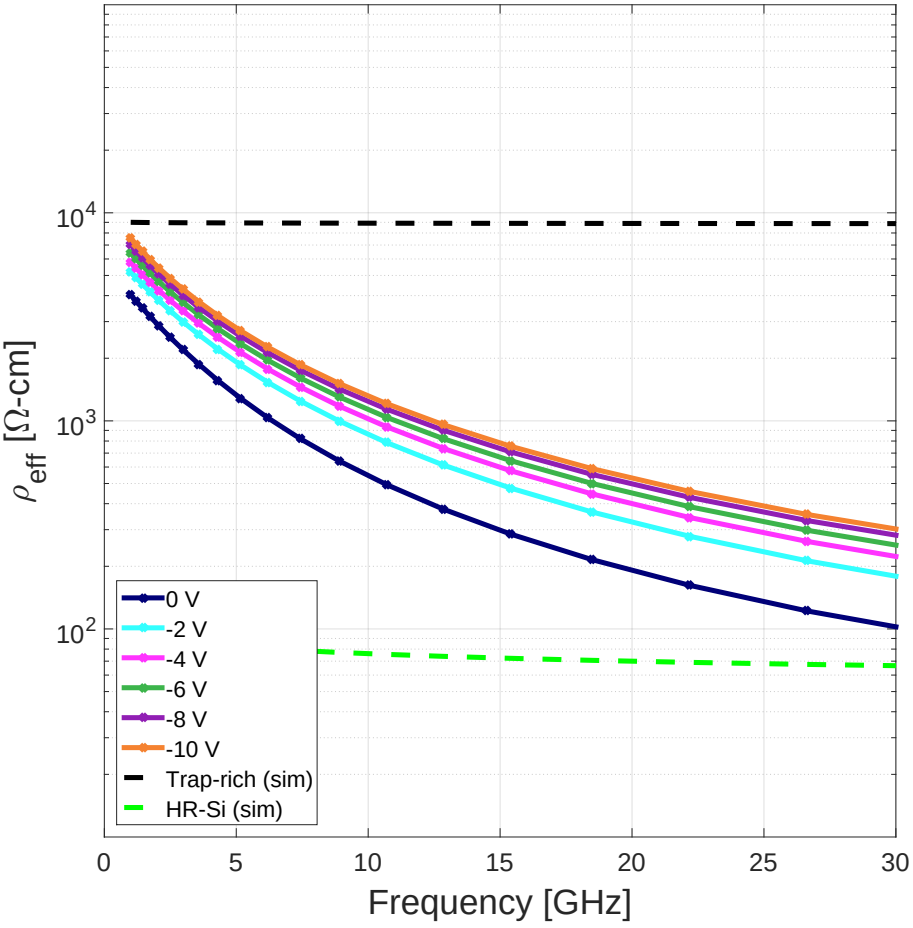


Fig. 4.10: Extracted effective resistivity of a simulated CPW line on HR-Si substrate with biased buried junctions. The reverse bias is varied from 0 V to −10 V.

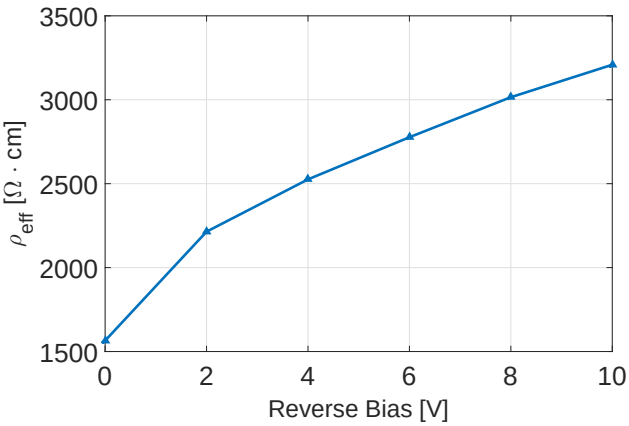


Fig. 4.11: Effective resistivity at 4 GHz extracted for different junction reverse bias voltages.

factor 3 can be made from the unbiased case as the proportion of high-resistivity capacitive regions increases as seen in Table 4.2, Furthermore, because of the increase of depletion length $l_n + l_p$, the transition capacitance C_T (Eq. 4.8) decreases and has a higher impedance at a given frequency.

$$C_T = \frac{\varepsilon_s}{l_n + l_p} \tag{4.8}$$

These promising results are however not expected to be completely representative of the effective resistivity of a practical substrate, because the biasing method is different and will not involve actual electrodes on top of the implants. In combination with an increase of junction density, it is expected that a combination of both effects will allow optimization of the effective resistivity. When biasing the junctions, care has to be taken with respect to the quasi-neutral regions : they have to exist for the depletion regions to appear. The optimal bias for a given junction density would have to be found by measuring the CPW line with different bias conditions.

4.3 Large-Signal Simulations

This part is not public.

4.3.1 Junction density

Large signal simulations were performed for implant widths of 1 µm, 0.6 µm and 0.4 µm, without any signal or ground electrode extension for mesh point limit reasons. Results for the second and third harmonic levels are shown in Fig. 4.12 and Fig. 4.13 and compared to measured HR And trap-rich substrates. First, it is clear that, as

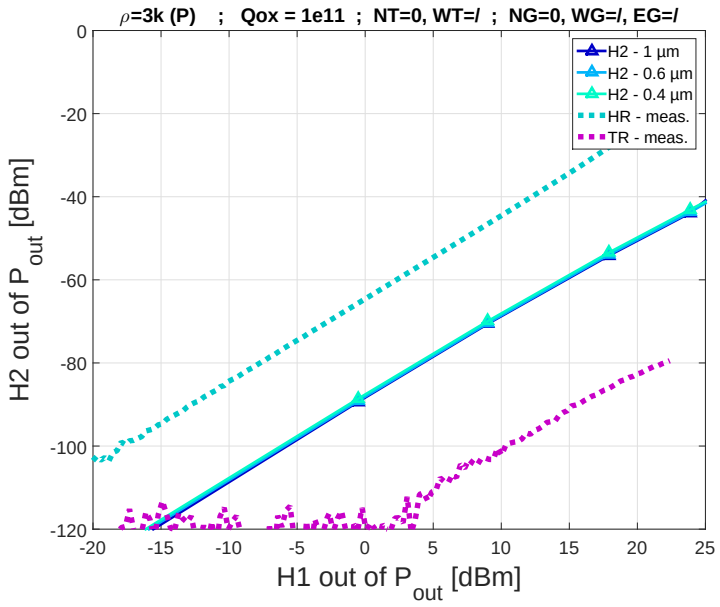


Fig. 4.12: Second harmonic extracted from Atlas simulations at varying implant widths. Measured trap-rich and HR substrates are used for comparison.

was seen for small-signal parameters, the buried implant layer substrate is a good

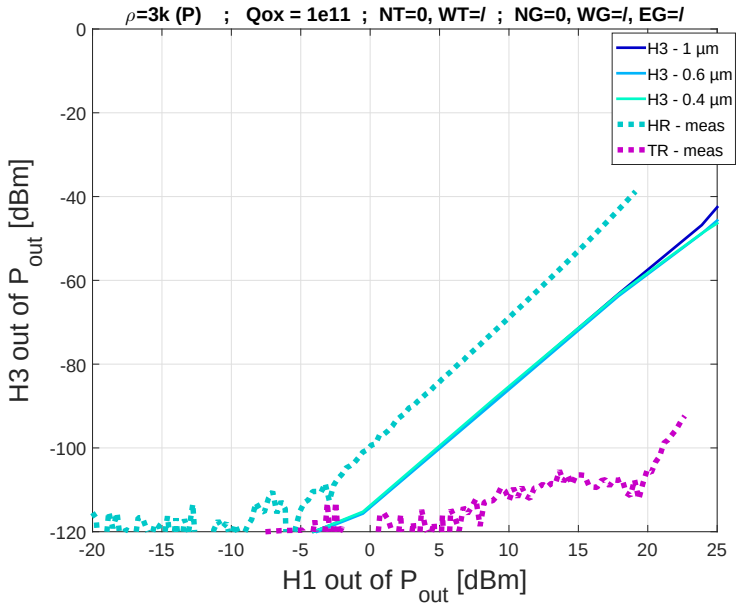


Fig. 4.13: Third harmonic extracted from Atlas simulations at varying implant widths. Measured trap-rich and HR substrates are used for comparison.

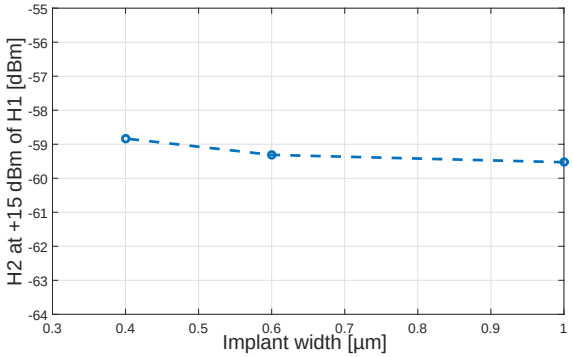


Fig. 4.14: Second harmonic level extracted at +15 dBm of H1 for various implant widths.

compromise between HR and trap-rich technologies. A gain of 25 dB is achieved with respect to HR for the second harmonic, and around 15 dB for H3. However, trap-rich technology still provides much better linearity.

Second, reduction of the implant width and thus increase in the amount of depletion junctions in the buried layer has only a very weak impact on harmonic levels. Contrarily as what was expected, a very slight increase in H2 is even seen on Fig. 4.12 when junction density increases, in opposition with the increase of ρ_{eff}. However, this variation is small (less than 1 dBm, see Fig. 4.14), and can not be considered significant.

Finally, where the HR and trap-rich linearity is dominated by the second harmonic, the doped substrate shows a higher H3, with a similar level to H2 at high input powers.

4.3.2 Junction biasing

The effect of reverse biasing the junctions and thus, increasing the depletion width as been investigated in large-signal conditions. Electrode width is 200 nm, and all junctions are reverse biased with a lumped resistance of $1 \times 10^{10}\,\Omega$ to prevent any current flowing to these parasitic ground contacts. Results for H2 are shown in Fig. 4.15, and in Fig. 4.16 for H3. Clearly, a large improvement of the simulated

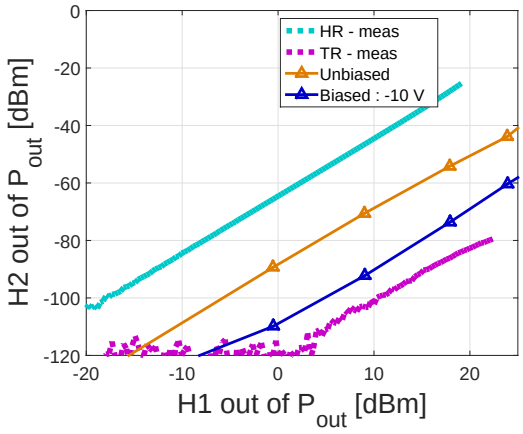


Fig. 4.15: Second harmonic extracted from Atlas simulations with and without reverse biased junctions (solid lines). Measured trap-rich and HR substrates are used for comparison (dotted lines).

substrate linearity is achieved by applying a $-10\,\mathrm{V}$ reverse bias. With respect to the unbiased substrate, the buried implant layer with biased junctions shows a reduction of H2 levels of around 20 dBm, and H3 levels are lowered by 25 dBm as well.

The difference between reverse biased and unbiased buried layers lies in the proportion of depleted regions and conductive, highly-doped regions. Substrate non-linearities are caused by a voltage dependence of the equivalent capacitance or conductance of the substrate [11, 43]. In this case, it appears that as the proportion of capacitive regions increases, harmonic distortion decreases. This implies that the transition capacitance formed at depletion junctions is less voltage dependent than the conductance of the quasi-neutral region. This could be due to the fact that more carriers are present in the quasi-neutral regions (strong doping), and are thus more sensitive to the field effect. Reducing the size of these regions reduces this phenomenon, and improves linearity. However, this drastic reduction of harmonic levels was not observed when reducing implant width, which also reduced the size of quasi-neutral regions. It has to be repeated that the biasing method used in these simulations is not representative of a real situation, where contacts will be located outside the region crossed by the CPW line electric field.

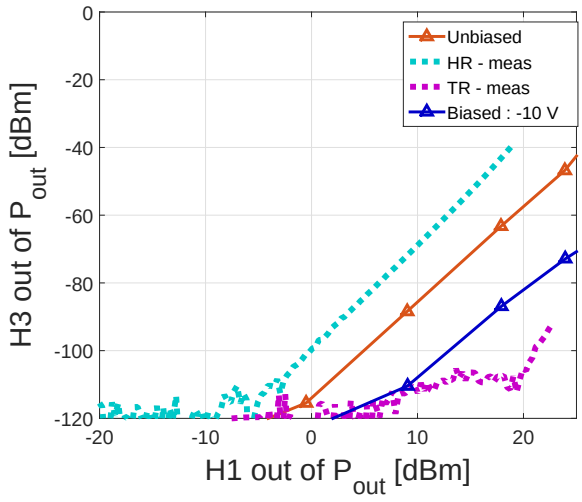


Fig. 4.16: Third harmonic extracted from Atlas simulations with and without reverse biased junctions (solid lines). Measured trap-rich and HR substrates are used for comparison (dotted lines).

4.4 Process Simulations

Using Silvaco Athena, a process simulator that can be combined with Atlas, the fabrication of samples with a buried implant layer was able to be simulated. These simulations were initially performed to predict small and large signal behavior of the samples used in [37]. However, they also allow to assess the possibility of reducing implant width to increase junction density.

4.4.1 Description of the process flow

The steps coded into the process simulator Athena are identical to real process flow steps used at UCLouvain to fabricate the samples. The process starts with a high resistivity Si wafer.

1. In crystalline materials, charged particles have preferential paths, depending on the crystal orientation. Indeed, because all directions are not equivalent in a crystal, an incident particle will encounter different stopping powers and travel further in some directions than others [44]. To prevent this effect, wafers are usually slightly tilted to present no particular orientation, but here, in order to avoid channeling, a thin layer of SiO_2 (20 nm) is deposited on top of the silicon. A diffusion step of 20 min at 800 °C under wet O_2 is then performed.

2. The first doping layer (N type) is implanted. Phosphorus atoms are implanted through the thin oxide at an energy of 50 keV and a dose of $1 \times 10^{13}\,\mathrm{cm}^{-2}$, giving the doping profile in Fig. 4.17.

3. A mask is then deposited and patterned for the P implants (see Fig. 4.18) The material used is an artificial barrier material. This mask is 200 nm thick.

4. Once the mask is patterned, the P type implants are done. Boron is implanted at a dose of $1 \times 10^{14}\,\mathrm{cm}^{-2}$ and an energy of 30 keV.

5. The dopants are then activated and diffused by thermal annealing, for 15 min at 950 °C.

6. Finally, the remaining oxide (180 nm, making it 200 nm thick) is deposited. This sample is thus not compatible with FD SOI technology.

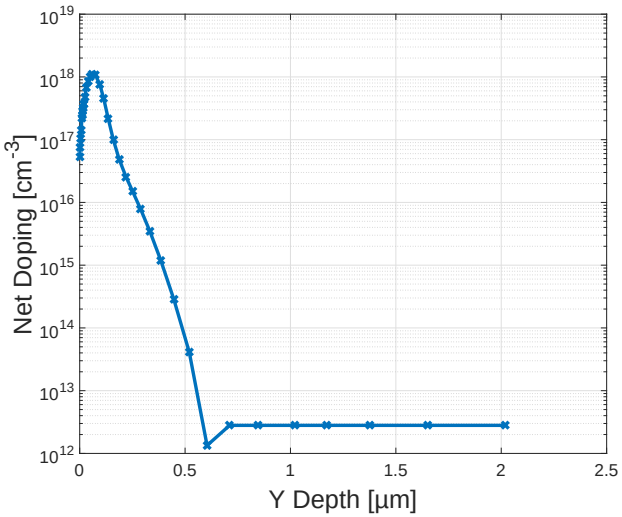


Fig. 4.17: Net doping profile after implantation of the N layer. The high doping is concentrated in the first 0.2 µm of the substrate.

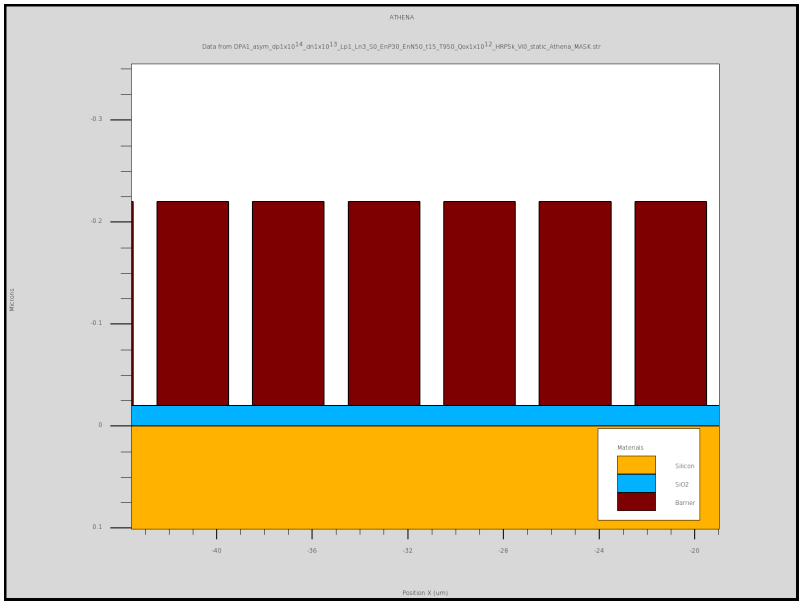


Fig. 4.18: Mask for implantation of Boron. Width of mask regions is 3 µm and are separated by a spacing of 1 µm for the P implantation. The mask is 200 nm thick.

The final structure is shown in Fig. 4.19. Using these steps, a structure is generated, which can then be used by Atlas to define electrodes and perform static, small and

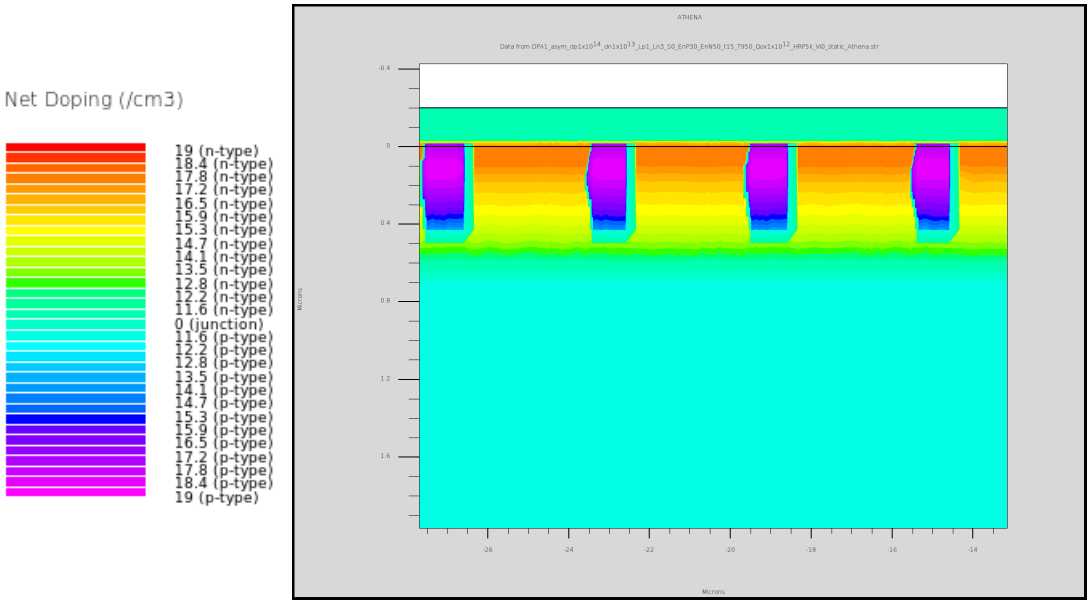


Fig. 4.19: Net doping after all process steps. N doped regions are about 3 µm wide and P doped regions are 1 µm wide.

large-signal analysis. The small and large-signal simulation results for the structure that was fabricated in [37] will be done for high temperatures and compared with measurements in the following section. Here, some variations on the process flow are presented, namely to increase the junction density, and to assess the compatibility with the thermal budget of a following full CMOS process.

4.4.2 Reducing junction density

The exact same process was simulated for N and P implant widths of 0.6 µm and 0.2 µm, respectively. The relative dimensions are identical, only absolute dimensions shrink. The goal is to observe if diffusion is significant to flatten the doping profile when the width of the implants is reduced. Indeed, the characteristic diffusion length for a given diffusion time, given by Fick's law (Eq. 4.9), is the same regardless of the implant width : only the diffusion coefficient matters.

$$L_{diff} = 4\sqrt{Dt} \tag{4.9}$$

The resulting dopant distribution is shown in Fig. 4.20. As can be seen, the different implants are still clearly defined when dimensions are reduced, only the light bulb shape is more apparent for the P implant. This shape is characteristic of scattering mechanisms occurring when the ions are penetrating into the substrate. However, the horizontal enlarging of the dopant distribution is not sufficient to alter the clear definition of the implants and allow the formation of depletion zones for this junction density. This phenomenon might still be a problem when implant width is further reduced, but not for this first improvement.

4.4.3 Thermal budget of a CMOS process

Following the fabrication of the substrate with buried implants, the wafer must undergo a full CMOS process without suffering from performance decrease. In

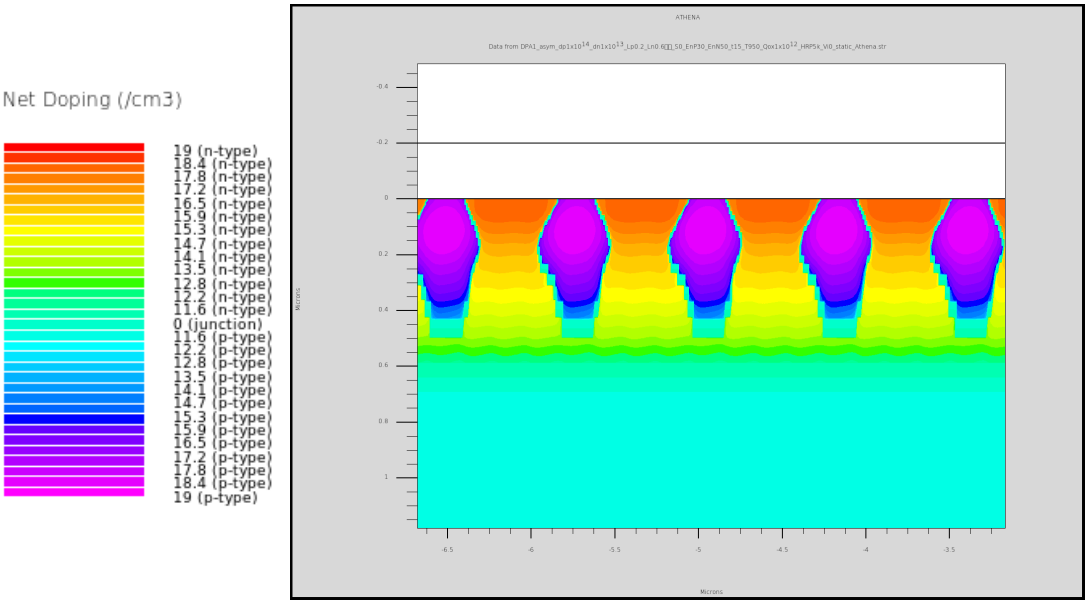


Fig. 4.20: Net doping after all process steps, with reduced implant widths.

particular, the high temperatures sustained during this process could lead to diffusion of the dopants. To simulate this thermal budget, a 4-hours diffusion step at 900 °C was added to the intial Athena simulation (with 3 micro/metre/1 µm implants). The resulting doping profile is shown in Fig. 4.21. No modification with respect to Fig. 4.19 can be observed, and it can safely be considered that a full CMOS process will not alter the performance of the buried implant substrate.

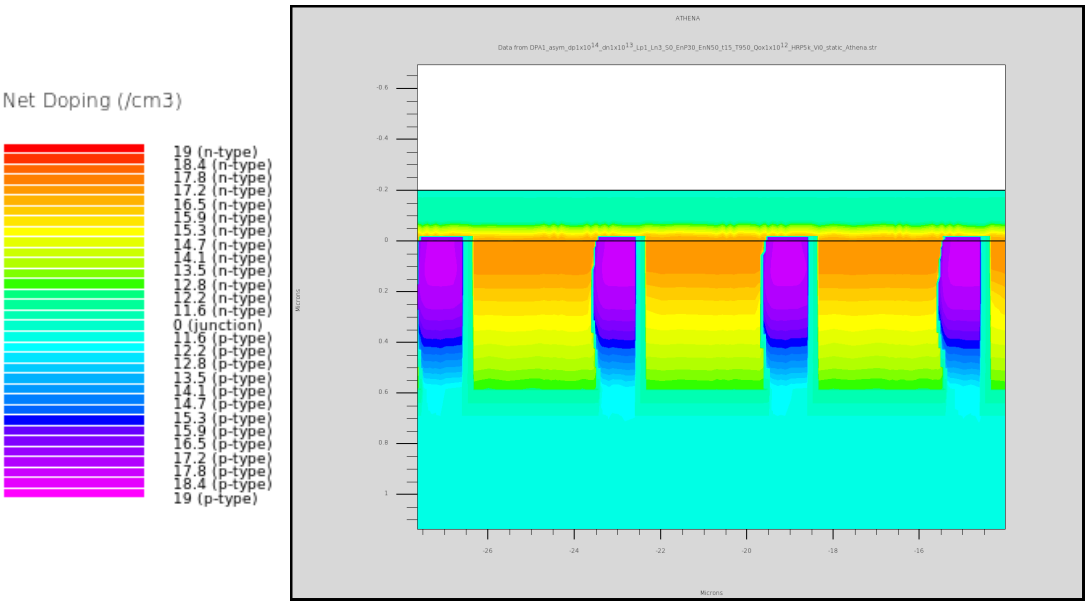


Fig. 4.21: Net doping after enduring a 4-hour long 900 °C temperature step.

4.5 Characterization at high temperature

Aside from simulations, the first fabricated substrate using this technology [37] was characterized at high temperature under small and large signal conditions, to

assess its possible use in applications where temperature is high, for example energy-consuming power amplifiers. The measured substrate is based on a high-resistivity ($\rho_{nominal} > 5\,\mathrm{k\Omega\,cm}$) Si wafer. Implantation was done before deposition of SiO_2, with the parameters shown in Table 4.3 that are also the parameters used in the process simulations. A total oxide thickness of 200 nm was used. The measured CPW line

Parameter	Value
N+ (Phosphorus) layer implantation energy	50 keV
N+ (Phosphorus) layer dose	$1 \times 10^{13}\,\mathrm{cm^{-3}}$
N implant width	3 µm
P+ (Boron) implantation energy	30 keV
P+ (Boron) implantation dose	$1 \times 10^{14}\,\mathrm{cm^{-3}}$
P implant width	1 µm

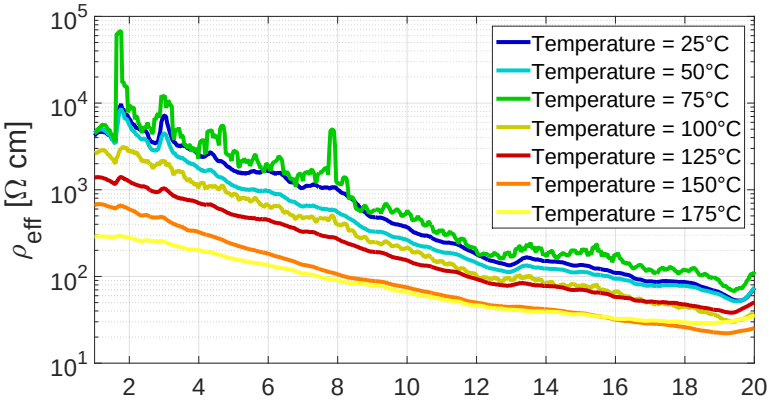
Table 4.3: Fabrication parameters for the measured substrate with buried implant layer.

has the usual 26/12 dimensions used throughout this work, and is thus designed to have a characteristic impedance of 50 Ω. Temperature was controlled by heating the chuck holding the wafer during the analysis. It was varied from room temperature (25 °C) to 190 °C. The measurements were all done using A PNA-X Vector Network Analyzer from Agilent Technologies, and a pair of GSG Z Probes from Cascade Microtech, after calibration on a standard impedance substrate.

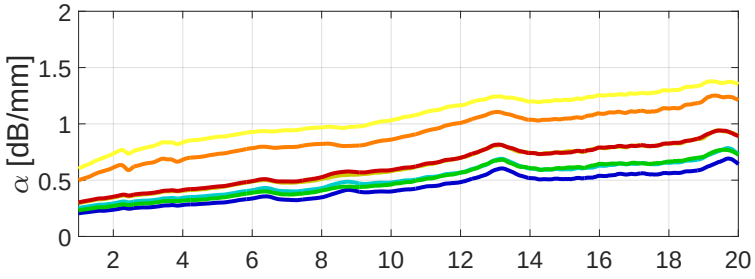
4.5.1 Small-signal measurements

Small signal S-parameters were measured and deembedded using a method described in [45]. Then, effective substrate parameters are extracted using the method described in [15]. The full results are shown in Fig. 4.22. In addition, Fig. 4.23 shows the variation of ρ_{eff} with temperature, along with values extracted from small-signal simulations based on the structure produced after process simulations by Athena.

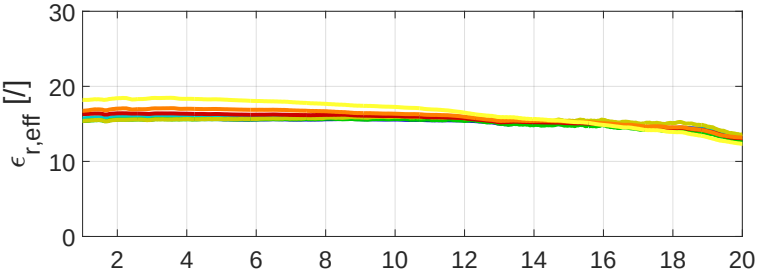
As expected, the measured effective resistivity drops, and losses increase with temperature, especially past a threshold temperature around 100 °C (however, the measurement point at 75 °C is slightly noisy, and thus maybe not so well performed). For ρ_{eff}, about an order of magnitude is lost between room temperature and 175 °C. In agreement with [10], this decrease in ρ_{eff} is attributed to an increase in intrinsic carrier concentration with temperature [40]. This phenomenon occurs in the substrate bulk, lowering the bulk resistivity and thus creating a conducting path below the buried implant layer. When compared to high temperature measurements on trap-rich and HR substrates in litterature [10], the depleted substrate presents intermediate effective resistivity. As shown in Fig. 4.23, Athena and Atlas simulations slightly overestimate effective resistivity, suggesting that perhaps the junctions are not so well defined in the physical substrate, because dopant diffusion occurred to a higher degree.



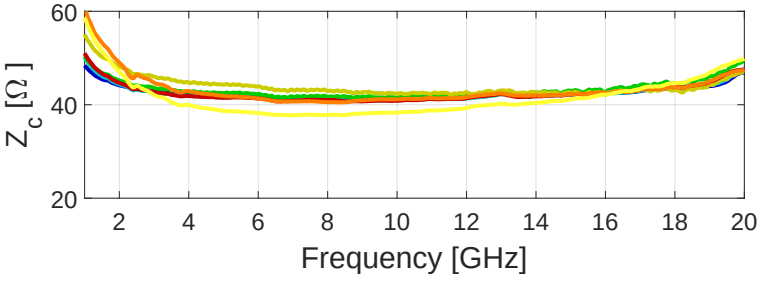
(a)



(b)



(c)



(d)

Fig. 4.22: Extracted effective resistivity (a), total loss factor (b), effective permittivity (c) and characteristic impedance (d), from RF measurements of UCLouvain-fabricated sample at high temperature.

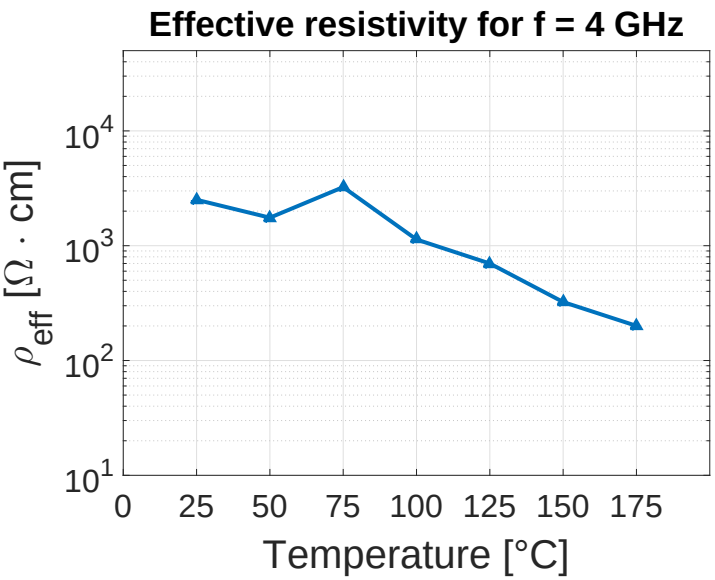


Fig. 4.23: Extracted effective resistivity at 4 GHz variation with temperature.

4.5.2 Large-signal measurements

A different setup is used for large-signal measurements, as a large range of input power is needed [11, 41]. Aside from the PNA-X Vector Network Analyzer from Agilent Technologies, a power amplifier is used to provide the needed high input power, which is swept from -30 to +25 dBm. To take into account the losses and attenuation in the equipment (cables, probes), a calibration is performed on a thru line built on the Impedance Standard Substrate, allowing deembedding of these parasitics and extraction of true measurements at the device under test. A series of filters at input and output allows a single fundamental tone of 900 MHz to be injected into the CPW line, and the network analyzer at output then detects and measures third and second harmonic levels as low as -115 dBm. In an identical fashion as for small-signal measurements, temperature was varied from 25 °C to 190 °C.

Results for both the second and third harmonic are shown on Fig. 4.24. The only DC bias point shown is 0 V, as no dependence on bias was observed for H2 or H3. For H2, an increase of around 10 dBm is measured between room temperature and 190 °C, where H3 increases by around 15 dBm. This has the effect of making H3 larger than H2 at high temperatures, dominating the total harmonic distortion. As seen on Fig. 4.25 and Fig. 4.26, the temperature dependence of harmonic levels of the substrate with buried implants is weaker than for the trap-rich substrate. This implies that the intrinsic carrier concentration increase with temperature has a reduced effect in the depleted substrate. As a result, at high temperatures, the total harmonic distortion measured for the substrate with buried implants and the trap-rich substrate have comparable levels, as seen in Fig. 4.27 where at 190 °C only a 5 dBm difference is observed.

In conclusion, the substrate with buried implant layer presents good performance at high temperature in terms of harmonic distortion. The variation of harmonic levels with temperature is moderate, and weaker than trap-rich substrate, offering comparable performance at very high temperature.

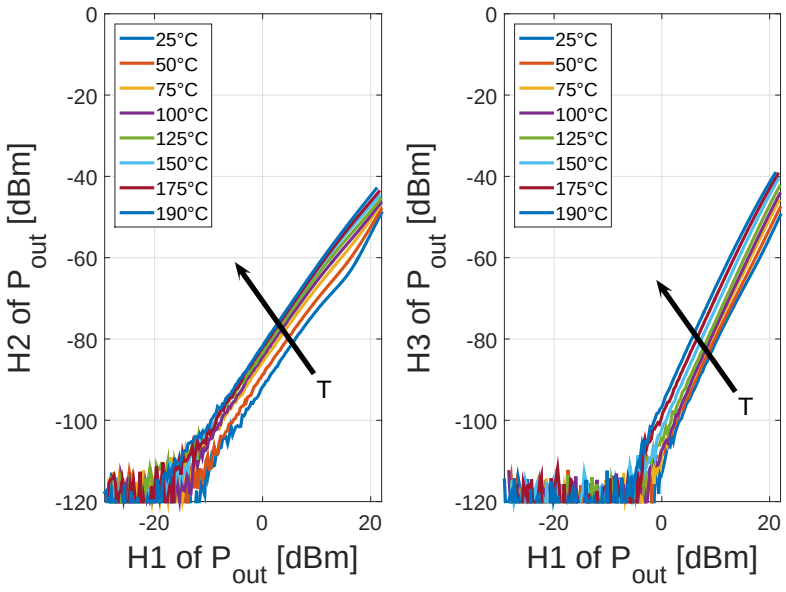


Fig. 4.24: Measured harmonic distortion levels at the output of a 2 mm CPW line built on UCLouvain-fabricated sample.

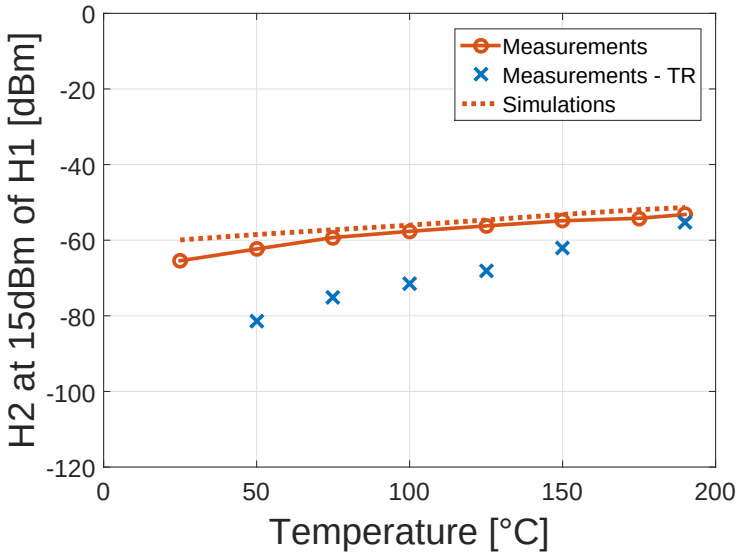


Fig. 4.25: H2 level at 15 dBm of H1 at high temperature, for Athena and Atlas simulations, measurements on the substrate with buried implants, and on a UCLouvain trap-rich substrate.

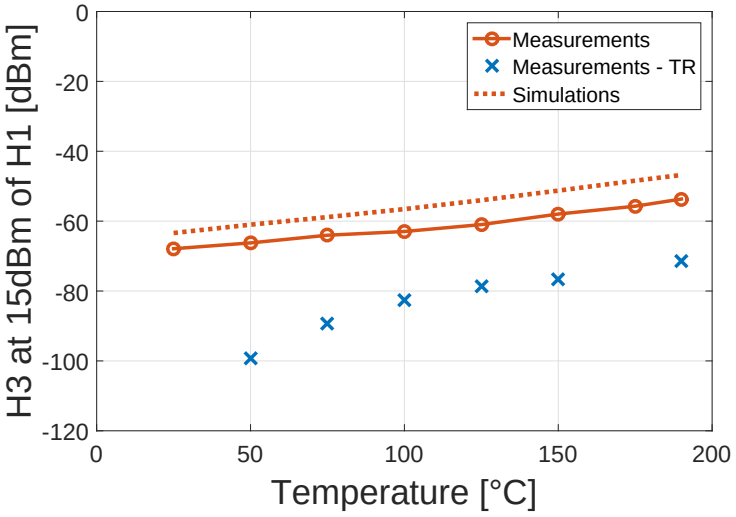


Fig. 4.26: H3 level at 15 dBm of H1 at high temperature, for Athena and Atlas simulations, measurements on the substrate with buried implants, and on a UCLouvain trap-rich substrate.

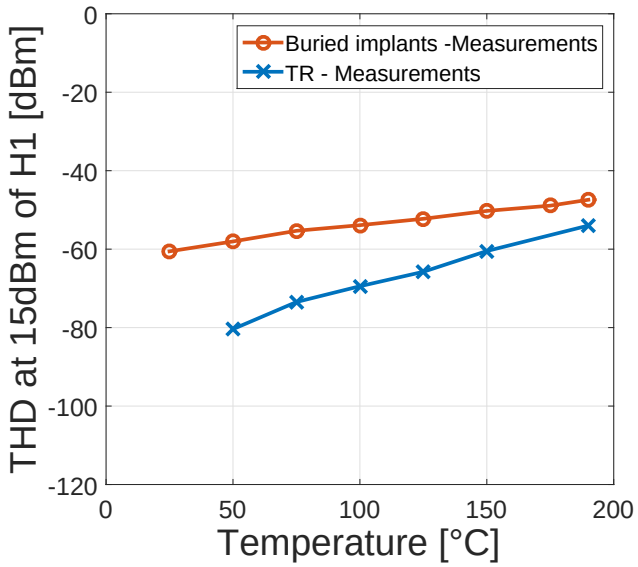


Fig. 4.27: Total harmonic distortion measured at the output of a 2 mm CPW line for both trap-rich and buried implants substrate.

Chapter 5

Conclusion

In future developments of the microelectronic industry, the next step is predicted to be integration of both RF and digital integrated circuits on the same platform, forming a system-on-chip. The substrate shared by these two different technologies must satisfy strong requirements, and in particular, Si-based substrates need to be improved for good RF performance in terms of losses and linearity. The trap-rich substrate is a widely available solution for RF applications, presenting excellent RF performance while being compatible with the CMOS process. However, integration on the FD SOI platform has not been achieved yet.

Indeed, in FD SOI, a heavily doped ground plane implant is implemented below the BOX, forming a P-N junction with the substrate. This P-N junction is reverse biased to prevent leakage, but reverse current could potentially increase when the junction is partially defined in polysilicon.

In this thesis, an alternative substrate technology was presented, where a layer of buried implants is implemented below the BOX. These alternating P and N doped implants increase resistivity by giving rise to depletion regions at the P-N junctions, where carrier concentration is low and resistivity is high. The performance of this concept was shown by experiments on a CPW line structure to be intermediate between trap-rich and HR-Si.

Following these first results, Atlas Simulations were carried out to investigate the possibility to optimize this design. First, it was shown that by using high-resolution lithography, a larger number of junctions per unit width could be achieved. This, in turn, increases the number of depletion regions and thus, of high-resistivity zones. An increase of ρ_{eff} by a factor 2 at high frequency can be achieved in this way, while no significant change in harmonic distortion appears to take place. Second, the possibility to reverse bias the junctions was explored. This has the effect of increasing the width of each individual depletion region, and thus also increasing effective resistivity. Biasing the junctions could also allow a drastic reduction of generated harmonics.

Furthermore, small- and large-signal measurements at high temperature showed a decrease of effective resistivity with temperature, attributed to an increase of the intrinsic carrier concentration. Harmonic distortion increases as well, but in a weaker fashion than a trap-rich substrate, leading to eventually similar levels at very high temperature. Both of these measurement where coherent with results obtained from process simulations using Athena.

Most of this work was based on simulations, and could sometimes not exactly

replicate a potential practical implementation, especially for the junction biasing. Furthermore, the reduction of the implant width is certainly limited by the depletion zone width, and the doping level. This limit will have to be found by actually going through a production process.

Finally, the ground-plane implant in trap-rich polysilicon was investigated and simulations of P-N junctions have not shown any change in reverse current. These simulations were perhaps not considering all mechanisms taking place in such structures, and more work is required to ensure that the ground plane implant quality would be preserved.

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UNIVERSITÉ CATHOLIQUE DE LOUVAIN
École polytechnique de Louvain
Rue Archimède, 1 bte L6.11.01, 1348 Louvain-la-Neuve, Belgique | **www.uclouvain.be/epl**