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Assessment of the split CV mobility extraction method in 28nm FDSOI transistors

Authors : Alban **MORELLE**,
Supervisors : Denis **FLANDRE**, Jean-Pierre **RASKIN**
Readers : LAURENT **FRANCIS**, Valeriya **KILCHYTSKA**,
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Abstract

Extraction of the effective carrier mobility is of major importance to evaluate the transport characteristics and performances of advanced transistors. The relative importance of parasitics has however increased with reduction of the gate length. Mobility extraction methods initially designed for long devices must therefore be adapted by including proper correction for these parasitcs in highly scaled nodes.
In this work, the application of the well known split CV method is assessed in 28FDSOI transistors with gate length down to 25 nm using TCAD simulations. The conventional split CV method is shown unable to extract the mobility correctly in short FDSOI transistors. This limitation is attributed to the increased impact of underlap-related parasitics neglected by the method's implicit assumptions.
The significant bias dependence of the access resistance and the non-negligible contribution of the inner finging capacitance are notably identified as the main sources of mobility underestimation by the split CV method in these short FDSOI transistors. An improved split CV extraction procedure accounting for these parasitics is then shown able to extract the effective mobility in strong inversion within less than 10% variation from the TCAD implemented model for gate lengths down to 25 nm.
Measurements on 28FDSOI transistors are seen to qualitatively confirm the insights from the TCAD simulations.

Acknowledgments

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Contents

1 Introduction

Mobility and transport characteristics are of paramount importance to evaluate the performance of advanced CMOS technologies. Their development has indeed involved significant efforts to enhance the carrier mobility, yielding higher on current without concession on leakage or load capacitance. Mechanical stress has notably been used to boost mobility as in the bulk 45nm bulk node [1] and, thanks to their inherent control of short channel effects, fully depleted devices can be left undoped to reduce the mobility lowering effective field in the channel [2].
Proper extraction of the carrier mobility thus plays an important role in the development of advanced transistors, which requires correlation of transport properties to transistor architecture, materials and processing.

Numerous extraction methods have been developed over the years, and progressively adapted to the difficulties arising in highly scaled devices. The most used are the Y function and the split CV methods. Current splitting techniques based on the Lorentz force have also been proposed [3].
Both the Y function and split CV methods are valid in strong inversion and performed in the linear regime (low V_{DS}) to avoid carrier velocity saturation and out of equilibrium transport [4]. The MOSFET current under these conditions writes

$$I_D = \frac{W_{eff}}{L_{eff}} \mu_{eff} Q_i^{'} V_{DS}^{'} \tag{1.1}$$

With $Q_i^{'} = \frac{Q_i}{W_{eff} L_{eff}}$ the inversion charge per unit area and $V_{DS}^{'} = V_{DS} - R_{SD} I_D$ the effective drain to source voltage, R_{SD} being the series access resistance.

The Y-function method was initially proposed by Ghibaudo in [5]. It assumes the so called *homographic* mobility dependence on the gate voltage

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 (V_{GS} - V_T) + \theta_2 (V_{GS} - V_T)^2} \tag{1.2}$$

with μ_0 termed the *low-field mobility*. The parameters θ_1,θ_2 are called the linear and quadratic attenuation factors, and respectively represent increased phonon scattering and surface roughness scattering for higher gate voltages (the initally proposed method assumed $\theta_2 = 0$) [4].
The inversion charge in strong inversion is expressed as $Q_i^{'} = C_{ox}(V_{GS} - V_T)$. From equations 1.1 and 1.2, one then derives the Y function as

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W_{eff}}{L_{eff}} C_{ox} \mu_0 V_{DS}} (V_G - V_T) \tag{1.3}$$

which doesn't depend on θ_1, nor on R_{SD}. Y varies linearly with V_{GS} in strong inversion (which is also a good criterion to evaluate the validity of the mobility model). The threshold voltage V_T can

then be extracted as the intercept of Y with the V_{GS} axis, and the low-field mobility μ_0 from the slope of the curve (provided one knows W_{eff}, L_{eff} and C_{ox}).

The Y-function method has the advantage of giving a consistent extraction of V_T and μ_0, and is most importantly independent of θ_1 and the series access resistance R_{SD} [4]. This is of particular interest in short transistors, for which R_{SD} becomes significant with respect to the channel resistance.
The inital method has been adapted to highly scaled devices by accounting for θ_2, an important factor for transistors with small equivalent oxide thicknesses (for which surface scattering becomes an important phenomenon). Different approaches to account for θ_2 are reviewed in [4]. A Y-function based method valid from weak to strong inversion has also been derived in [6], and Karatsori et al. used a lambert W function for preciser modeling of $Q_i^{'}$ with the gate voltage [7].

The Y-function method is widely used for extraction of the low field mobility μ_0 in the FDSOI transistors considered in this work. Its results have shown important degradation of μ_0 with the gate length below $100\,nm$. This has been attributed to scattering by neutral defects in the channel, most likely introduced during implantation of the source and drain diffusions [2, 8, 9] (though [10, 11] have indicated this degradation could be an artifcat of the Y-function extraction due to the access resistance bias dependence).

Despite its improvements, the Y-function method still relies on predetermined expression of $\mu_{eff}(V_{GS})$ and $Q_i(V_{GS})$. Assuming a non-homographic mobility law prevents it to be applied effectively, for example in junction less double gate FET's [12, 13].

The split CV method was initially proposed by Koomen et al. to study interface states in weak inversion [14]. It was later extended to mobility extraction by Sodini et al. [15]. The method relies on measurement of both current $I_D(V_{GS})$ and gate capacitance $C_{gg}(V_{GS})$ curves. Starting from Eq. (1.1), one writes

$$\mu_{eff} = \frac{L_{eff}^2 I_D}{Q_i V_{DS}^{'}} \tag{1.4}$$

from which μ_{eff} can thus be obtained by extraction of L_{eff}, Q_i and R_{SD}. Unlike in the Y-function method, the inversion charge Q_i is obtained here by integration of the gate capacitance C_{gg} from a starting voltage V_{GS}^* in accumulation (where the gate capacitance is theoretically zero except for the parasitic capcitances):

$$Q_i(V_{GS}) \approx \int_{V_{GS}^*}^{V_{GS}} C_{gg}(V)dV \tag{1.5}$$

The method is thus very sensitive to the extraction of the gate capacitance C_{gg}. Several modifcations to the inital method have been developed to adapt it for advanced transistors. [16, 17, 18] propose corrections for the high gate leakage current perturbing the extraction for transistors with thin gate oxides. Parasitic capacitances and series resistances also play an increased role when scaling down the length. The total gate capacitance measurements then need to be corrected from parasitic contributions and the access resistance R_{SD} must be accounted for in $V_{SD}^{'}$ (Eq. (1.1)) [19] [20].
Alternatively, RF split CV techniques have been proposed to discriminate between different capacitances in leaky devices [21] and eliminate floating body [22] or self-heating effects [23].

The split CV method has shown specific advantages for FinFET's and FDSOI transistors, and regained attention for its robustness where other simple method are insufficient [22] [24]. It doesn't pre-assume any specific dependence of the mobility and inversion charge on the gate voltage, and is exclusively based on direct measurement of the devices [20]. Moreover, the split CV method is particulary interesting for multigate transistors as it enables the extraction of μ_{eff} without prior knowledge of C_{ox} or W_{eff}, which might not be reliably known in such devices [22].

This work proposes an in-depth assessment of the application of the split CV method to advanced FDSOI devices down to $L_{mask} = 25\,nm$. It builds on previous work by Vandermolen et al., which notably encountered difficulties for the experimental extraction of the inversion charge in 28FDSOI transistors [23].
A two-dimensional TCAD simulation structure (further called "deck") with geometry and doping profiles close to 28FDSOI technology [25] was made available by the CEA-Leti. It was thus decided to leverage TCAD simulations in this work to investigate the intrinsic limitations of the method at the device level, free of possible measurement artifacts.

A important prior step to this work was thus to master the Synopsys Sentaurus TCAD simulation software and to familiarize with the 28FDSOI deck. This intial TCAD simulation setup is described Chapter 2, and assumes a simple constant mobility model. This is modified by adding relevant physical mobility models in order to obtain a qualitatively correct mobility behaviour, satisfying enough to reliably assess the split CV extraction method.

In Chapter 3, a conventional split CV method is then applied to the TCAD extracted curves and its hypotheses are systematically highlighted. The method is shown unable to correclty extract μ_{eff} in short transistors, motivating the deeper study of its limitations proposed in the next chapters.

The importance of the access resistance R_{SD} is firstly studied in Chapter 4. Different R_{SD} extraction methods are compared, and the total resistance method is shown suitable in our case. A significant dependence of R_{SD} with V_{GS} is extracted, in good agreement with results from literature. This behaviour is shown to have a major impact on the extracted mobility values and evolution with V_G in short transistors. This impact has been reported for the Y-function method, but had to the author's knowledge been neglected up to now in split CV mobility extractions.

Chapter 5 investigates the parasitic contributions to the gate capacitance. It is highlighted that in FDSOI the inner fringing capacitance is not shielded in accumulation due to the well known absence of dynamic hole response. A capacitance extraction method proposed by Vandermolen et al. is successfully applied and confirmed useful to discriminate between the different contributions to C_{gg}. Using its insights, it is shown that the inner fringing capacitance can be partly linked to gate modulation of the underlap charges.

The impact of this inner fringing capacitance on the mobility extraction is then studied in Chapter 6. It is seen to be the major remaining factor of apparent mobility degradation with the gate length after $R_{SD}(V_{GS})$ extraction. The above mentioned capacitance extraction method is shown effective to correct for its contribution, and mobility results in good agreement with the TCAD imposed values are then obtained. Alternatively, performing linear interpolation on the extracted charge is also proposed as a practical way to get rid of the inner fringing parasitic contribution.

Finally, the improved method developed from TCAD simulations is applied to 28nm FDSOI measurements in Chapter 7. Although quantitative discussion would require more extensive characterization, the insights from the TCAD simulations are retrieved qualitatively by these measurements.

2 TCAD simulation setup

TCAD simulations presented throughout this work have been performed with the Synopsys Sentaurus sofware suite. An initial simulation structure (further called ‘"deck") was provided by CEA-Leti and will be detailed in the following sections. It was designed as a look-alike version of a full simulation setup, including process simulation and calibrated to measurements on 28FDSOI technology [25]. The structure and doping profiles of the available deck are thus very close to the ones of this full setup.
After presenting these, one will briefly discuss the physical models of the simulation. The simple constant mobility intially implemented will be modified by taking into account relevant physical mobility degradation phenomena. The goal is to retrieve a qualitative, physically correct mobility behaviour to reliably assess the split CV extraction method. The obtained I-V curves will be compared against the UTSOI2.2 compact model to confirm the suitability of this modified mobility model.

2.1 Structure and doping profiles

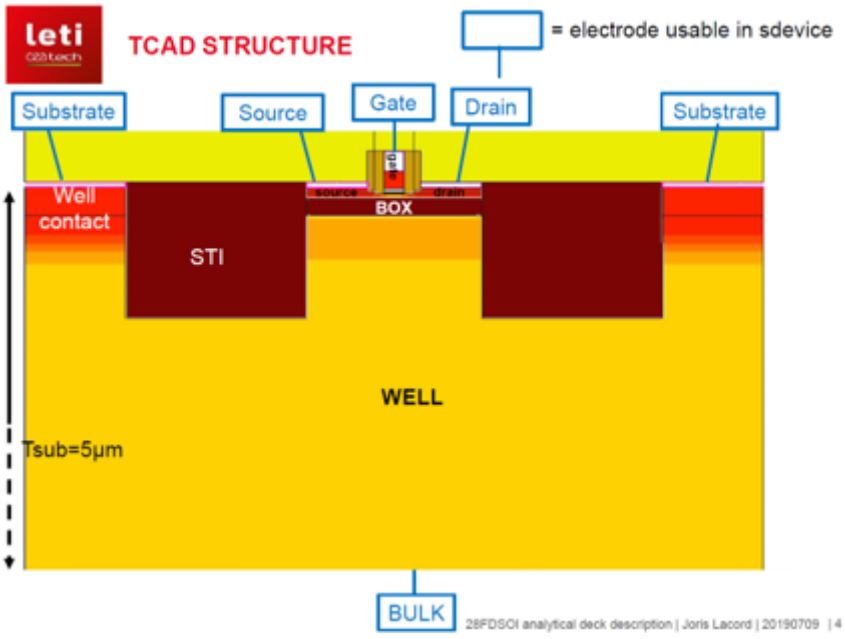

Fig. 2.1: Structure of the Synopsys Sentaurus deck provided by CEA-Leti

Figure 2.1 shows the 2D TCAD simulation structure. The 28FDSOI transistor is embedded in a $5\,\mu m$ thick substrate. The well contacts are isolated from the transistor with SiO_2-filled shallow trenches

(STI). The "substrate" and "bulk" electrodes in Fig. 2.1 are imposed $V = 0\,V$ for all simulations performed in this work.

A closer look on the transistor structure is shown in Fig. 2.2. LVT transistors are simulated in this work. Their $6.7\,nm$ thick Si channel is separated from the N-doped well by a $25\,nm$ thin buried oxide (BOX) [26]. The silicon nitride spacers separate the source and drain diffusion regions (indicated by S and D) from the channel, resulting in an underlapped structure.

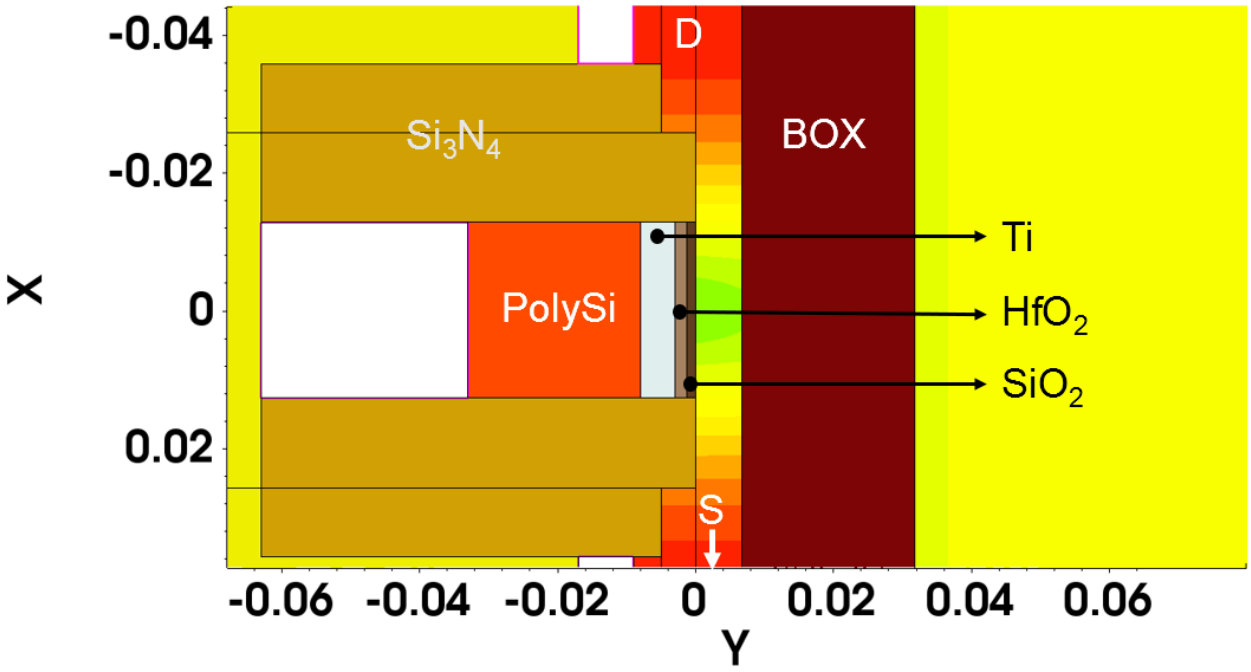

Fig. 2.2: Synopsys Sentaurus 2D transistor structure, $L_{mask} = 25\,nm$. The color scale shows the doping in the channel and S/D contacts. White regions indicate the electrodes where the potentials are fixed to bias the transistor. The X and Y axis scales are in μm.

The ideal transistor length is noted L_{mask} throughout this work. Due to the fabrication process (lithography), the corresponding actual length is given by $L_g = 0.9L_{mask} + 3\,nm$ (from CEA-Leti data) and is the one implemented in the TCAD simulation structures. The effective electrical length is then written $L_{eff} = L_g - \Delta L$ with ΔL the length reduction due to the extension of source and drain diffusions in the channel.

The phosphorous doping profile along the channel is shown in Fig. 2.3 (it is several orders of magnitude higher than the background Boron doping, not represented). The highly doped source and drain diffusion regions are clearly visible. They extend into the channel are seen to start merging for $L_{mask} < 25\,nm$ approximately. A high phosphorous doping is still present in the channel for longer transistors, effectively making it N-type. It is believed to be due to the N-well implantation, however the process simulations on which this result is based might not be accurate in such thin channels.

2.2 Physical models

Carrier transport is simulated with the drift-diffusion model, with quantization effects included using the density gradient quantization model (with default Sentaurus Device parameters). No self-heating is taken into account, a constant and uniform temperature $T = 300K$ is thus assumed everywhere in the device. Shockley-Read-Hall recombination and its dependance on doping is further included in the model [27].

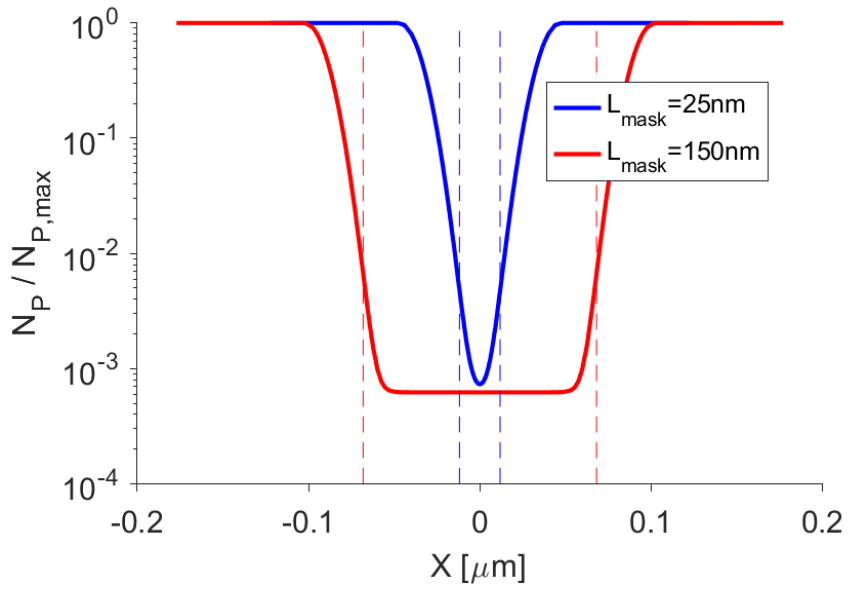

Fig. 2.3: Normalized phosphorous doping profiles along the channel, at a distance $Y = 1\,nm$ from the gate oxide for $L_{mask} = 150\,nm$ and $L_{mask} = 25\,nm$. Dashed lines indicate the corresponding effective lengths.

The initial deck assumes a very simplistic mobility model only taking into account phonon scattering as defined by default in Sentaurus Device

$$\mu_{cl} = \mu_L(\frac{T}{300K})^{-\zeta} \tag{2.1}$$

with μ_L hardcoded to $150\,cm^2/Vs$ (a typical value in short channel FDSOI transistors) and $\zeta = 2.5$ for electrons. Additionally, a modified mobility model is activated to take into account tunneling through semiconductor barriers:

$$\mu = \frac{\mu_{cl} + r\mu_t}{1 + r} \tag{2.2}$$

with μ_t a fitting parameter fixed to $0.05\,cm^2/Vs$ here and r defined in [27].

As the temperature is fixed at $T = 300K$ everywhere in the structure, this mobility model effectively results in $\mu = 150\,cm^2/Vs$ uniformly in the device. Although not physical, this model will be useful to simply evaluate mobility extraction procedures as presented in next chapters.

2.3 A more complete mobility model

2.3.1 Relevant additional mobility models

As mentioned earlier, a fully calibrated deck with complex mobility models and modified parameters has been developed at CEA-Leti, but was not available for this work. Redevelopping such a model would obviously be a huge and mostly pointless task in the frame of this work. Still, the very simple constant mobility model presented in the previous section doesn't account for many important mobility degradation phenomena, and its use for assessing the mobility extraction procedures might thus be limited.

Therefore, a first step in this work is to retrieve a more physical, qualitatively correct mobility model. It is not required to show absolute fitting with measures, but rather to reproduce the main mobility tendencies satisfyingly enough to enable meaningful study of the split CV mobility extraction technique.

To this end, the hardcoded mobility in the inital deck was removed and several physical mobility degradation models were then activated in the TCAD simulation setup, adding up following Matthiessen's rule. They will be briefly exposed here, readers are referred to chapter 15 in [27] for details of their implementation.

- High field velocity saturation is taken into account by the Canali model [28]. The driving field for electrons is computed by the gradient of the quasi-Fermi potential.
- Scattering by charged dopant ions is accounted for using the Masetti model [29]. It is of particular importance for our investigations considering the high doping levels in both source and drain diffusion regions and the channel.
- The thin layer mobility model is necessary to account for geometric quantization in channels only a few nm thick as simulated here [30]. It is used in complement to the Lombardi model for mobility degradation at interfaces due to the vertical field (acoustic phonon and surface roughness scattering)[31].
- (Carrier-carrier scattering was also activated with the default Conwell-Weisskopf model, see [27]. Its influence will be seen small in the next section.)

Figure 2.4 shows the spatial dependence of the mobility for $L_{mask} = 25\,nm$, $V_{DS} = 50\,mV$, $V_{GS} = 1.2\,V$. The influence of the source and drain doping (see Fig. 2.3) is clearly visible, as well as the mobility degradation close to the interface.

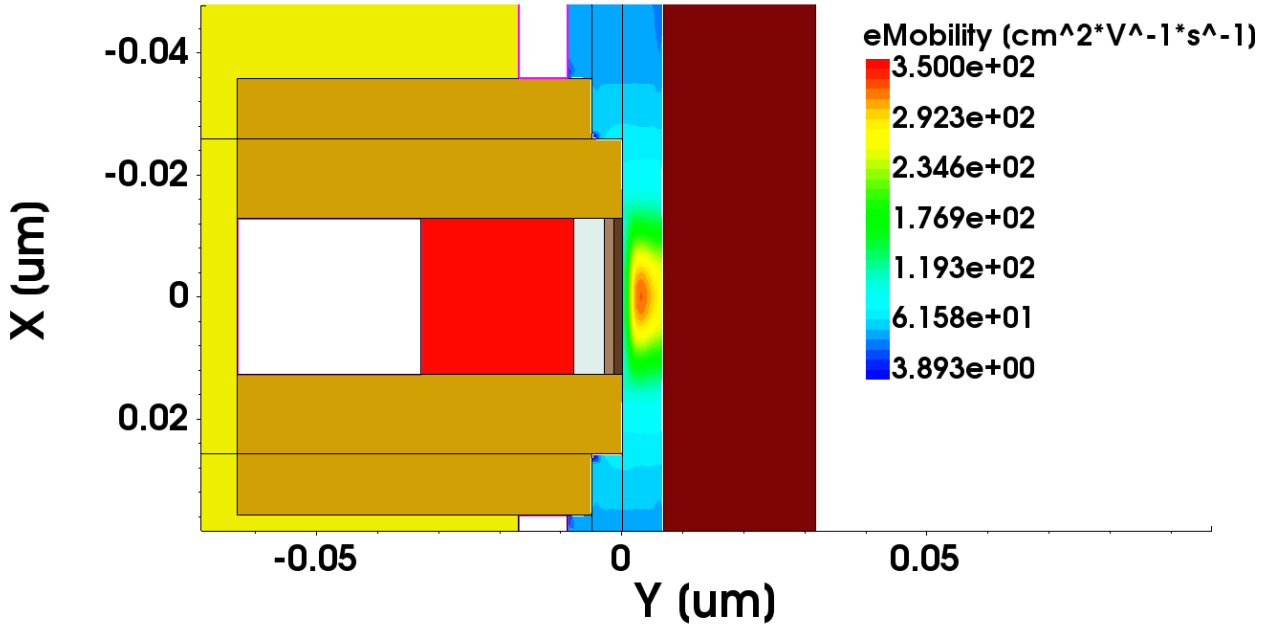

Fig. 2.4: Spatial dependence of the electron mobility in a $L_{mask} = 25\,nm$ transistor with $V_{DS} = 50\,mV$, $V_{GS} = 1.2\,V$

A way to estimate the effective mobility impacting the current is to compute the integral of the mobility over the intrinsic channel region weighted by the carrier density. One has

$$\mu_{vol} = \iint_S \mu(x,y)n(x,y)dxdy \,/\, \iint_S n(x,y)dxdy \tag{2.3}$$

Where $n(x,y)$ is the local free carrier density and S the effective channel area ($Y = [0, 6.7\,nm]$, $X = [-L_{eff}/2, L_{eff}/2]$, see Fig. 2.2). The resulting μ_{vol} for different transistor lengths is show on

Fig. 2.5. The observed decrease for lower lengths is explained by the increased impact of the source and drain diffusions which result in high doping in a larger fraction of the channel. The impact of this on R_{SD} and the extracted mobility will be discussed in more detail in Section 4.2.1.

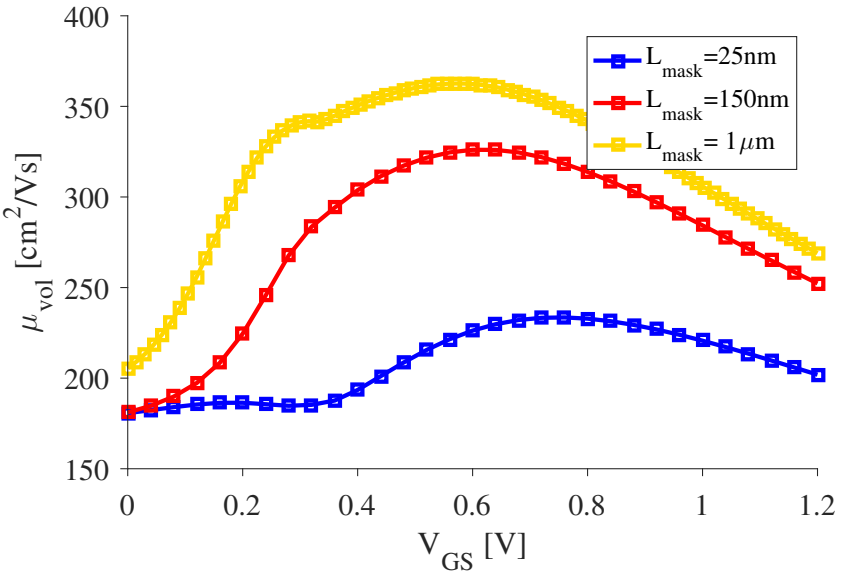

Fig. 2.5: μ_{vol} (Eq. (2.3)) from TCAD simulations of different transistor lengths.

2.3.2 Results and validation against UTSOI2.2 compact model

Split CV mobility extraction requires I-V curves in strong inversion and linear regime. In this work, the drain to source voltage will be fixed to $V_{DS} = 50\,mV$, and channel lengths down to $25\,nm$ will be considered.

The characteristics obtained by adding the different mobility models for such a $L_{mask} = 25\,nm$ transistor at $V_{DS} = 50\,mV$ are shown in figures 2.6 - 2.8. Velocity saturation and mobility degradation with doping are seen the be the major contributions to the total mobility reduction.

The obtained curves are compared to results of the UTSOI2.2 model [32][33]. Though the current and subthreshold slope are overestimated by all TCAD models, one finds qualitative agreement between the TCAD and UTSOI2.2 curves in strong inversion when accounting for all previously mentioned mobility reduction phenomena. Thus the developed mobility model (further called "full mobility model", as opposed to the inital constant mobility model) is considered satisfying enough for the purpose of this work.

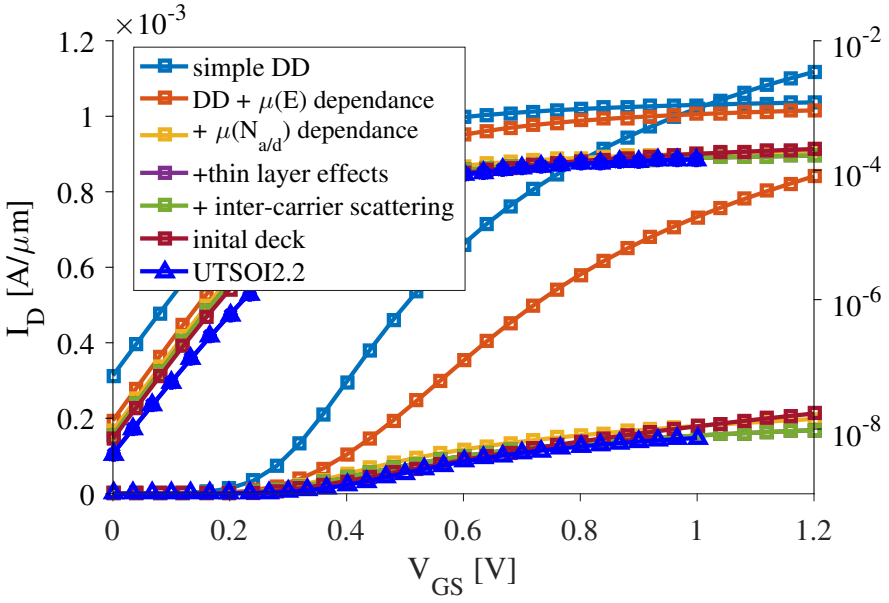

Fig. 2.6: TCAD current-voltage characteristics for $L_{mask} = 25\,nm$, $V_{DS} = 50\,mV$ with addition of different mobility models, compared to results from the inital deck (constant $\mu = 150cm^2/Vs$) and the UTSOI2.2 compact model. TCAD curves have been shifted by $+100\,mV$ to compensate for the V_{TH} difference with the UTSOI curves and enable easier comparison. "Simple DD" stands for the simple drift diffusion model, with the mobility fixed to the bulk silicon value. "$\mu(E)$" indicates high field saturation, "$\mu(N_{a/d})$" doping dependence (charged dopant ions scattering), "thin layer effects" mobility degradation at the interface due to the vertical field.

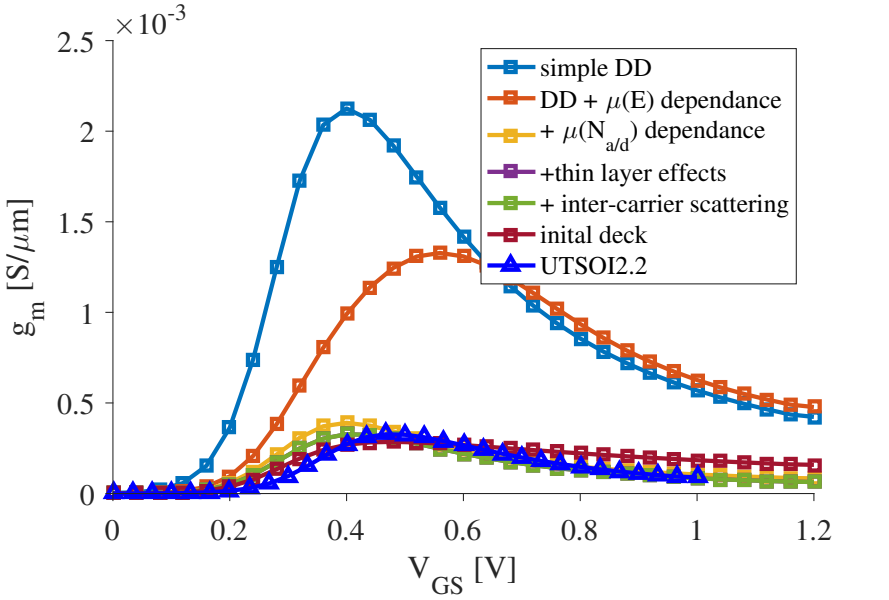

Fig. 2.7: TCAD gate transconductance-voltage characteristics for $L_{mask} = 25\,nm$, $V_{DS} = 50\,mV$ with addition of different mobility models, compared to results from the UTSOI2.2 compact model.

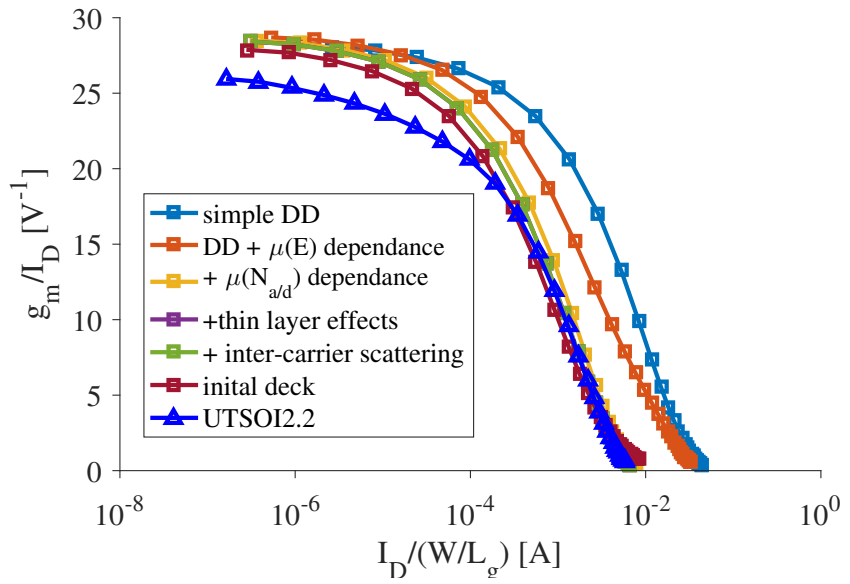

Fig. 2.8: TCAD g_m/I_D ratio with respect to the normalized current (the 2D simulation represents an equivalent $W = 1\,\mu m$) for $L_{mask} = 25\,nm$, $V_{DS} = 50\,mV$ with addition of different mobility models, compared to results from the UTSOI2.2 compact model.

2.4 Threshold voltage extraction

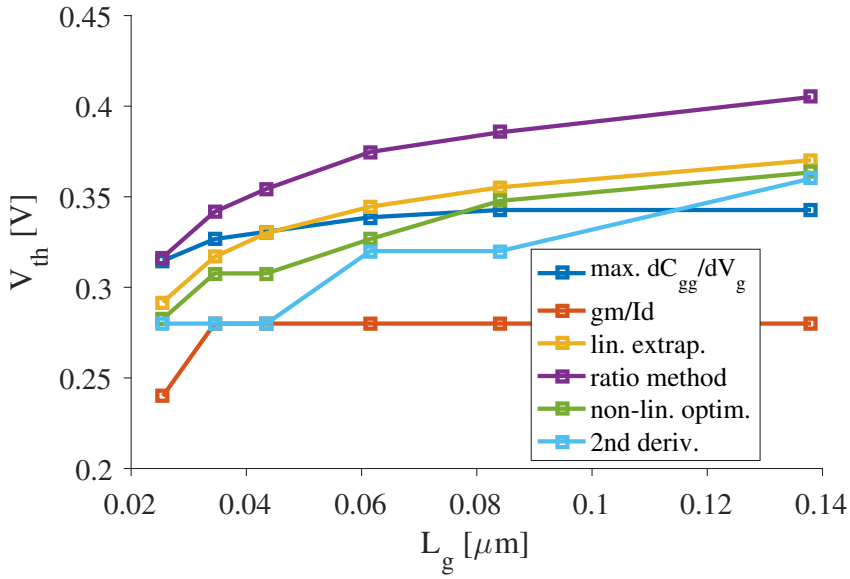

Fig. 2.9: V_{TH} extracted by several methods: maximum gate capacitance derivative, g_m/I_d method, linear extrapolation, ratio method, non-linear optimzation and second derivative method.

Figure 2.9 shows the threshold voltage V_{TH} extracted by several methods from the TCAD simulations. The maximum gate capacitance derivative relies on the $C_{gg}(V_{GS})$ curves, and is seen to give the lowest V_{TH} variation between $L_{mask} = 150\,nm$ and $L_{mask} = 25\,nm$ ($\Delta V_{TH} \approx 30\,mV$). This extraction method is deemed the best suited for the short transistors considered here, as the other current-based methods suffer from the impact of access resistances and mobilility variation with V_{GS}. Its application is shown in Fig. 2.10 below.

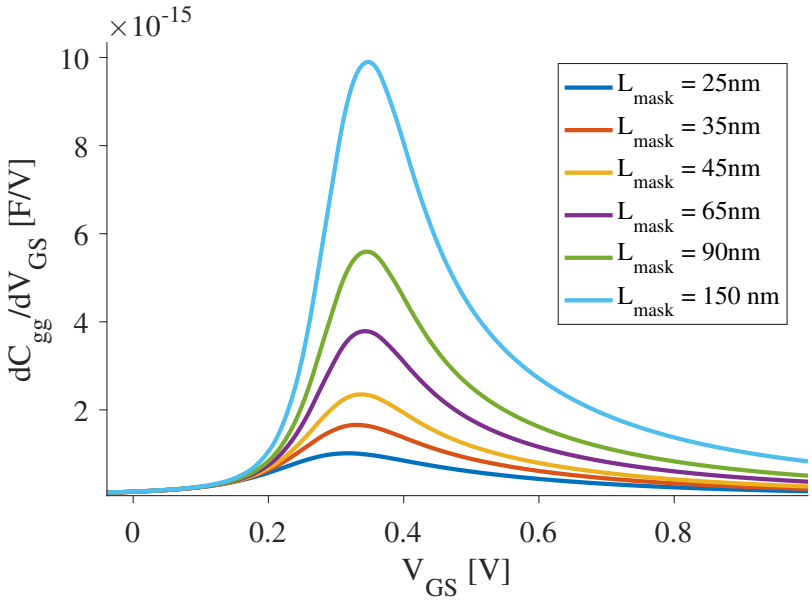

Fig. 2.10: V_{TH} extraction from the maximum of TCAD $\frac{dC_{gg}}{dV_g}$ curves

In all rigor, this extraction should be performed using the derivative of the intrisic gate capacitance dC_{ggi}/dV_g, but this thus requires the prior knowledge of C_{ggi}. Using the total gate capacitance C_{gg} will nevertheless be seen to give good results in the rest of this work (as discussed in Section 5.2.1, it can be confirmed *a posteriori* to give the same results as using C_{ggi}).
The extracted threshold voltages are shown in Table 2.1.

$L_{mask}\,[nm]$	25	35	45	60	90	150
$V_{TH}\,[V]$	0.315	0.327	0.33	0.339	0.343	0.343

Table 2.1: Threshold voltages extracted from the maximum of dC_{gg}/dV_g for different transistor lengths.

3 Simple split CV method

In this chapter, the conventional split CV method (as in [19, 20]) will be presented and applied to I-V and C-V curves extracted from the previously described 28FDSOI TCAD simulations. The underlying hypotheses of the effective length L_{eff}, intrinsic charge Q_i and access resistance R_{SD} extractions will be systematically highlighted, and the importance of correcting for the series resistance will be stressed.

This simple method will be shown unable to correctly extract the mobility for short transistors. This will form the main motivation behind the rest of this work, where the influence of different parasitics, mainly related to the underlapped structures, will be studied and corrected for.

3.1 Conventional split CV mobility extraction

The principle of the split CV method was briefly presented in the introduction and is recalled here. The extraction is performed in strong inversion and in linear regime, where the MOSFET current writes

$$I_D = \frac{W_{eff}}{L_{eff}} \mu_{eff} Q_i' V_{DS}' \tag{3.1}$$

with $Q_i' = \frac{Q_i}{W_{eff} L_{eff}}$ the inversion charge per unit area and $V_{DS}' = V_{DS} - R_{SD} I_D$ the effective drain to source voltage. Reworking this equation, one can write:

$$\mu_{eff} = \frac{L_{eff}^2 I_D}{Q_i V_{DS}'} \tag{3.2}$$

Thus one needs L_{eff}, Q_i and R_{SD} to compute the effective mobility μ_{eff}. The inversion charge Q_i is ideally obtained by integration of the intrinsic gate capacitance C_{ggi} from a starting voltage V_{GS}^* in accumulation (where C_{ggi} is zero):

$$Q_i(V_{GS}) \approx \int_{V_{GS}^*}^{V_{GS}} C_{ggi}(V) dV \tag{3.3}$$

In short nodes, C_{ggi} must thus be extracted from the total gate capacitance C_{gg} after elimination of the significant parasitic contributions [19, 20]. This important step is described in the next section.

3.2 Gate capacitance model

The total gate capacitance C_{gg} is constituted of the intrinsic gate capacitance $C_{ggi} = dQ_i/dV_{GS}$, needed for Q_i extraction, and the contribution of parasitics $C_{gg,par}$:

$$C_{gg}(V_{GS}, L_{eff}) = C_{ggi}(V_{GS}, L_{eff}) + C_{gg,par}(V_{GS}, L_{eff}) \tag{3.4}$$

Figure 3.1 shows the parasitic gate capacitances that are usually considered for advanced MOSFET's. One has overlap ($C_{gge,ov}$), outer fringing ($C_{gge,of}$) and inner fringing ($C_{gge,if}$, from the gate to the source/drain contacts through the channel) contributions. The total gate capacitance C_{gg} is then expressed as in [20]:

$$C_{gg}(V_{GS}) = C_{ggi}(V_{GS}, L_{eff}) + C_{gge,ov} + C_{gge,of}(L_{eff}) + C_{gge,if}(V_{GS}) \tag{3.5}$$

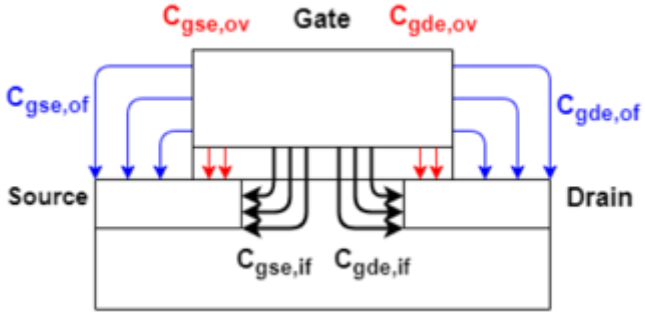

Fig. 3.1: Parasitic gate capacitances as modeled in [20]. Image taken from [23]

One usually eliminates the outer fringing and overlap capacitances by substracting the gate capacitance at a gate voltage $V_{GS,min}$ in accumulation from C_{gg}. The normalized gate capacitance $C_{gg,norm}$ is then defined as [20]:

$$\begin{aligned} C_{gg,norm}(V_{GS}, L_{eff}) &= C_{gg}(V_{GS}, L_{eff}) - C_{gg}(V_{GS,min}, L_{eff}) && (3.6)\\ &\approx C_{gg}(V_{GS}, L_{eff}) - C_{gge,ov} - C_{gge,of}(L_{eff}) && (3.7)\\ &\approx C_{ggi}(V_{GS}, L_{eff}) + C_{gge,if}(V_{GS}) && (3.8) \end{aligned}$$

Additionaly to the looked-for intrinsic gate capacitance, one thus still has the contribution of the inner fringing capcitance $C_{gge,if}$. Eq. (3.8) relies on several hypotheses:

- (Hyp.1) The outer fringing and overlap capacitances $C_{gge,of}$ and $C_{gge,ov}$ are considered independent of the gate voltage
- (Hyp.2) The inner fringin capacitance $C_{gge,if}$ is taken independent of the length L_{eff}
- (Hyp.3) The inner fringing capacitance $C_{gge,if}$ is assumed shielded at $V_{GS} = V_{GS,min}$ (in accumulation)
- (Hyp.4) The threshold voltage variation with L_{eff} is assumed low enough for the extraction to be performed at the same V_{GS} for all transistors.

(Hyp.2) will be discussed below and (Hyp.3), (Hyp.4) assessed at length further in this work.

Figure 3.2 shows the C_{gg} and $C_{gg,norm}$ versus gate voltage curves from TCAD small signal simulations at $f = 100\,kHz$ (the extraction frequency is of little importance here, as the extracted capacitance doesn't vary on the $10\,Hz - 10\,Ghz$ range, see Fig. 5.2). As in [20, 23], $V_{GS,min}$ in Eq. (3.6) was chosen as the lowest available gate voltage ($V_{GS,min} = -1.2\,V$).

Parasitic capacitances are seen to represent a significant part of the total gate capacitance for short transistors. For $L_{mask} = 25\,nm$, one has $\frac{C_{gg}(V_{GS}=-1\,V)}{C_{gg}(V_{GS}=1\,V)} = 42\%$.

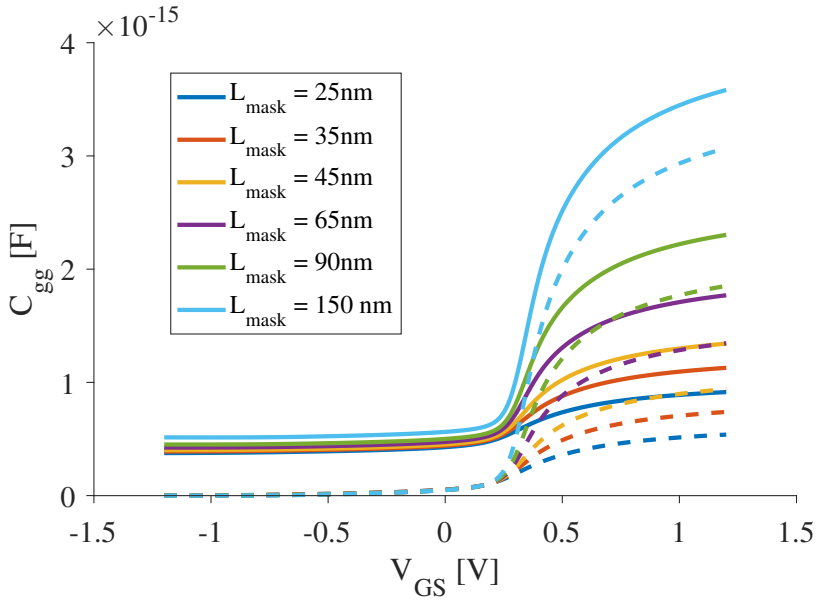

Fig. 3.2: C_{gg} (full) and $C_{gg,norm}$ (dashed) versus gate voltage from small signal TCAD simulation for different transistor lengths and $V_{DS} = 50\,mV$. The simulation is performed at $100\,kHz$ for gate voltages from $-1.2\,V$ to $1.2\,V$ by $33\,mV$ steps. Spline interpolation to 500 equally spaced points in $V_g = [-1.2\,V, 1.2\,V]$ is then performed.

In [20], Romanjek et al. proposed a method to get rid of the inner fringing $C_{gge,if}$ term in Eq. (3.8), considering it is length independent (see (Hyp.2)). One writes

$$C'_{gg,norm}(V_{GS}, L_{eff,1}) = \frac{C_{gg,norm}(V_{GS}, L_{eff,2}) - C_{gg,norm}(V_{GS}, L_{eff,1})}{L_{eff,2} - L_{eff,1}} L_{eff,1} \tag{3.9}$$

with $L_{eff,2}$ close to $L_{eff,1}$ to avoid large threshold voltage mismatch. The obtained capacitance $C'_{gg,norm}$ was then integrated to estimate the intrinsic charge Q_i.
This method was attempted by Vandermolen et al. on 28nm FDSOI transistors in [23], but resulted in difficulties as the value of $C_{gg,norm}$ was significantly modified in strong inversion after correction by Eq. (3.9). This unexpected behaviour was then attributed to length dependence of $C_{gge,if}$.

Figure 3.3a shows $C_{gg,norm}$ from TCAD simulations in a semilogarithmic scale, compared to curves extracted from the UTSOI2.2 model [32, 33]. The TCAD results indeed confirm what was obtained by Vandermolen et al. on 28nm FDSOI [23], namely that the extracted $C_{gg,norm}$ is dependent on the transistor length for low V_{GS}. Interestingly, Fig. 3.3a shows this behaviour is not reproduced by the UTSOI2.2 compact model.

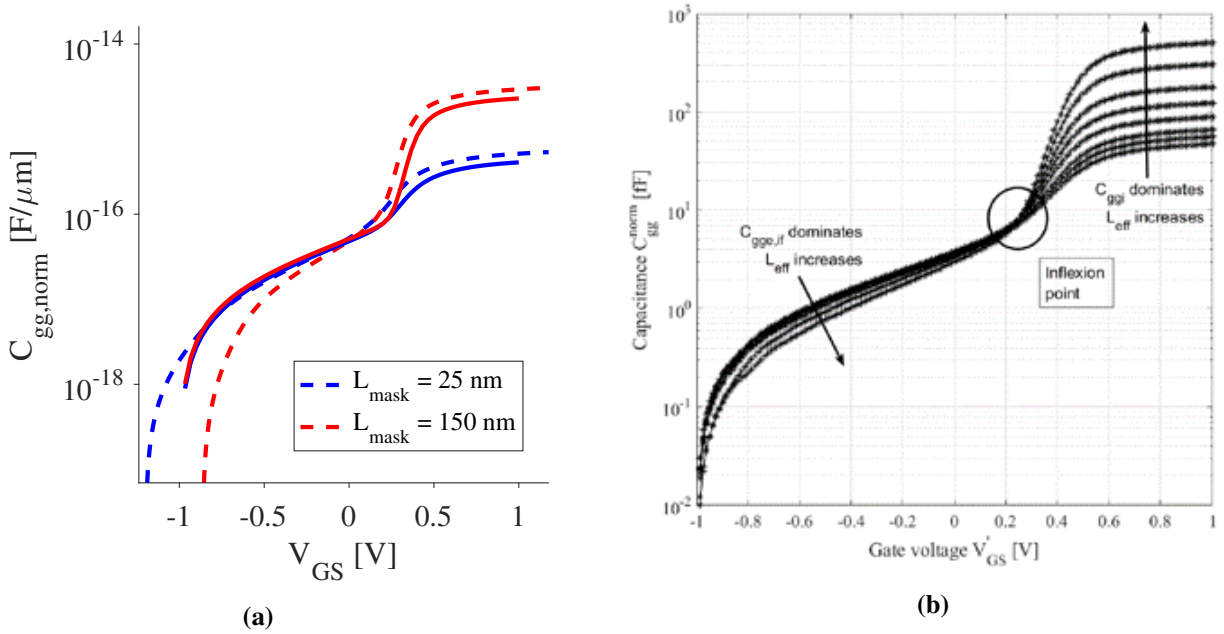

Fig. 3.3: Semilogarithmic $C_{gg,norm}$ versus gate voltage plots from **(a)** TCAD simulations (dashed), UTSOI2.2 model (full) and **(b)** Measurements on 28FDSOI from [23]. $V_{DS} = 50\,mV$ and $20\,mV$ respectively.

Despite this extracted variation of $C_{gg,norm}$ with the gate length, a "global equivalent" of Eq. (3.9) (i.e. based on linear regression on C_{gg} against all transistor lengths) was later proposed by Vandermolen et al. and successfully applied on 28FDSOI measurements [34]. This method will be confirmed useful for C_{ggi} extraction further in this work (Chapter 5).
As the values of $C_{gg,norm}$ are in any case very low in the voltage range where it is length dependent, they are not expected to have significant impact on the final extraction. The difficulties to apply Eq. (3.9) observed by Vandermolen et al. are thus rather believed to be due to voltage threshold mismatch.

In the next section, one will go on with $C_{gg,norm}$ from the conventional method to continue its assessment as proposed in this chapter.

3.3 Intrinsic charge extraction

In [23], the integration of $C_{gg,norm}$ was performed with a starting voltage V_{GS}^* from which the intrisic gate capacitance is considered to dominate over the inner fringing contribution ("inflexion point" on Fig. 3.3b). One thus has:

$$Q_i(V_{GS}, L_{eff}) = \int_{V_{GS}^*}^{V_{GS}} C_{ggi}(V, L_{eff})dV \approx \int_{V_{GS}^*}^{V_{GS}} C_{gg,norm}(V, L_{eff})dV \tag{3.10}$$

The underlying assumptions of this method are thus

- (Hyp.5) $Q_i(V_{GS} = V_{GS}^*)$ is negligible
- (Hyp.6) $C_{gge,if}$ is small with respect to C_{ggi} for $V_{GS} > V_{GS}^*$

It corresponds to the usual integration (as performed in [19, 20]) when V_{GS}^* is equal to $V_{GS,min}$ from Eq. (3.6). The choice of V_{GS}^* results in a trade off for the validity of (Hyp.5) and (Hyp.6). Indeed, $C_{gge,if}$ is known to decrease to zero when moving to stronger inversion because of screening by the inversion layer (see Section 5.1). However, the integral of C_{ggi} then gets important and (Hyp.5)

becomes a worse assumption. From Fig. 3.3a, V^*_{GS} is fixed at $0V$ in our case (where C_{ggi} is small (Fig. 3.2) and no dependance on length is seen).

The validity of (Hyp.6) and the impact of the inner fringing capacitance on the extraction will be discussed at length in Chapter 5.

3.4 Effective length L_{eff} extraction

The transistor effective length writes $L_{eff} = L_g - \Delta L$ with ΔL the length reduction due to the extension of source and drain diffusions in the channel. It is typically extracted from the estimated intrinsic capacitance in strong inversion (at $V_{GS} = V_{GS,max}$) and at $V_{DS} = 0V$. From Eq. (3.8), one has ($C_{gge,if}$ is shielded by the inversion layer, see Section 5.1)

$$C_{gg,norm}(V_{GS} = V_{GS,max}) \approx C_{ggi}(V_{GS} = V_{GS,max}) = C_{ox}(L_g - \Delta L) \tag{3.11}$$

with C_{ox} the equivalent gate oxide capacitance. This expression again relies on (Hyp.1-4) from Eq. (3.8).
Performing a linear interpolation on the $C_{gg,norm}$ versus L_g curves then enables to extract ΔL as shown on Fig. 3.4. With $L_{mask} = [25,\ 35,\ 45,\ 65,\ 90,\ 150]\ nm$, one obtains $\Delta L = 1.8\,nm$.

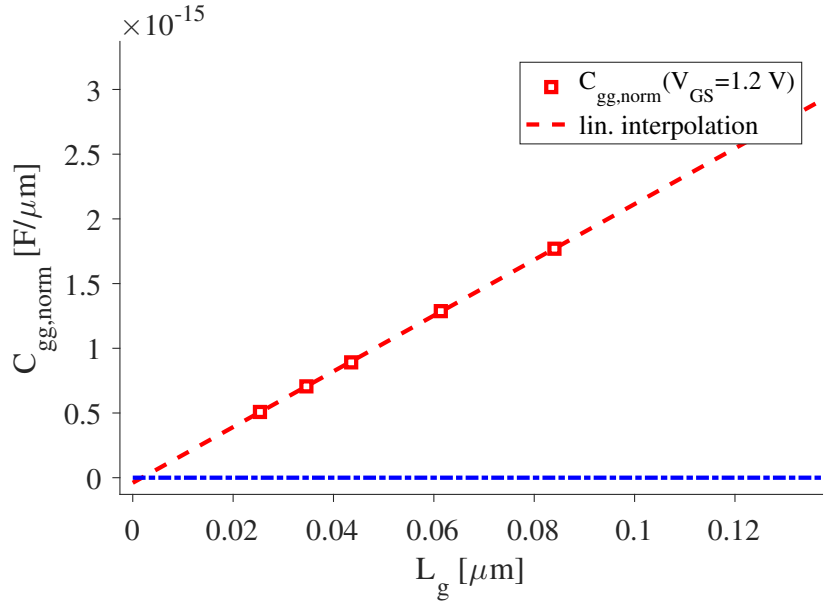

Fig. 3.4: L_{eff} extraction from linear interpolation of TCAD $C_{gg,norm}(V_{GS} = 1.2\,V, V_{DS} = 0\,V)$ versus L_g data. The blue line indicates the zero on the capacitance axis.

The linear fitting of the data is evaluated in Fig. 3.5, where ΔL is extracted using an increasing number of lengths starting from the two smallest in $L_{mask} = [25,\ 35,\ 45,\ 65,\ 90,\ 150]\ nm$ and adding the following ones. ΔL is reduced by 17% from when all lengths are used to when only the two smallest are considered. Part of this $0.3\,nm$ variation could be attributed to (Hyp.4) (see Section 6.1), but it is in any case small compared to the considered gate lengths.

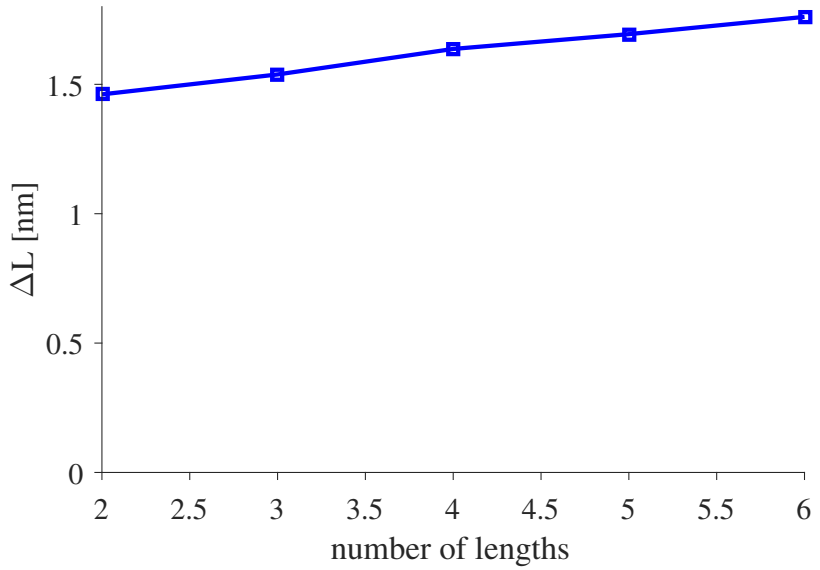

Fig. 3.5: ΔL extracted from linear interpolation of TCAD $C_{gg,norm}(V_{GS} = 1.2\,V, V_{DS} = 0\,V)$ versus the number of lengths used.

3.5 Extraction of access resistance R_{SD}

Correcting for the access resistance $R_{SD} = R_S + R_D$ is of primary importance in short transistors as it dominates their total resistance $R_m = V_{DS}/I_D$. Figures 3.6 and 3.7 show the mobility obtained by split CV with Q_i and L_{eff} as extracted in the previous sections while neglecting R_{SD} (thus using $V'_{DS} = V_{DS} = 50\,mV$ in Eq. (3.2)). From Fig. 3.6, it is seen that the extracted mobility is then severly underestimated for the shorter transistors. The same effect is shown with the full mobility model on Fig. 3.7 As a side note, on this figure one also remarks the good match between values extracted from TCAD simulation and the UTSOI2.2 compact model, which further validates the previously described mobility model.

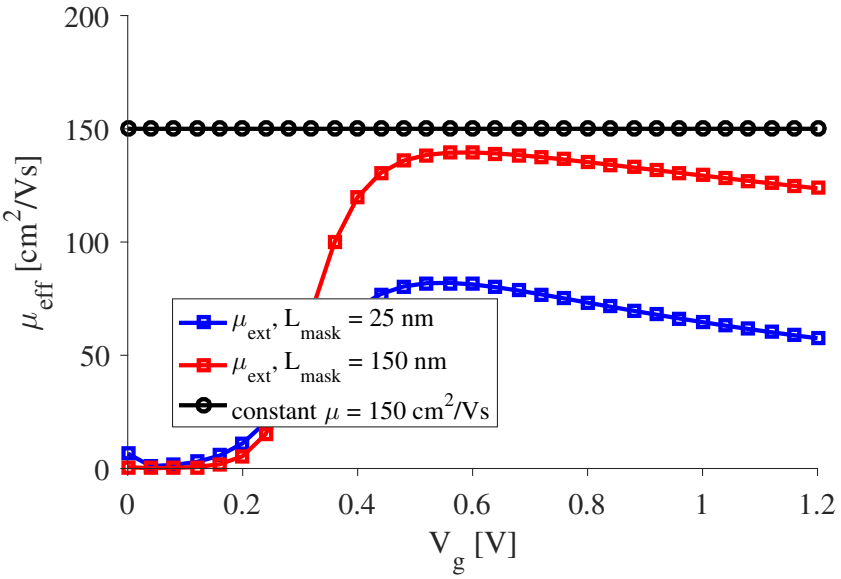

Fig. 3.6: Split CV extracted mobility μ_{ext} without R_{SD} correction for the simple constant mobility model ($\mu = 150 cm^2/Vs$ implemented in TCAD)

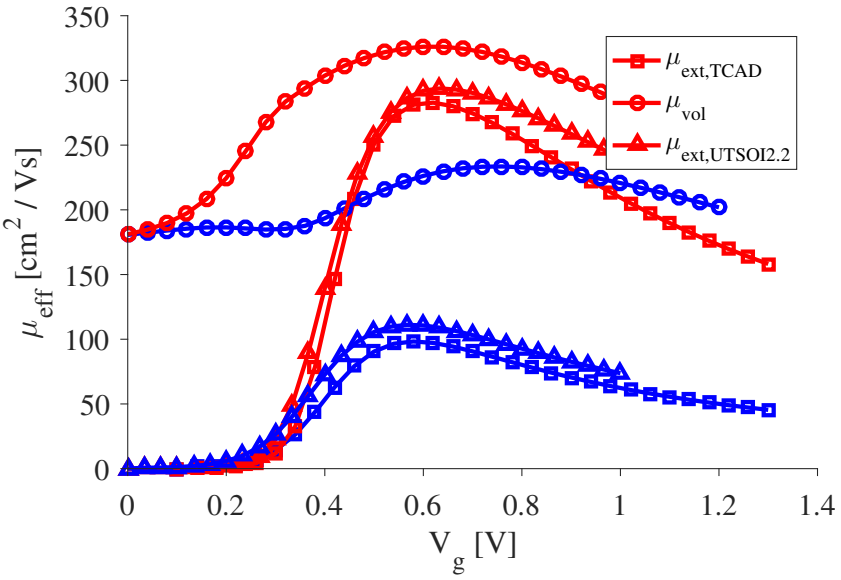

Fig. 3.7: Mobility extracted by split CV without R_{SD} correction for the full mobility model. TCAD extracted μ_{ext} (circles) is compared to the mobility extracted from the UTSOI2.2 compact model (triangles) and μ_{vol} implemented in TCAD (circles). TCAD curves have been shifted by $+100\,mV$ to correct for the V_{TH} shift w.r.t. the UTSOI2.2 curves and enable easier comparison. Blue and red curves are for a $L_{mask} = 25\,nm$ and $L_{mask} = 150\,nm$ transistor respectively.

Numerous R_{SD} extraction methods exist and some of them will be discussed for our purpose in Section 4.1. Here, we start with the simple total resistance method [35]. From Eq. (3.1) and $V'_{DS} = V_{DS} - R_{SD}I_D$, one can write

$$R_m = V_{DS}/I_D = R_{channel}(V_{GS}, L_{eff}) + R_{SD} \tag{3.12}$$

where, in strong inversion :

$$R_{channel} \approx L_{eff}/(\mu_{eff} W_{eff} C'_{ox}(V_{GS} - V_{TH})) \tag{3.13}$$

One can thus extract R_{SD} by linear interpolation of R_m versus L_{eff}.
A single value of R_{SD} is usually extracted from the maximum gate voltage, as shown on Fig. 3.8 for the full mobility model.
One obtains $R_{SD} = 248\,\Omega\mu m$ from the full mobility model TCAD simulations (Fig. 3.8), in good agreement with $R_{SD} = 259\,\Omega\mu m$ extracted from the UTSOI2.2 compact model. As expected, it is seen that the access resistance dominates the total resistance R_m in short transistors: for $L_{mask} = 25\,nm$, R_{SD} represents 83% of $R_m = 299.7\,\Omega$. The simple CEA model gives only $R_{SD} = 141\Omega\mu m$, which is not a physical value seen the simplistic mobility model (that notably doesn't consider doping dependence).

The total resistance method used here implies the following approximations:

- (Hyp.4) The threshold voltage variation with L_{eff} is assumed low enough for the extraction to be performed at the same V_{GS} for all transistors.
- (Hyp.7) The mobility μ_{eff} is assumed independent of L_{eff}
- (Hyp.8) R_{SD} is extracted as a single value, considering no dependence on V_G.

The excellent linearity of the R_m versus L_{eff} plot (Fig. 3.8) is a strong indication in favour of (Hyp.7). This assumption and (Hyp.8) will be discussed further in this work (Section 4.2.1).

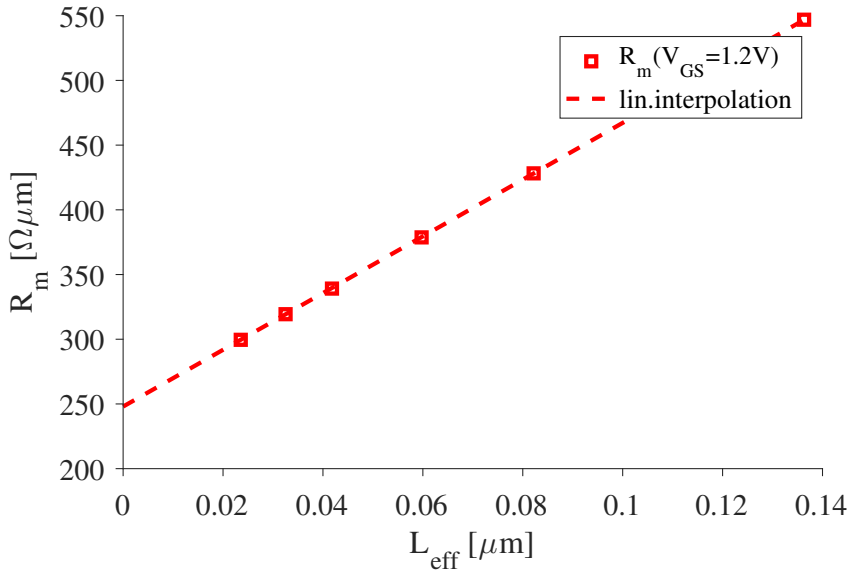

Fig. 3.8: R_{SD} extraction from TCAD simulations with the full mobility model using the total resistance method. $V_{DS} = 50\,mV$

3.6 Results of conventional split CV method

Correcting for R_{SD} is performed by writing $I_D^{'} = I_D/(1 - I_D R_{SD}/V_{DS})$ in Eq. (3.2). This is mathematically equivalent to using $V_{DS}^{'} = V_{DS} - R_{SD} I_D$ [20].
Figure 3.9 and 3.10 compare the extracted mobilities before and after this R_{SD} correction. One remarks the major impact on the extracted mobility curves.

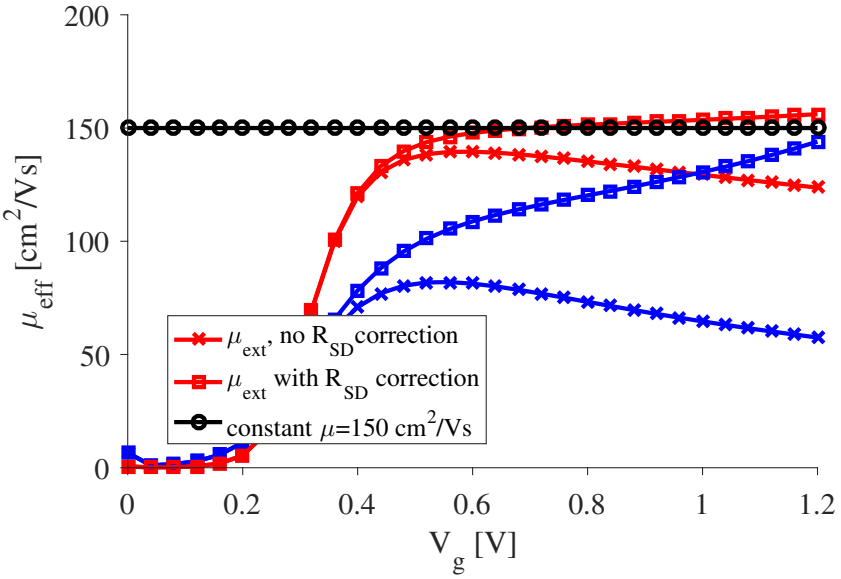

Fig. 3.9: Extracted mobility before (crosses) and after (squares) correction for a constant R_{SD} in the simple mobility model, compared with the constant mobility value imposed in TCAD (black circles). Blue curves indicate $L_{mask} = 25nm$, red curves $L_{mask} = 150nm$

The simple split CV method with constant R_{SD} correction extracts μ_{eff} in good qualitative agreement with the effective mobility implemented in TCAD for the long ($L_{mask} = 150\,nm$) transistor. However, the method proves insufficient to extract the mobility in a $L_{mask} = 25\,nm$ node. Its extracted μ_{eff}

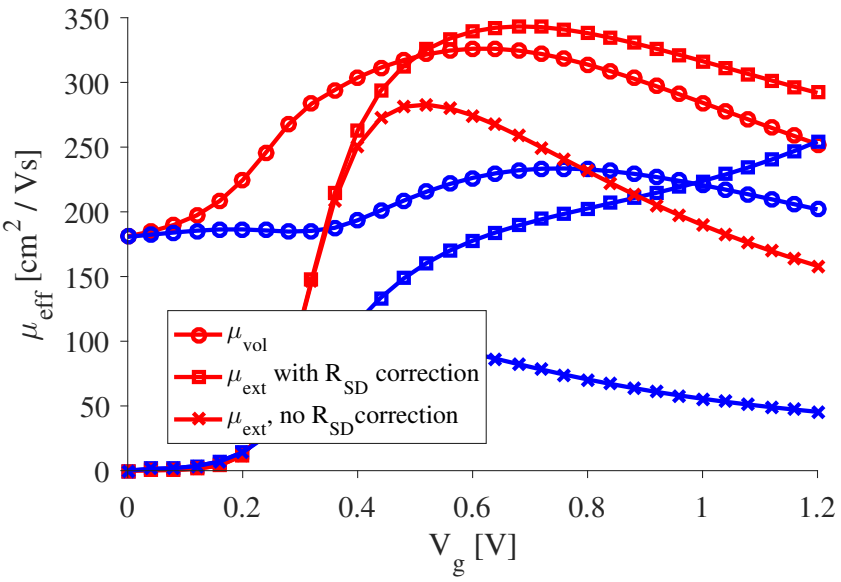

Fig. 3.10: Extracted mobility before (crosses) and after (squares) correction for a constant R_{SD} in the full mobility model, compared with μ_{vol} from TCAD (circles). Blue curves indicate $L_{mask} = 25nm$, red curves $L_{mask} = 150nm$.

indeed shows an unphysical behaviour after R_{SD} correction.

3.7 Summary and conclusion

This chapter presented the application of a conventional split CV method with constant R_{SD} extraction to TCAD simulations of 28FDSOI transistors. One systematically mentioned the approximations underlying the different extractions. This simple method was shown unable to extract the mobility correctly in a short ($L_{mask} = 25nm$) transistor.

This thus forms the motivation for the rest of this work. In the following chapters, it will be studied how this limitation of the simple split CV method for shorter transistors stems from the increased impact of parasitic effects neglected by its approximations.

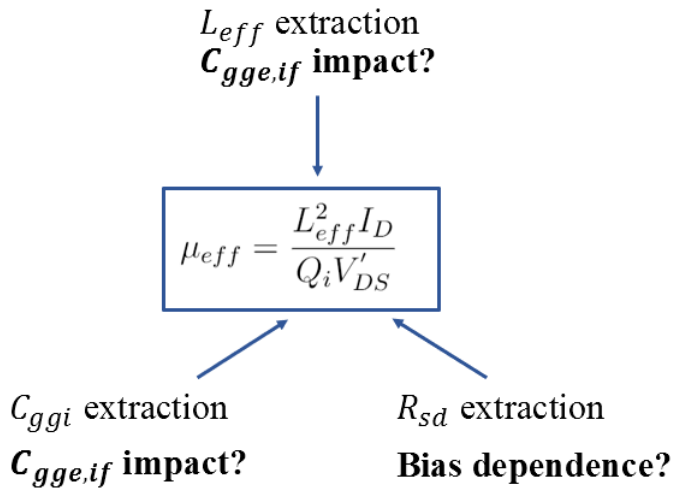

Fig. 3.11: Impact of parasitics on split CV μ_{eff} extraction

TCAD simulations will prove a powerful tool to confirm results from the litterature and assess the validity of these approximations by leveraging deeper insights into the device physics. Most difficulties will be shown to be related to the underlapped structure of the considered devices. As represented in Fig. 3.11, the influence of the inner fringing capacitance $C_{gge,if}$ and the bias dependence of the access resistance R_{SD} will notably be discussed in the next chapters.

4 Impact and correction of the series access resistance

In the previous chapter, the simple total resistance method was used to extract a bias-independent access resistance R_{SD}. After correcting for it, the split CV method enabled qualitative extraction of the mobility in long ($L_{mask} = 150\,nm$) transistors. However, the method was shown unsuitable for short transistors as the extracted mobility shows an unphysical behaviour.

Here, we will start by comparing different R_{SD} extraction procedures, and confirm the suitability of the total resistance method to extract R_{SD} from the TCAD simulations. The bias dependence of R_{SD} will be shown to be a major factor impacting mobility extraction in short transistors, in agreement with trends reported in literature. Improved results taking this dependence into account will indeed be seen to correct for the unphysical extracted mobility behaviour.

4.1 Comparison of access resistance extraction methods

Many different R_{SD} extraction methods have been proposed in literature, both from DC and AC measurements [23, 35]. Some of them were compared experimentally for 28FDSOI in [23].
In this section, we will show and compare results from the simple total resistance method (using DC I-V curves) and cold fet method proposed in [36] (using AC S-parameters).

4.1.1 Total resistance method (DC)

The total resistance method was described in Section 3.5. One has:

$$R_m = V_{DS}/I_D = R_{channel}(V_{GS}, L_{eff}) + R_{SD}$$

where, in strong inversion and linear regime :

$$R_{channel} \approx L_{eff}/(\mu_{eff} W_{eff} C'_{ox}(V_{GS} - V_T))$$

R_{SD} can thus be extracted by linear interpolation of R_m versus L_{eff} (Method 1) or $1/(V_{GS} - V_T)$ (Method 2). Both approaches rely on implicit assumptions:

- Method 1 assumes μ_{eff} is independent of L_{eff} (Hyp.7 in Section 3.5)
- Method 1 neglects the dependence of V_{TH} on the transistor length (Hyp. 4). In all rigor $R_m(V_{ov})$ should thus be used.
- (Hyp.9) Method 2 neglects μ_{eff} variation with $V_{ov} = V_{GS} - V_{TH}$
- Method 1 and method 2 extract a single, bias-independent R_{SD} value (Hyp.8 in Section 3.5)

- Method 1 and 2 rely on proper extraction of L_{eff}, and thus inherit (Hyp.1-3), see Section 3.4

Results of method 1 were presented in Section 3.5. Good linearity of the total resistance R_m versus L_{eff} was observed and the values extracted from the full TCAD model agreed well with the ones from the UTSOI2.2 compact model.

Method 2 first requires to extract the threshold voltage V_{TH}. This was previously discussed in Section 2.4. The maximum of dC_{gg}/dV_g was motivated to be the best suited method for the considered short transistors. The threshold voltages presented in Table 2.1 are thus used here.
One thereafter needs to select a minimum gate voltage overdrive $GVO_{min} = (V_{GS} - V_{TH})_{min}$ limiting the extraction to strong inversion.

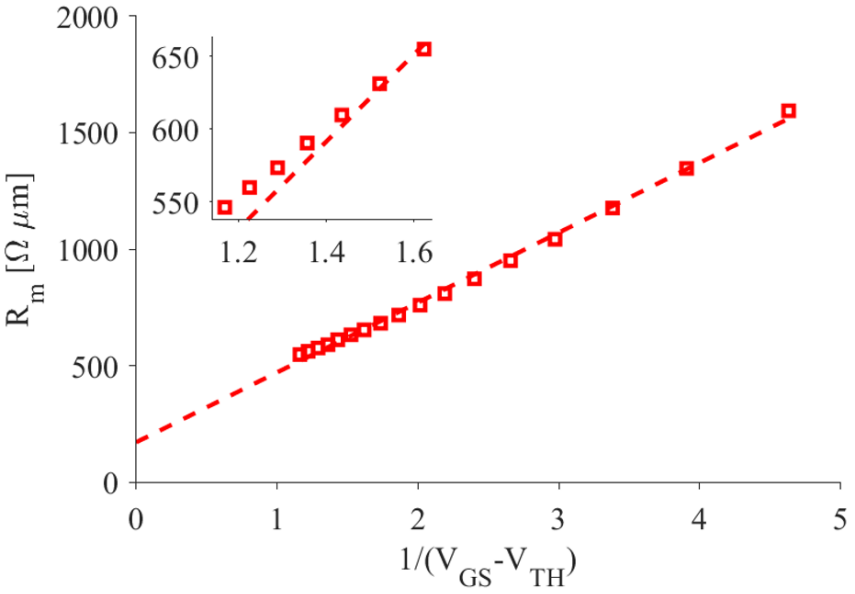

Fig. 4.1: Extraction of R_{SD} with method 2 from TCAD simulations (full mobility model) for $L_{mask} = 150\,nm$. $GVO_{min} = 0.2\,V$ was deliberately chosen low to highlight the deviation from the linear fit for increasing gate voltage overdrive.

Figure 4.1 shows the application of the method to a $L_{mask} = 150\,nm$ transistor. As shown on the inset, the total resistance values deviate from the linear fit for increasing gate voltage overdrives. As a consequence, the extracted R_{SD} values will increase when choosing a higher GVO_{min}.
Selecting a high GVO_{min} ensures the device is effectively biased in strong inversion, but reduces the number of points for linear interpolation. This could be alleviated using a smaller gate voltage step in the I_D-V_G curves. Here, the step was limited to $33\,mV$ to keep reasonable TCAD simulation times, and GVO_{min} is thus practically limited to maximum $0.5\,V$. $GVO_{min} = 0.4\,V$ is chosen as a compromise in the following.

The dependence on the gate voltage overdrive is shown in figure Fig. 4.2, and implies sensitivity of the method to the V_{th} extraction. This has been discussed at length in [23]. The extracted values vary significantly between the different lengths, increasing by more than 30% from $L_{mask} = 25\,nm$ to $L_{mask} = 150\,nm$ in the case of TCAD with $GVO_{min} = 0.5V$.

4.1.2 Cold FET method (AC)

The cold FET method was introduced by Bracale et al. in [36], and its underlying assumptions reviewed in detail [23]. The most notable one is to consider that the intrinsic output conductance g_{dsi} is directly proportionnal to $V_{GS} - V_{TH}$ in strong inversion, neglecting the dependence of μ_{eff} on the

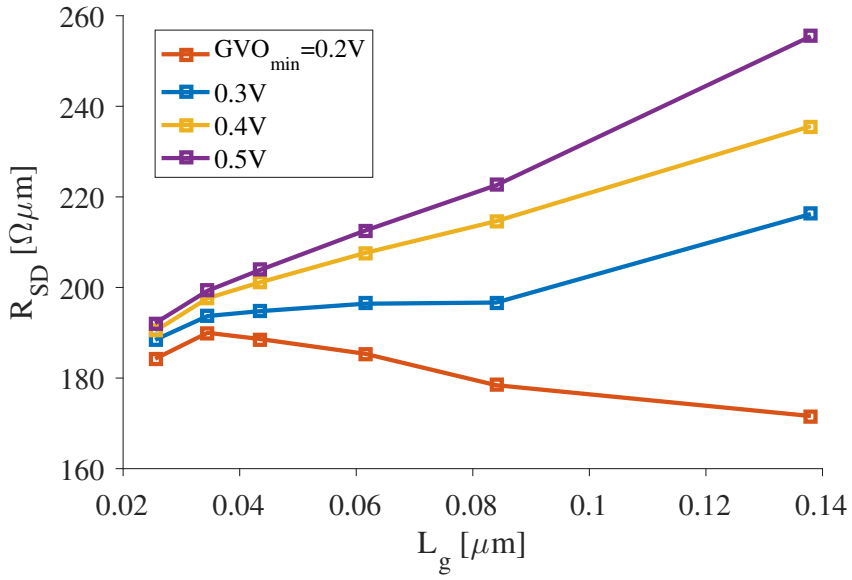

Fig. 4.2: R_{SD} extracted from TCAD (full mobility model) by method 2 for different minimum gate voltage overdrives and transistor lengths.

gate voltage (Hyp.9). It is further assumed that in "cold regime", i.e. at $V_{DS} = 0\,V$, the intrinsic transconductance $g_{mi} = 0$ and $C_{gd} = C_{gs}$. Based on a small signal model of the "cold" FET (at $V_{DS} = 0V$) in strong inversion, one then has [36]:

$$Re(Z_{22}) = R_{SD} + \frac{1}{g_{dsi}} \tag{4.1}$$

$$Re(Z_{12}) = R_S + \frac{1}{2g_{dsi}} \tag{4.2}$$

$$Re(Z_{22} - Z_{12}) = R_D + \frac{1}{2g_{dsi}} \tag{4.3}$$

Where port 1,2 refer to the gate and drain contacts respectively and the model is referenced at the source. g_{dsi} is the intrinsic output conductance of the device. It tends to infinity when L_{eff} or $1/(V_{GS} - V_{th})$ tends to zero. Equation (4.1) can then be used to extract R_{SD} from linear interpolation against L_{eff} (Method 3) or $1/(V_{GS} - V_{th})$ (Method 4).

AC simulations were performed in TCAD to extract the Y parameters of the transistor at $100\,kHz$ (see Section 3.2 and Fig. 5.2, the extraction frequency doesn't bear much importance here). After inversion of the Y matrix to Z matrix, $Re(Z_{22})$ is used for the linear interpolations (extractions with $Re(Z_{12})$ confirmed $R_S \approx R_D \approx R_{SD}/2$).

Application of the method 3 is shown in Fig. 4.3. As for method 1, the linearity of the $Re(Z_{22})$ versus L_{eff} plot is excellent. The extracted value $R_{SD,meth2} = 246\,\Omega\mu m$ is very close to the previously extracted $R_{SD,meth1} = 248\,\Omega\,\mu m$.
Figure 4.4 presents method 4 applied on a $L_{mask} = 150\,nm$ transistor. As for method 2, a minimal GVO_{min} must be chosen to ensure bias in strong inversion while keeping a sufficient number of points for the linear interpolation. In Fig. 4.4, $GVO_{min} = 0.2V$ is again deliberately chosen low to better show the deviation from the linear fit (similar to method 2, see Fig. 4.1). It is less visible here as S-parameters were simulated only to $V_{GS} = 1.2\,V$ while $I - V$ curves were extracted to $V_{GS} = 1.2/, V$. One could thus again expect sensitivity on GVO_{min} and hence on the extraction of the threshold voltage V_{TH}.
The dependence of the extracted R_{SD} on the length is very similar to that of method 2 (see Fig. 4.5).

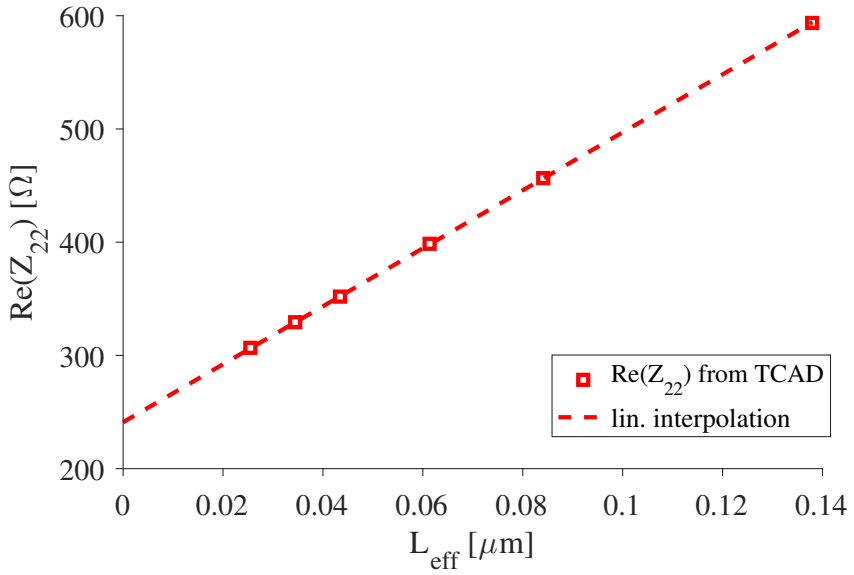

Fig. 4.3: Extraction of R_{SD} from TCAD simulations (full mobility model) with method 3 ($f = 100\,kHz$,$V_{DS} = 50\,mV$)

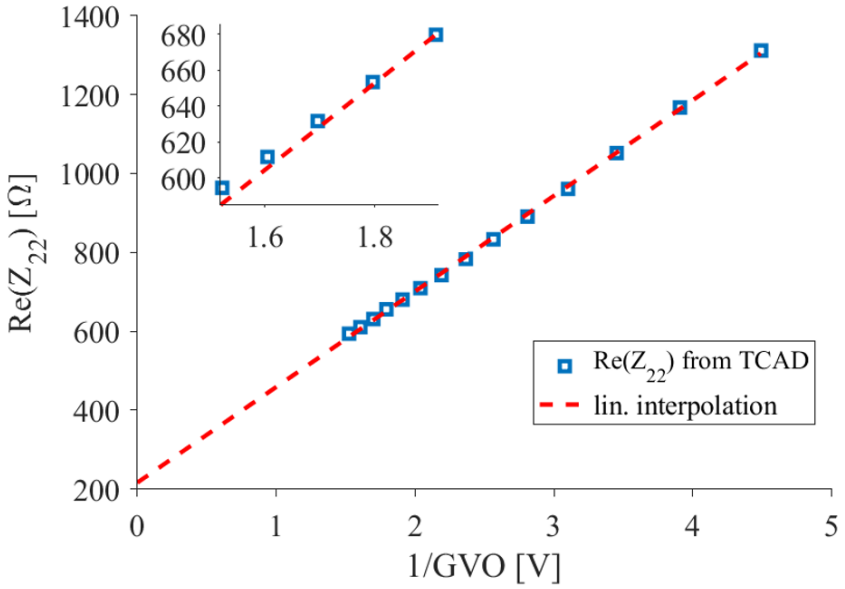

Fig. 4.4: Extraction of R_{SD} with method 4 (full mobility model). $L = 150\,nm$, $GVO_{min} = 0.2\,V$ deliberately chosen low to show the deviation from linear fitting ($f = 100\,kHz$,$V_{DS} = 50\,mV$)

4.1.3 Comparison

A comparison between the four discussed R_{SD} extraction methods is presented in Fig. 4.5. The first observation is the good agreement between values extracted from DC (I-V) and AC (Y-parameters) methods. Methods 2 and 4, based on regression against $1/(V_{GS} - V_{TH})$, give unexpected significant variations of R_{SD} with the gate length. They also showed deviations from the linear relation, resulting in sensitivity on the chosen minimum overdrive voltage and extraction of V_{TH}.

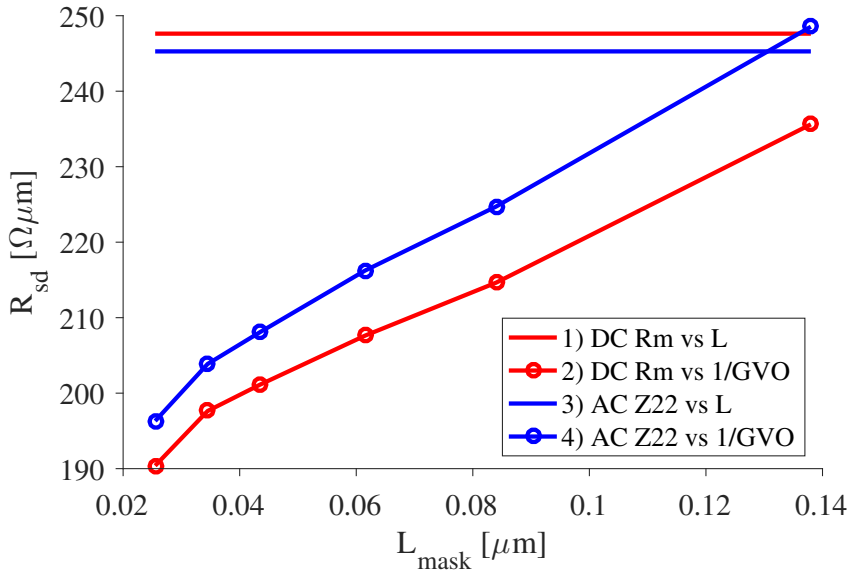

Fig. 4.5: Comparison of R_{SD} values extracted with methods 1-4 (full mobility model). Methods 1 and 3 give a single value independent of the length, represented here by a constant line. $GVO_{min} = 0.4V$ for methods 2 and 4.

Methods 1 and 3, based on regression versus L_{eff}, both show excellent linearity and give close results in good agreement with values extracted from the UTSOI2.2 compact model ($259\,\Omega\mu m$). Very importantly, they also enable extraction of R_{SD} in function of the gate bias. As will be shown in the next section, this is a major factor for mobility extraction in short channel transistors. Method 1 (total resistance versus L_{eff}) has been employed in litterature for such investigations and will therefore be used in the rest of this work.

4.2 Importance of bias dependence

4.2.1 Bias dependence of the FDSOI access resistance

Up to now, the values of R_{SD} have been considered independent of the gate bias. The total resistance method was used at $V_{GS} = V_{GS,max}$ to extract R_{SD} and correct for it in the split CV mobility extraction procedure. It notably relies on 1) proper extraction of L_{eff} and 2) the hypothesis that the effective mobility μ_{eff} is independent of L_{eff} (Hyp.7, see Section 4.1).
This assumption is backed by the excellent linearity of the total resistance R_m versus L_{eff}, as will be discussed further in this section. As seen in Section 3.6, after constant R_{SD} correction the mobility could be extracted in qualitative agreement with the TCAD models for a $L_{mask} = 150\ nm$ transistor. However, the method remained problematic in a $L_{mask} = 25\ nm$ device.

In [37], Fleury et al. proposed to extract R_{SD} from linear interpolation against $1/\beta$, where $\beta = \mu_{eff} C_{ox} W/L_{eff}$ takes into account possible variation of μ_{eff} with the gate length. However, extraction of β relies on the assumption. that R_{SD} is weakly dependent on the gate bias.
In [10], Monsieur et al. evidenced the important bias dependence of R_{SD} from TCAD simulations of FDSOI structures, geometrically similar to the ones considered in this work. Channel doping was made uniform and S/D junctions abrupt, thus generating a uniform channel where μ_{eff} is not expected to degrade with smaller transitor lengths. From TCAD insights, they proposed the following model for R_{SD}:

$$R_{SD} = R_0 + \frac{\sigma}{W(V_{ov} + dV_{th})}. \tag{4.4}$$

Where σ is an experimentally determined coefficient. The constant term R_0 represents the bias-independent contact and silicide resistances. Interestingly, the second term is seen to be associated to the local inversion beneath the spacer, in the underlaps regions. These underlaps thus behave as parasitic access transistors, driven by a local threshold voltage $V_{th,u} = V_{th,c} - dV_{th}$, where $V_{th,c}$ is the intrinsic transistor threshold voltage and $dV_{th} > 0$ (this makes physical sense seen the higher doping in the underlap regions).

Introducing Eq. (4.4) (with $dV_{th} = 0$) into Eq. (3.12), it was shown that Fleury's $1/\beta$ method is unable to correctly extract the R_{SD} variation with V_G. This bias dependence was then seen to generate an erroneous collapse with the gate length of the low-field mobility μ_0 extracted from the Y-function method.
The total resistance method was shown able to extract the $R_{SD}(V_G)$ variation correctly, and successfully applied to 28 nm FDSOI transistors measurements [10]. This thus further motivates its use in this work.

Those elements were confirmed by Henry et al. in [11]. The total resistance method was shown applicable to 28 nm and 14 nm FDSOI transistors, and it was further affirmed that the variation of access resistance with V_G is a major parameter degrading the apparent mobility in short transistors. Correcting for it, both articles obtained a length-independent low-field mobility μ_0, rather than the usual degradation with shorter gate lengths.
One notes that the UTSOI compact model offers a parameter ("RSG") to model the R_{SD} dependence with V_G [38], with a similar form as proposed by Henry et al.

From above insigths, it is thus decided here to extract $R_{SD}(V_G)$ using the total resistance method, and to take this bias dependence into account in the split CV $\mu_{eff}(V_G)$ extraction. To the author's knowledge, this has up to now been neglected in split CV mobility extractions.

At this point, an important question can be raised on the method's main underlying hypothesis that μ_{eff} doesn't significantly depend on L_{eff} (Hyp.7).
This assumption is usually considered acceptable for a constant and uniform channel doping. For example, [37] mentions a critical transistor length L_{crit} such that for $L_g < L_{crit}$ pocket implants are overlapped, hence giving an uniform channel. In our case, the channel doping cannot be assumed uniform due to the source and drain diffusion profiles extending into the channel. Nevertheless, as was shown in Section 3.5, the linearity of the total resistance $R_m(L_{eff})$ plots is still excellent. With all gate lengths ($L_{mask} = [25,\ 35,\ 45,\ 65,\ 90,\ 150]\ nm$), one extracted $R_{SD} = 248\,\Omega\mu m$, while with only the three smallest lengths ($L_{mask} = [25,\ 35,\ 45]\ nm$) one gets $247\,\Omega\mu m$. This linearity was also observed experimentally for 28 nm FDSOI and for 14 nm FDSOI in the previously discussed papers [10] and [11]. In these, it is then taken as a proof that the intrinsic mobility doesn't depend significantly on the gate length.

In our TCAD simulations, this is probably explained by the high background doping in the channel (see Fig. 2.3), which gives a similar intrinsic channel mobility for all considered transistor lengths. Indeed, the doping in the center of the channel is similar for a $L_{mask} = 25\,nm$ and a $L_{mask} = 150\,nm$ transistor (see Fig. 2.3), while the mobility drop due to the highly doped source and drain diffusions is accounted for through R_{SD}.

4.2.2 Bias dependent R_{SD} extraction

Figure 4.6 shows the extraction of $R_{SD}(V_{GS})$ from the total resistance R_m versus L_{eff} plots for $0.6\,V < V_{GS} < 1.2\,V$. The linearity of the curves is excellent for all these voltages in strong inversion.

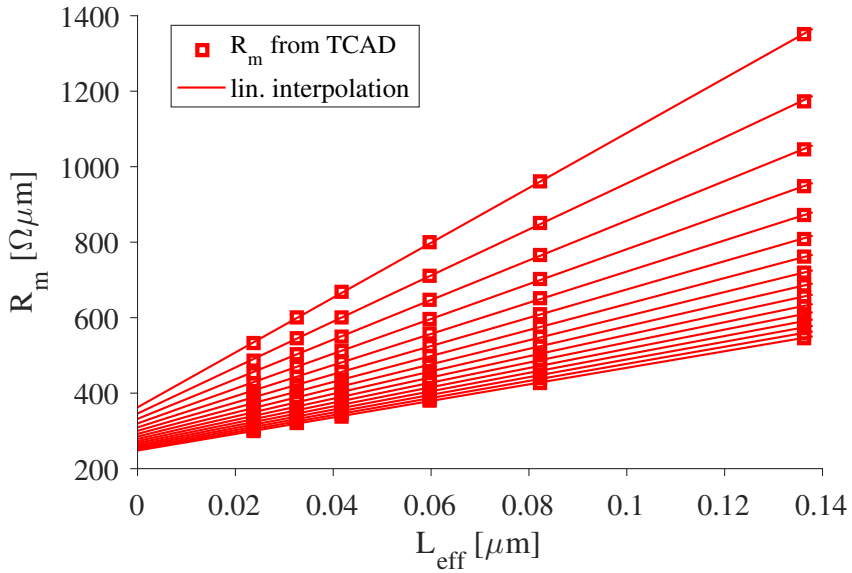

Fig. 4.6: Extraction of R_{sd} from the total resistance R_m versus L_{eff} plots for $V_{GS} = 0.6V$ (higher curves) to $V_{GS} = 1.2\,V$ (lower curves) by $40\,mV$ steps (full mobility model).

Figure 4.7 shows the extracted R_{SD} values, which are valid in strong inversion only. One indeed observes a significant decrease with V_G in agreement with Eq. (4.4), due to the parasitic access transistors getting more conductive (decrease of 44% between $R_{SD}(V_{GS}) = 0.6\,V$ and $R_{SD}(V_{GS}) = 1.2\,V$). These results are very similar to those experimentally obtained by Henry et al. [11].

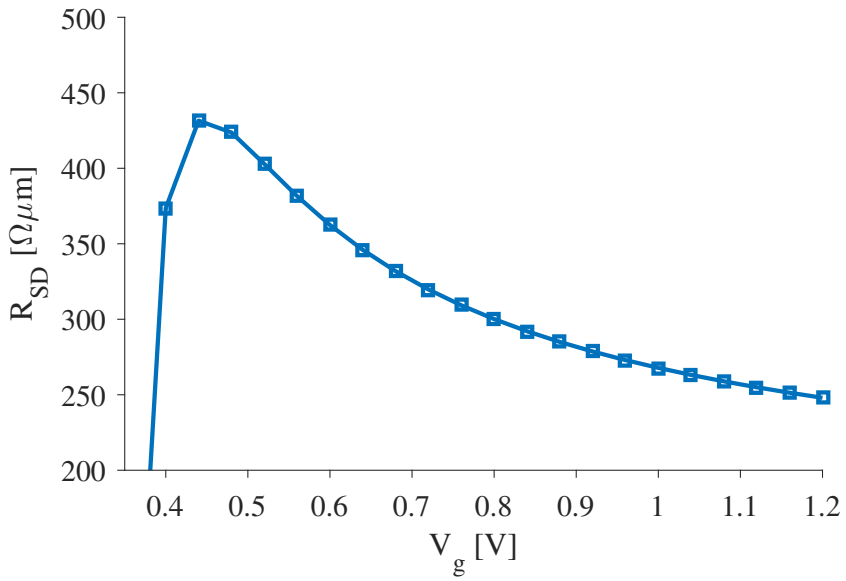

Fig. 4.7: R_{sd} bias dependance extracted from the total resistance method (full mobility model). The extracted value are only valid in strong inversion, and the peak around threshold can thus not be considered physical.

4.2.3 Impact on mobility results

Figures 4.8 and 4.9 compare the extracted mobility with and without considering the R_{SD} bias dependence.

The impact on the extraction is relatively modest for the simple mobility model (Fig. 4.8). Indeed, the value of the access resistance $R_{SD} \approx 141\,\Omega\mu m$ is unphysically low as doping dependence isn't

properly accounted for. The impact on the $L_{mask} = 150\,nm$ transistor is then practically negligible. It is more important for $L_{mask} = 25\,nm$ where correcting for the R_{SD} bias dependence results in a better behaved curve, which however still clearly underestimates the mobility implemented in TCAD.

The method is seen to have a major influence on the extracted mobility for the full mobility model (Fig. 4.9). The high doping of the source and drain diffusions compared to the channel makes the effect of R_{SD} important, particularly for $L_{mask} = 25\,nm$ (see sections 3.5 and 3.6). Accounting for its dependence on V_G (Fig. 4.7) has a particularly significant impact for the short ($L_{mask} = 25\,nm$) transistor. The unphysical, monotonically increasing mobility behaviour is indeed seen to be corrected. For both transistor lengths, one then obtains a mobility evolution with V_G in better agreement with μ_{vol}.
The value of the extracted mobility μ_{ext} is seen to be higher than this μ_{vol}. As mentioned in Section 4.2.1, this can be attributed to the doping of the source and drain diffusions which lowers μ_{vol}, while their influence on μ_{ext} is precisely corrected for through R_{SD}.

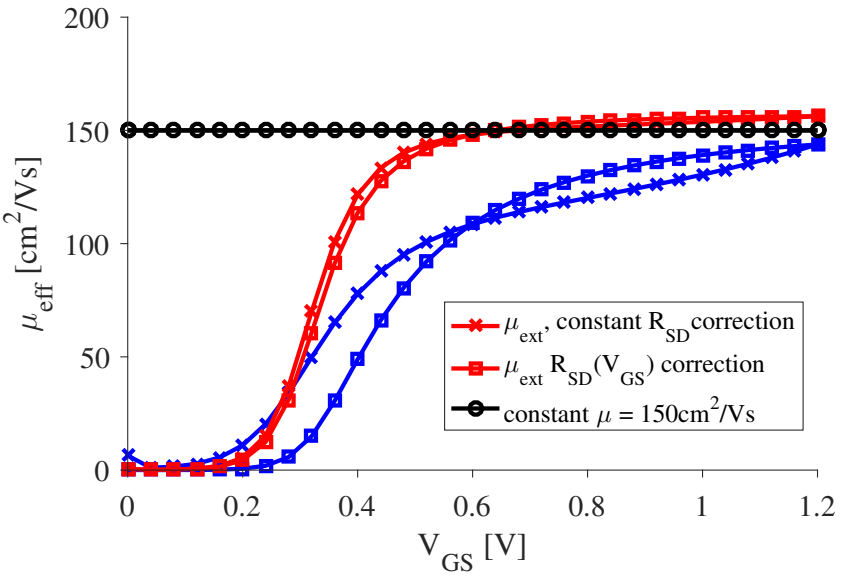

Fig. 4.8: Mobility extracted from the simple TCAD mobility model when correcting for R_{SD} bias dependence (squares), compared to that with constant R_{SD} (crosses) and $\mu = 150 cm^2/Vs$ implemented in TCAD (black circles). Blue curves indicate $L_{mask} = 25\,nm$, red curves $L_{mask} = 150\,nm$.

4.3 Summary and conclusion

This chapter started with the comparison of different R_{SD} extraction methods. The simple total resistance method was shown suitable for our purpose. Firstly, the linearity of the total resistance R_m with respect to L_{eff} was seen to be excellent, confirming (Hyp.7) in our TCAD simulations. This was attributed to the high channel background doping, resulting in similar intrinsic channel mobility for all considered transistor lengths. Secondly, this method enabled to extract the significant dependence of R_{SD} on V_G with similar results as reported in literature, supporting the analysis that the underlaps behave as parasitic access transistors.

This R_{SD} bias dependence was shown to have a major impact on the mobility values extracted in short transistors and their evolution with V_G. This thus indicates that (Hyp.8) is unsuited in short FDSOI transistors. Accounting for this bias dependence enabled to retrieve a mobility evolution in better agreement with μ_{vol}. This is considered an important result of this work.
While the influence of the R_{SD} bias dependence on the low-field mobility μ_0 extracted with the

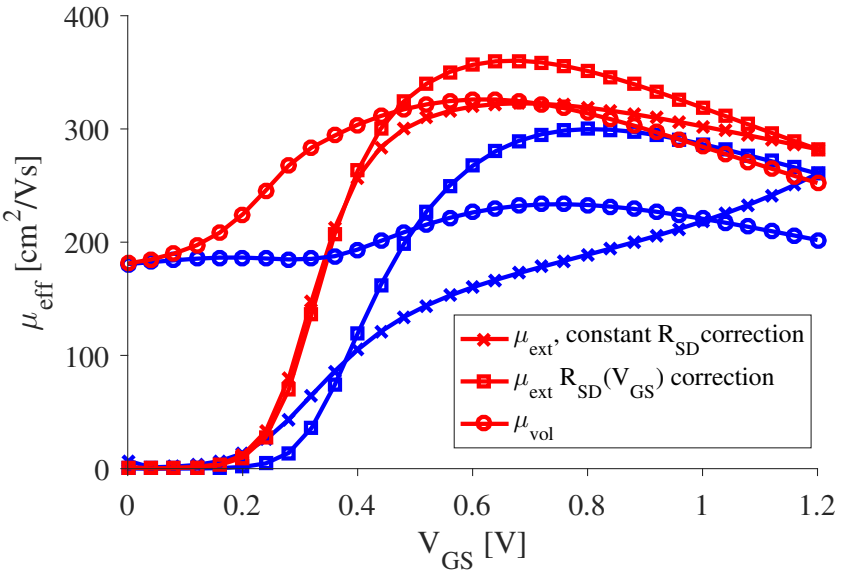

Fig. 4.9: Mobility extracted from the full TCAD mobility model when correcting for R_{SD} bias dependence (squares), compared to that with constant R_{SD} (crosses) and μ_{vol} from TCAD (circles). Blue curves indicate $L_{mask} = 25\,nm$, red curves $L_{mask} = 150\,nm$.

Y function has been discussed in literature, it has to the author's knowledge up to now not been accounted for in $\mu_{eff}(V_G)$ split CV extractions.

The mobility is however still seen to be underestimated in short transistors after this correction, as notably indicated by the results on the simple mobility model. In the next chapters, this will be attributed to the parasitic contribution of the inner fringing capacitance to the intrinsic charge extraction.

5 Gate capacitance contributions

In the previous chapter, one showed the importance of the R_{SD} bias dependence to extract a correct mobility behaviour in short transistors. However, the mobility was still seen to be underestimated in these short devices.
In this chapter, it is thus proposed study the parasitic contributions to the gate capacitance more deeply. Their impact on the mobility extraction will then be presented in Chapter 6, indicating the inner fringing capacitance as the source of this remaining underestimation.

The parasitic gate capacitances usually considered for advanced nodes were shown in Chapter 3. One expressed the total gate capacitance C_{gg} as

$$C_{gg} = C_{ggi}(V_{GS}, L_{eff}) + C_{gge,ov} + C_{gge,of}(L_{eff}) + C_{gge,if}(V_{ov}) \tag{5.1}$$

with the different parasitic contributions recalled in Fig. 5.1 below.

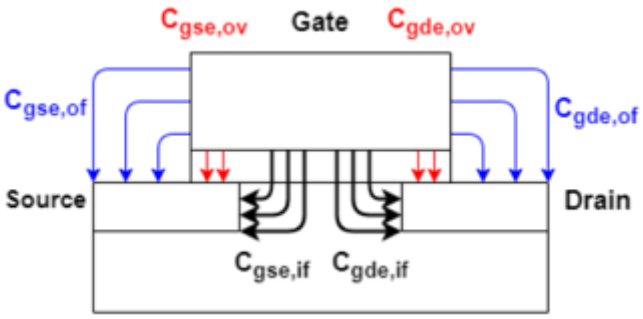

Fig. 5.1: Parasitic gate capacitances as modeled in [20]. Image taken from [23]

One attempted to extract the intrinsic gate capacitance C_{ggi} from the total gate capacitance C_{gg} as classically done by defining $C_{gg,norm}$ (Eq. (3.8))

$$\begin{aligned} C_{gg,norm} &= C_{gg}(V_{GS}, L_{eff}) - C_{gg}(V_{GS} = V_{GS,min}, L_{eff}) \\ &\approx C_{ggi}(V_{GS}, L_{eff}) + C_{gge,if}(V_{GS}) \end{aligned}$$

with $V_{GS,min}$ placing the transistor in accumulation. This expression of $C_{gg,norm}$ relies on the assumptions recalled below:

- (Hyp.1) The outer fringing and overlap capacitances $C_{gge,of}$ and $C_{gge,ov}$ are considered independent of V_{ov}

- (Hyp.2) The inner fringing capacitance $C_{gge,if}$ is taken independent of the length
- (Hyp.3) The inner fringing capacitance $C_{gge,if}$ is assumed shielded in accumulation regime (at $V_{GS} = V_{GS,min}$)
- (Hyp.4) The threshold voltage variation with L_{eff} is assumed low enough for the extraction to be performed at the same V_{GS} for all transistors.

$C_{gg,norm}$ was then used as an estimate of C_{ggi} for both Q_i and L_{eff} extraction, although is known to be perturbed by the inner fringing capacitance. The following hypotheses were thus made for Q_i extraction, performed by integration of $C_{gg,norm}$ with starting voltage V^*_{GS}:

- (Hyp.5) $Q_i(V_{GS} = V^*_{GS})$ is negligible
- (Hyp.6) $C_{gge,if}$ is small with respect to C_{ggi} for $V_{GS} > V^*_{GS}$

In this chapter, one will assess the different assumptions related to the inner fringing capacitance $C_{gge,if}$. (Hyp.3) will be confirmed to be invalid in FDSOI transistors as the absence of dynamic hole response in accumulation prevents shielding of $C_{gge,if}$.

An alternative C_{ggi} extraction method proposed by Vandermolen et al. will then be validated and shown useful to gain insight on the different contributions to the total gate capacitance. It will then be shown how the inner fringing capacitance behaviour can be partly related to modulation of charges in the underlaps, hinting at the link with the parasitic access transitor concept discussed in Section 4.2.1.

5.1 $C_{gge,if}$ bias dependence

5.1.1 $C_{gge,if}$ modeling in FDSOI

A first model for the inner fringing capacitance in bulk MOSFET's was proposed in [39]. The capacitance was computed from a geometrical double plate model using a suitable transformation. Its bias dependence was completely neglected in this analysis.

Prégaldigny et al. adapted this model for advanced bulk nodes and added the bias dependence explicitly, taking into account shielding by free carriers in inversion or accumulation regimes [40]. This model has then been widely considered in split CV extractions both in bulk and, questionably, FDSOI transistors [20, 21, 41, 42] .

Kim et al. [43] proposed bias-independent geometry-based expressions for fringing capacitances in ultra-thin body SOI structures with underlaps, also introducing length-dependent fringing through the bulk. The relation with the underlap doping profiles and effective length was then studied by Agrawal et al. [44]. However, the inner fringing behaviour in accumulation regime wasn't clarified.

A charge-based modeling of the inner fringing capacitance in SOI MOSFET's was reported by Wiatr et al. in [45]. The inner fringing capcacitance was considered shielded only in inversion regime. This unshielded inner fringing behaviour in FDSOI has also been reported in [46, 47].
Indeed, it is well known that, contrary to what happens in bulk devices, no dynamic hole response occurs in accumulated FDSOI transistors. This can be readily appreciated from the $C_{gg} - V_{GS}$ plots as in Fig. 3.2.
In a bulk NMOS transistor, the gate capacitance almost reaches the equivalent gate oxide capacitance C_{ox} in accumulation regime as holes are the majority carriers in the P-doped channel. They can be moved from/to the bulk, and thus respond easily to gate voltage changes. In the case of an N-type FDSOI transistor, the source and drain regions are highly N-doped and the channel left undoped.

Furthermore, the channel is separated from the body by the buried oxide. There is thus no "reservoir" holes can be generated from. As a result, they are unable to follow the gate voltage at practical frequencies, and the inner fringing capacitance is can then not be shielded dynamically [46].

A physical inner fringing capacitance model, based on the computation of the associated inner fringing charges, has recently been introduced in the UTSOI2.2 compact model for improved description of C_{gg} in short transistors [38].

5.1.2 Rewriting $C_{gg,norm}$

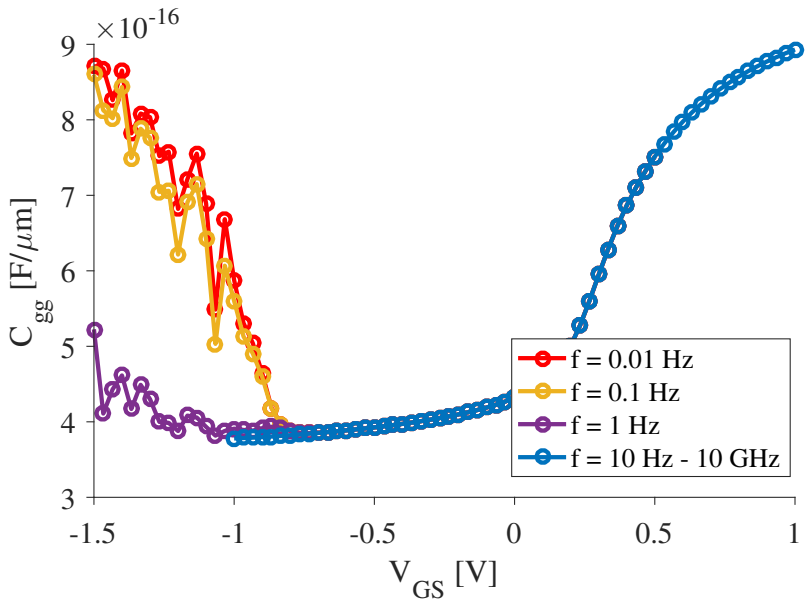

Fig. 5.2: TCAD $C_{gg}(V_{GS})$ curves for frequencies $f = 10^{-2}\,Hz$ to $f = 10^{10}\,Hz$, one frequency per decade.

The absence of hole response at usual frequencies is assessed by TCAD simulation in Fig. 5.2. No dynamic hole response is observed and the curves are superimposed for all $f > 10\,Hz$. The onset of a hole response around $V_{GS} = -0.8\,V$ is visible below $f = 1\,Hz$, well under our extraction frequency of $f = 100\,kHz$.

Note that generation-recombination or tunneling models were not studied in more detail, hence the TCAD simulation used here might lack accuracy when those phenonomena dominate. Figure 5.2 should thus be seen as a confirmation that hole response might only occur at frequencies several orders of magnitude below our extraction frequency of $f = 100\,kHz$, rather than as a precise determination of this dynamic hole response cutoff frequency.

(Hyp.3), which was valid for bulk transistors, is thus not acceptable anymore in FDSOI. For the latter, Eq. (3.8) should then be rewritten

$$C_{gg,norm}(V_{GS}, L_{eff}) = C_{gg}(V_{GS}, L_{eff}) - C_{gg}(V_{GS,min}, L_{eff}) \tag{5.2}$$

$$\approx C_{ggi}(V_{GS}, L_{eff}) + C_{gge,if}(V_{GS}) - \mathbf{C_{gge,if}(V_{GS,min})} \tag{5.3}$$

which shows the appearance in $C_{gg,norm}$ of an additional inner fringing term in accumulation.
In the following, an alternative C_{ggi} extraction method will be evaluated and used to discriminate between the different contributions to C_{gg}. It will notably be useful to assess the significance and bias dependence of $C_{gge,if}$.

5.2 Alternative capacitances extraction

In this section, we will apply a gate capacitance modeling method proposed in unpublished work by Vandermolen et al. [34], very similar to an approach mentioned in [11]. Its ability to describe C_{gg} with precision will be confirmed here from the TCAD simulations. The method will be used to discriminate between the different contributions to the total gate capacitance (see Section 3.2) and evaluate their relative importance and dependence with bias.

5.2.1 Normalization to V_{ov}

One starts by extracting the threshold voltage V_{TH} from the maximum of the gate capacitance derivative dC_{gg}/dV_g as was shown in Section 2.4. As mentioned there, V_{TH} should rigorously be extracted from the maximum of dC_{ggi}/dV_g. The intrinsic gate capctiance C_{ggi} is however not available at this stage of the method, as its extraction will precisely rely on normalization of C_{gg} to the overdrive voltage V_{ov}. Nevertheless, in [34] using the total gate capacitance was verified *a posteriori* to give very similar results. This was also verified in our case (see figures A.1 and A.2 in appendix)

The capacitance curves are then normalized to $V_{ov} = V_{GS} - V_{TH}$ and spline interpolated (500 points) from $V_{ov,min} = (V_{GS,min} - V_{TH,mean})$ to $V_{ov,max} = (V_{GS,max} - V_{TH,mean})$, with $V_{GS,min} = -1.2\,V$, $V_{GS,max} = 1.2\,V$ and $V_{TH,mean} = 0.332\,V$ the average threshold voltage computed from Table 2.1. The curves are thus weakly impacted at their extremities. Those with corresponding V_{TH} greater (resp. smaller) than $V_{TH,mean}$ are extrapolated near $V_{GS,min}$ (resp. $V_{GS,max}$) and truncated near $V_{GS,max}$ (resp. $V_{GS,min}$).

With this method, (Hyp.4) is then eliminated from the C_{ggi} extraction (however not totally, as linear interpolation of C_{gg} will be performed against L_{eff}, whose extraction still relies on (Hyp.4)). .

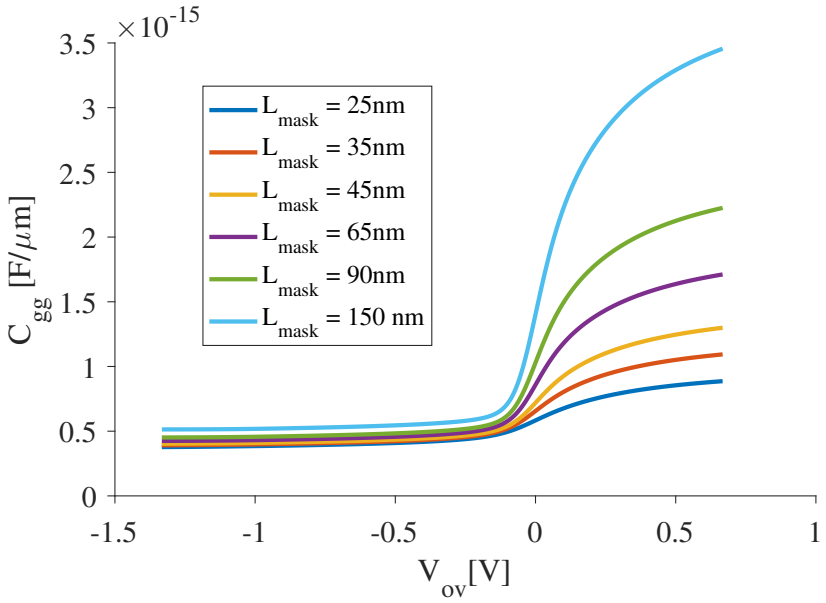

Fig. 5.3: $C_{gg}(V_{ov})$ curves from TCAD, with V_{TH} extracted at the maximum of the gate capacitance derivative.

5.2.2 Linear interpolation of C_{gg}

A plot of C_{gg} against L_{eff} (as extracted in Section 3.4) for $V_{ov,min} < V_{ov} < V_{ov,max}$ is shown on Fig. 5.4.

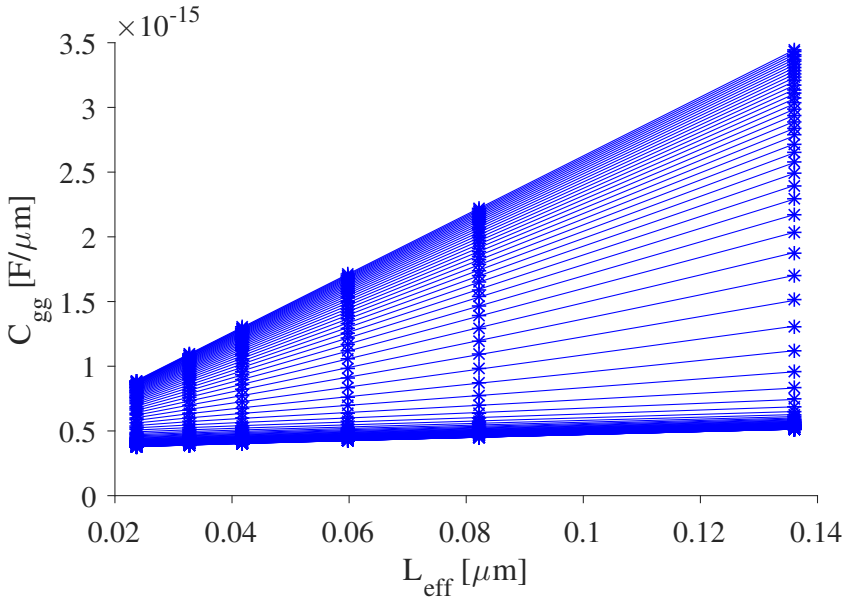

Fig. 5.4: Total gate capcitance C_{gg} plotted against L_{eff} for V_{ov} from $V_{ov,min}$ to $V_{ov,max}$ by steps of $20\,mV$

These curves suggest a linear relation between C_{gg} and L_{eff}. Here, a difference is made with [34] where the gate length L_g is used. Using the effective length L_{eff} instead is deemed more physical for the extraction of C_{ggi} presented below.

From the observation of Fig. 5.4, Vandermolen et al. proposed to assume [34]

$$C_{gg}(V_{ov}, L_{eff}) \approx A(V_{ov})L_{eff} + B(V_{ov}) \tag{5.4}$$

with

$$A(V_{ov}) = A_1(V_{ov}) + A_2 \tag{5.5}$$
$$B(V_{ov}) = B_1(V_{ov}) + B_2 \tag{5.6}$$

A linear interpolation of the total gate capcitance C_{gg} against L_{eff} can then be performed to extract the coefficients A and B. The results are shown in Fig. 5.5.
The extracted $B(V_{ov})$ coefficient corresponds to a usual parasitic capacitances plot obtained in a similar manner (against L_g) in [11, 41, 42]. One remarks the peak around $V_{GS} = 0.2\,V$, attributed to the maximal contribution of inner fringing in depletion (see Section 5.1).

Only [11] also reports the evolution of $A(V_{ov})$, which unsurprisingly corresponds to an intrinsic capacitance behaviour (plus a constant term). To the author's knowledge, it hasn't been used for split CV extraction except in [34], even though doing so can be seen as a generalization of the method proposed by Romanjek et al. [20].

As proposed in [34], the terms A_1, A_2, B_1 and B_2 in equations 5.5 and 5.6 can be associated to the different contributions to the total gate capacitance C_{gg} recalled below:

$$C_{gg} = C_{ggi}(V_{GS}, L_{eff}) + C_{gge,ov} + C_{gge,of}(L_{eff}) + C_{gge,if}(V_{ov})$$

Note the A and B coefficients are average results obtained by linear regression of the gate capacitance against all the different lengths, thus not including possible variations between different geometries. This is underlined by the "mean" notation of their symbols.

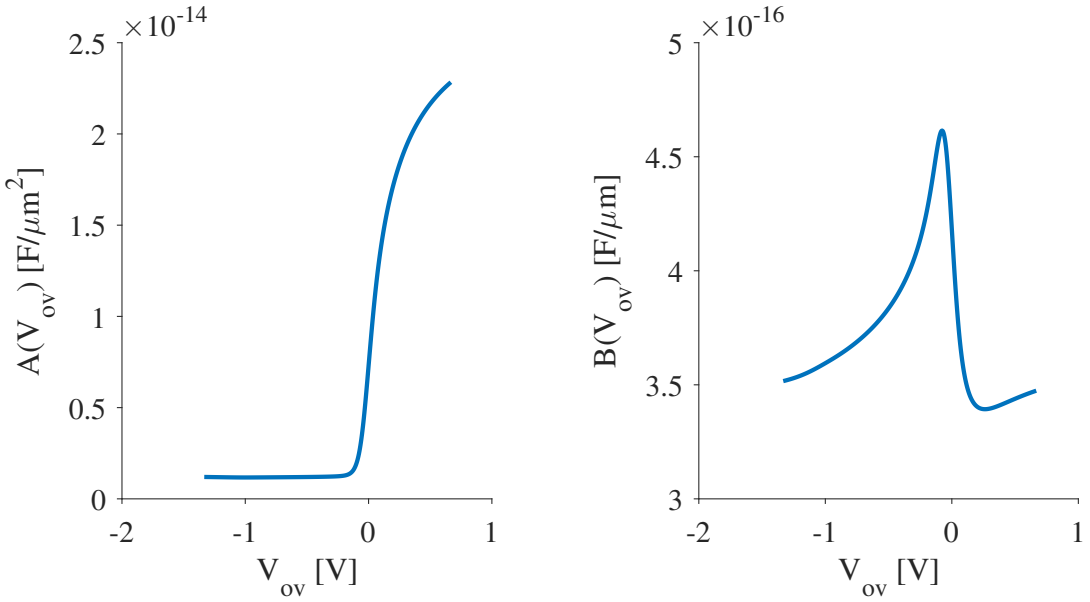

Fig. 5.5: Linear interpolation coefficients A and B in function of V_{ov} extracted from Fig. 5.4

- The intrinsic capacitance C_{ggi} depends on V_{ov} and scales linearly with L_{eff}. Thus $A_1(V_{ov})$ is associated to the mean intrinsic gate capacitance per unit length $\overline{C'_{ggi}}$

- The outer fringing capacitance $C_{gge,of}$ is known to depend on the gate length (and thus L_{eff} as $L_{eff} = L_g - \Delta L$ with ΔL constant for all L_g) [48]. One thus attributes A_2 to $\overline{C'_{gge,of}}$ (average outer fringing capacitance per unit length)

- The inner fringing capacitance is assumed independent of the length in this method (Hyp.2). As it varies with bias, $B_1(V_{ov})$ then models $\overline{C_{gge,if}}$

- The overlap capacitance C_{ov} is independent of the length and not impacted by V_{ov} (Hyp.1). The mean overlap capacitance $\overline{C_{ov}}$ is thus modeled by the B_2 term.

5.2.3 Evaluation of the method

Figure 5.6 and 5.7 evaluate the ability of Eq. (5.4) to reconstruct the inital total gate capacacitance C_{gg} from the interpolated terms for $L_{mask} = 150\,nm$ and $L_{mask} = 25\,nm$ (results for all lengths are found in Appendix A.1, figures A.9 - A.4). The method is confirmed to model C_{gg} accurately for both long and short channel transitors, thus validating the approach (see Fig. A.10: less than 2.5% relative error for all gate lengths on the entire voltage range).
One remarks the significant contribution of parasitics to the total gate capacitance in the $L_{mask} = 25\,nm$ transistor (Fig. 5.7).

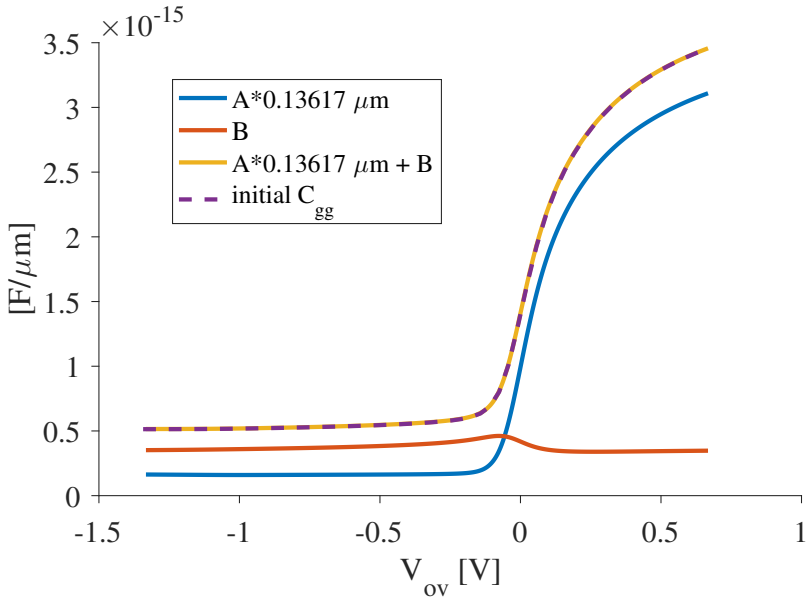

Fig. 5.6: Modeling of the gate capacitance C_{gg} by the linear interpolation method. The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 150\,nm$, $L_{eff} = 136.2\,nm$

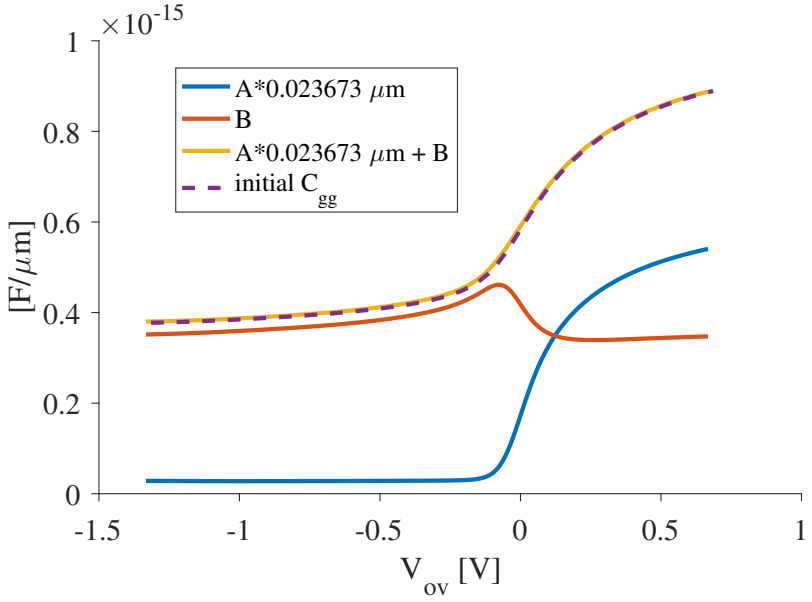

Fig. 5.7: Modeling of the gate capacitance C_{gg} by the linear interpolation method. The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 25\,nm$, $L_{eff} = 23.7\,nm$

The $A_1(V_{ov})$ term is associated to $\overline{C'_{ggi}}$, thus one can now estimate the intrinsic gate capacitance C_{ggi} by $\overline{C_{ggi}} = A_1(V_{ov})L_{eff}$. The result is compared with $C_{gg,norm}$ used in the conventional split CV method in Fig. 5.8.

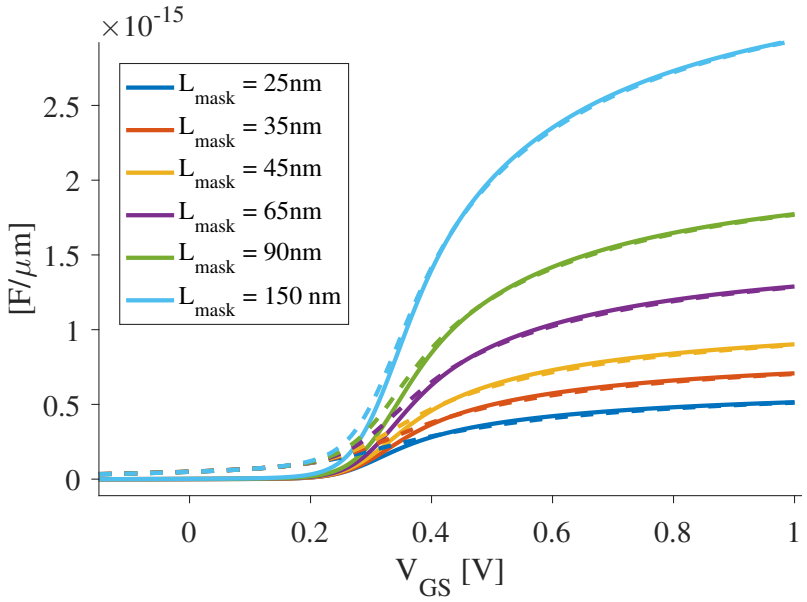

Fig. 5.8: Comparison between $A_1(V_{GS})L_{eff}$ (full) and $C_{gg,norm}(V_{GS}, L_{eff})$ (dashed) as estimates of C_{ggi}

The "elbow" around threshold in the $C_{gg,norm}$ curves is attributed to the inner fringing contribution and seen to be corrected by $\overline{C_{ggi}} = A_1(V_{GS})L_{eff}$ (see also Fig. 5.9). This linear interpolation method is thus seen promising for Q_i extraction, as was proposed by Vandermolen et al. and will be confirmed in the next chapter.

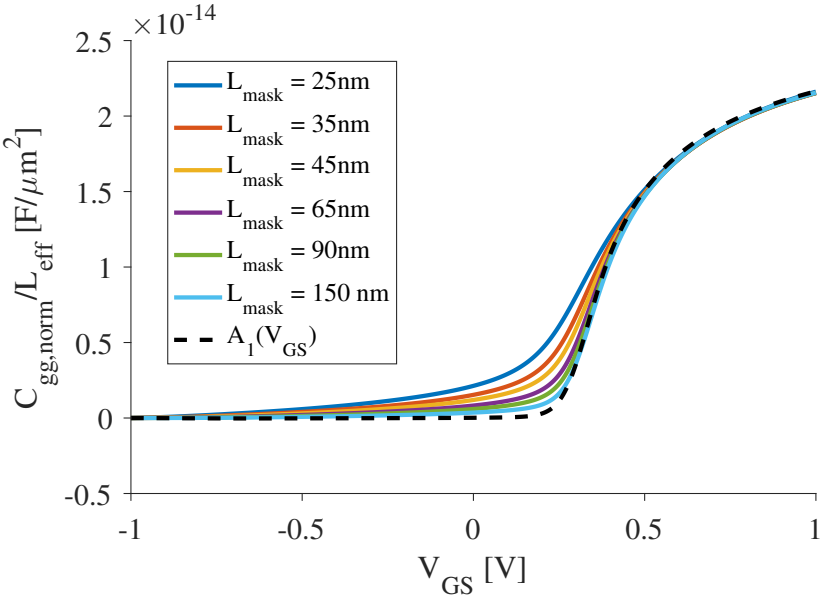

Fig. 5.9: Comparison between $A_1(V_{GS})$ (dashed black line) and $C_{gg,norm}/L_{eff}$ (colors) as estimates of C'_{ggi}. The influence of the inner fringing is particularly visible in the shorter transistors as $C_{gge,if}$ is larger compared to C_{ggi}.

Going one step further, one can compare Eq. (5.3):

$$\begin{aligned} C_{gg,norm}(V_{GS}, L_{eff}) &= C_{gg}(V_{GS}, L_{eff}) - C_{gg}(V_{GS,min}, L_{eff}) \\ &\approx C_{ggi}(V_{GS}, L_{eff}) + C_{gge,if}(V_{GS}) - C_{gge,if}(V_{GS,min}) \end{aligned}$$

against

$$\overline{C_{gg,norm}}(V_{GS}, L_{eff}) = A_1(V_{GS})L_{eff} + B_1(V_{GS}) - B_1(V_{GS,min}) \tag{5.7}$$

$$\approx \overline{C'_{ggi}(V_{GS})}L_{eff} + \overline{C_{gge,if}(V_{GS})} - \overline{C_{gge,if}(V_{GS,min})} \tag{5.8}$$

As shown in Fig. 5.10. $C_{gg,norm}$ is well modeled by Eq. (5.8), including both intrinsic and inner fringing contributions. It thus overestimates C_{ggi} in weak inversion due to the maximum contribution of $C_{gge,if}$ in this region, while it slightly underestimates it in strong inversion due to the $C_{gge,if}(= V_{GS,min})$ term [34].

This thus confirms the interest of the linear interpolation method to extract the behaviour of the different gate capacitances. Its insights will be leveraged in the next chapter to assess the impact of the inner fringing capacitance on the mobility extraction.

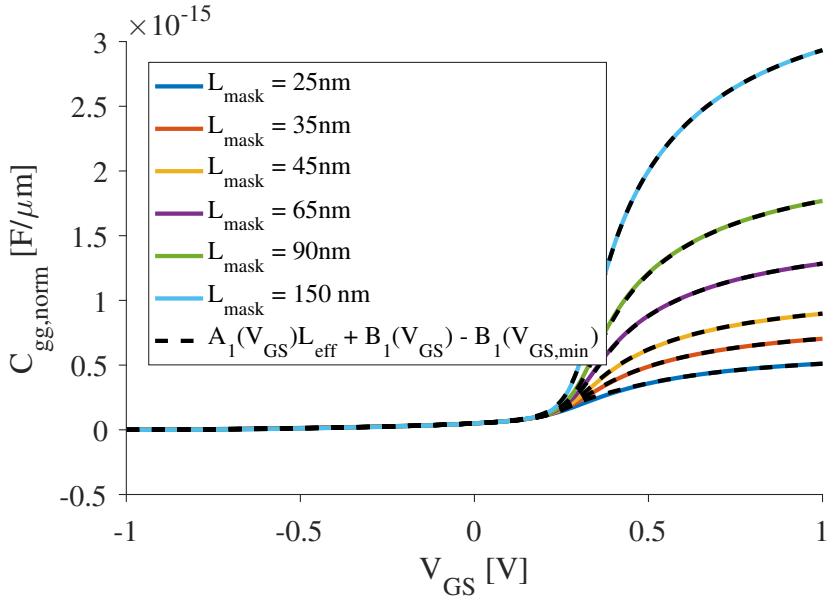

Fig. 5.10: Comparison between $C_{gg,norm}$ from Eq. (3.6) (full) and $\overline{C_{gg,norm}}$ from Eq. (5.8) (dashed) for different transitor lengths.

5.3 Link to underlap charge modulation

The behaviour of the inner fringing capacitance was studied in the previous section using the C_{gg} linear interpolation method proposed by Vandermolen et al. Here, we will show how part of this behaviour can be retrieved from the modulation of charges in the underlaps of the transistor.

Figure 5.11 and 5.12 show the evolution of the potential and electron density along a cut through the channel and the underlaps of a $L_{mask} = 25\,nm$ transistor. The effective length L_{eff} is indicated by the red dashed lines. Both quantities are seen to be modulated by the gate voltage much beyond the effective length, i.e in the underlaps.

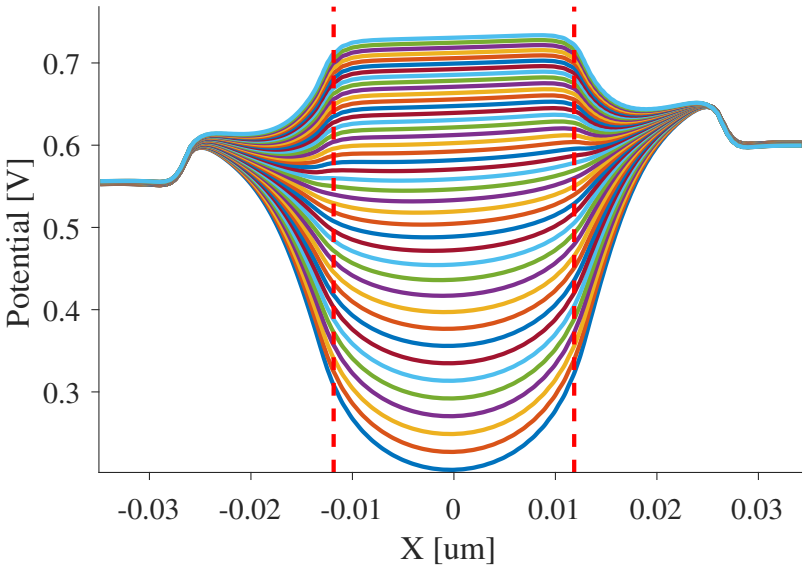

Fig. 5.11: TCAD simulated potential cut along the channel $0.1\,nm$ below the gate oxide for a $L_{mask} = 25\,nm$ transistor. V_{GS} goes from $0\,V$ (lowest curve) to $1\,V$ (highest curve) by $25\,mV$ steps. The dashed red lines delimitate L_{eff}.

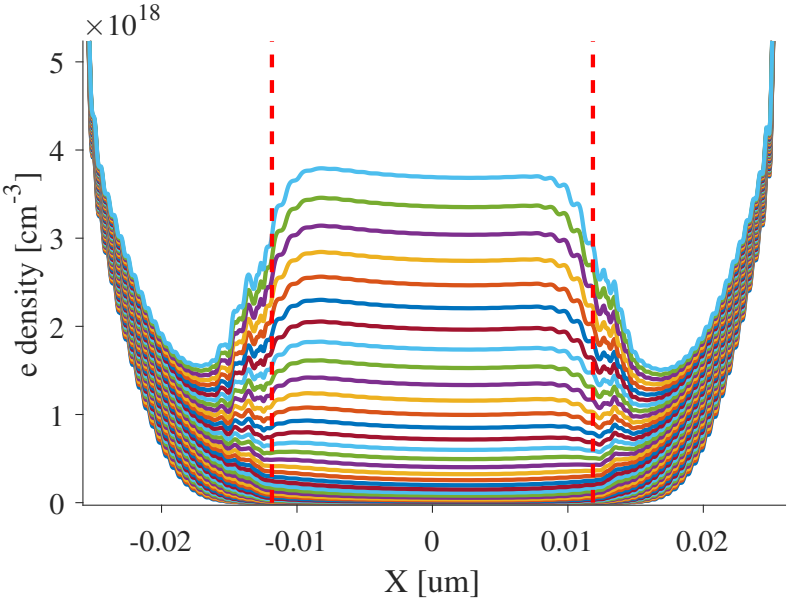

Fig. 5.12: TCAD simulated electron density along the channel $0.1\ nm$ below the gate oxide for a $L_{mask} = 25\,nm$ transistor. V_{GS} goes from $0V$ (lowest curve) to $1\,V$ (highest curve) by $25\,mV$ steps. The dashed red lines delimitate L_{eff}.

The modulation of charges by the gate voltage shown in Fig. 5.12 is naturally linked to the gate capacitance behaviour. It is thus proposed to study the equivalent capacitances associated to the total charge variation with V_G in both channel and underlap regions. To do so, the total charge density $\rho(x, y, V_G)$ is integrated over 1) the channel region ($X = [-L_{eff}/2, L_{eff}/2]$, $Y = [0, t_{Si} = 6.7\,nm]$) and 2) the underlaps and source/drain diffusion regions (see Fig. 2.2). One thus has

$$Q_c(V_G) = \iint_{channel} \rho(x, y, V_G)dxdy \tag{5.9}$$

$$Q_u(V_G) = \iint_{underlaps+S/D} \rho(x, y, V_G)dxdy \tag{5.10}$$

and computes the associated equivalent capacitances $\frac{dQ_c(V_G)}{dV_G}$ and $\frac{dQ_u(V_G)}{dV_G}$. Their behaviour is shown in Fig. 5.13a and compared with the coefficients extracted from the linear interpolation technique (Fig. 5.13b).

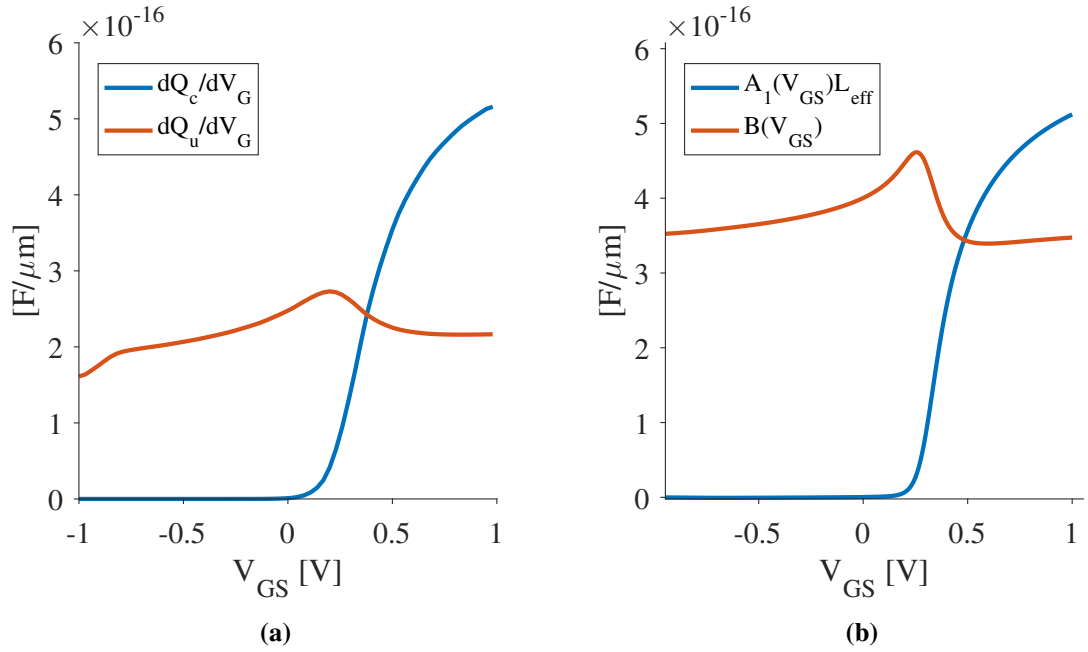

Fig. 5.13: **(a)** Channel and underlap capacitances extracted from the TCAD simulated charge variation with V_G **(b)** $A_1(V_{GS})$ and BV_{GS} coefficients from the linear interpolation method, $L_{mask} = 25\,nm$.

The channel charge variation $\frac{dQ_c}{dV_g}$ shows the expected intrinsic capacitance behaviour, in agreement with $\overline{C_{ggi}}$. The charge variation in the underlaps is shown to reproduce the inner fringing behaviour, with the characteristic peak in the depletion regime. Part of this inner fringing behaviour can thus be linked to the modulation of charges by the gate voltage in the underlapped regions.

5.4 Summary and conclusion

This chapter studied the parasitic gate contributions in more detail. The different hypotheses underlying the expression of $C_{gg,norm}$ were recalled. (Hyp.3), the assumption that $C_{gge,if}$ is shielded in accumulation, was seen to be invalid in FDSOI transistors due to the absence of dynamic hole response. $C_{gg,norm}$ was then rewritten taking into account an inner fringing term in accumulation.
An alternative capacitance extraction method proposed by Vandermolen et al. was confirmed able to describe C_{gg} with precision, and shown useful to extract the behaviour of its different terms. Using its insights, it was then seen that the inner fringing behaviour is partly retrieved from the modulation of the underlap charge by the gate voltage.

In the next chapter, one will discuss the impact of this inner fringing capacitance on L_{eff}, Q_i and mobility extraction. Its contribution to the extracted charge will be identified as the source of the remaining mobility underestimation in short transistors after $R_{SD}(V_{GS})$ correction.

6 Impact and correction of the inner fringing capacitance

In the previous chapters, several assumptions underlying the conventional split CV mobility extraction were discussed and critically assessed for FDSOI transistors. The bias dependence of R_{SD} was confirmed to be a major effect impacting mobility extraction in short devices (see (Hyp.8)). Furthermore, in FDSOI the inner fringing capacitance was seen not to be shielded in accumulation (see (Hyp.3)). An alternative capacitance extraction method was shown useful to evidence the contribution of $C_{gge,if}$ to $C_{gg,norm}$ and provide a preciser extraction of C_{ggi}.

In this chapter, one will study the impact of the inner fringing capacitance on the split CV mobility extraction.
A first step will be to normalize I-V and C-V curves to $V_{ov} = V_{GS} - V_{TH}$ before the extraction. The method then fully accounts for V_{TH} variation with the gate length, and the influence of (Hyp.4) on R_{SD} and L_{eff} extraction is thus removed.
After this correction, one will firstly assess the impact of the inner fringing on L_{eff} estimation. The extraction will be seen perturbed by the inner fringing capacitance term at $V_{GS,min}$. Nevertheless, L_{eff} will be considered correctly extracted in our case.
The contribution of the inner fringing capacitance to the extracted charge will then be discussed, and shown significant in short transistors. Using C_{ggi} as obtained from the alternative capacitance extraction method will be seen to correct for this contribution. Mobility extraction results in good agreement with the TCAD implemented mobility will then be obtained. This indicates that the inner fringing capacitance, through the parasitic charge it generates, can be identified as the major source of mobility underestimation by the split CV method in short transistors (after V_{ov} normalization and $R_{SD}(V_{GS})$ correction).

6.1 Normalizing the extraction to V_{ov}

Different methods to extract the threshold voltage V_{TH} were presented in Section 2.4. The maximum of the gate capacitance derivative was selected as the best suited method, and used in the previous chapter to normalize C_{gg} to $V_{ov} = V_{GS} - V_{TH}$ before extraction of the different capacitance contributions.
However, R_{SD} and L_{eff} were extracted respectively from the total resistance R_m and from $C_{gg,norm}$ with the same V_{GS} for all transistor lengths, thus neglecting V_{TH} variation with L_g (Hyp.4).

Here, both I-V and C-V curves will be normalized to the overdrive voltage before the extraction and spline interpolated from $V_{ov,min} = V_{GS,min} - V_{TH,mean} = -1.53\,V$ to $V_{ov,max} = V_{GS,max} - V_{TH,mean} = 0.87\,V$ (as in Section 5.2.1). This will totally eliminate (Hyp.4) from the estimation of R_{SD} and L_{eff}, and enable to study its impact on the mobility extraction.

6.1.1 Impact on L_{eff} extraction

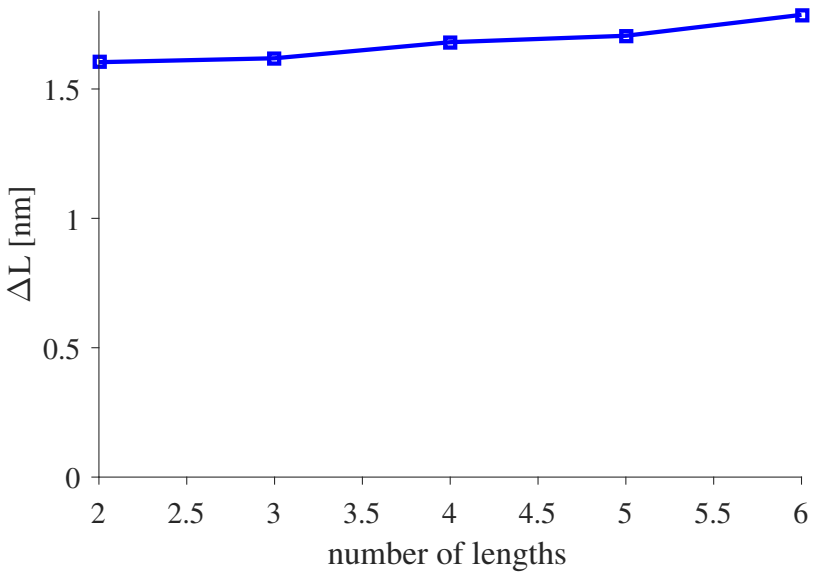

Fig. 6.1: ΔL extracted from linear interpolation against L_g of $C_{gg,norm}(V_{ov,max}, V_{DS} = 0\,V)$ versus the number of lengths used.

Figure 6.1 shows ΔL extracted from $C_{gg,norm}(V_{ov,max}, V_{DS} = 0\,V)$ using an increasing number of lengths, starting from the two smallest in $L_{mask} = [25,\ 35,\ 45,\ 65,\ 90,\ 150]\ nm$ and adding the following ones. Using all lengths, one again obtains $\Delta L = 1.8\,nm$ as in Section 3.4. This is not surprizing as the variation of $C_{gg,norm}$ in strong inversion is small over $\Delta V_{TH} \approx 30\,mV$.
The extracted ΔL variation (11% decrease between ΔL extracted with all lengths and ΔL extracted with the two smallest ones) is reduced compared to that in Fig. 3.5. It thus stays even smaller compared to the considered gate lengths.

6.1.2 Impact on R_{SD} extraction

The linearity of the total resistance $R_m(V_{ov,max})$ against L_{eff} is still excellent. With all gate lengths ($L_{mask} = [25,\ 35,\ 45,\ 65,\ 90,\ 150]\ nm$), one extracts $R_{SD}(V_{ov,max}) = 250\,\Omega\mu m$ (compared to $248\,\Omega\mu m$ without V_{ov} normalization). With only the three smallest lengths ($L_{mask} = [25,\ 35,\ 45]\ nm$), one gets $252\,\Omega\mu m$ (compared to $247\,\Omega\mu m$ without V_{ov} normalization). Again, this is not surprizing for such an extraction at high $V_{GS,max}$ where the ΔV_{TH} variation is small compared to considered overdrive voltages.

Figure 6.2 then shows the extraction of the bias dependent $R_{SD}(V_{ov})$ for $0.3V < V_{ov} < 0.8\,V$.
The linearity of the $R_m(L_{eff})$ curves for these overdrive voltages is assessed in Fig. 6.3. R_{SD} is extracted using a number of lengths N starting from the two smallest ones in $[25,\ 35,\ 45,\ 65,\ 90,\ 150]\ nm$.
The access resistance extracted from the smaller lengths tends to be higher.
One could be interpret this as an indication of lower effective mobility in the shorter devices (see the discussion in Section 4.2.1). The effect is more pronounced than in Fig. 4.6 (without V_{ov} normalization), which one could attribute this to the fact that, without V_{ov} normalization, the mobility degradation with L_g is compensated by a higher V_{ov} (lower V_{TH}) in the expression of the channel resistance (Eq. (3.13)). Nevertheless, the linearity is good when moving to stronger inversion, hence the method is still considered viable for our extraction.

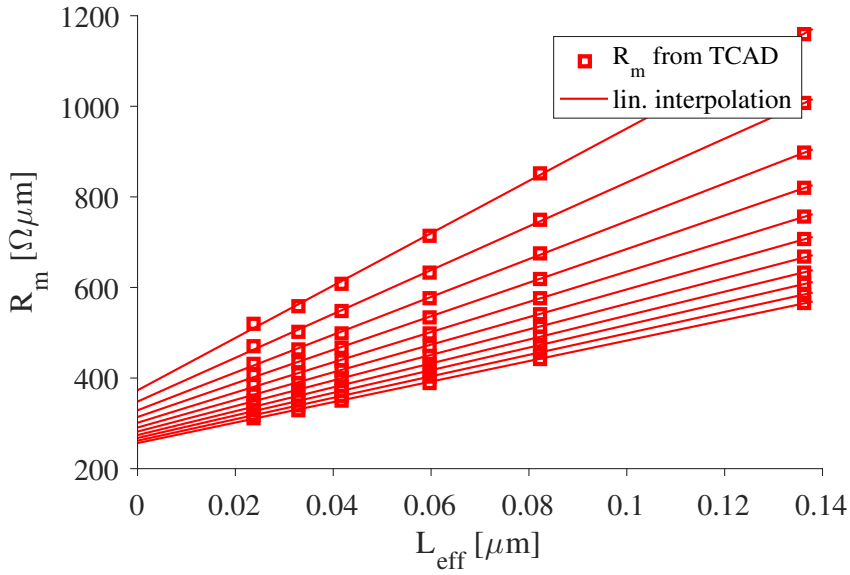

Fig. 6.2: Full mobility model $R_m(L_{eff})$ for V_{ov} from $0.3\,V$ (higher curves) to $0.8\,\mathrm{V}$ (lower curves) by $50mV$ steps

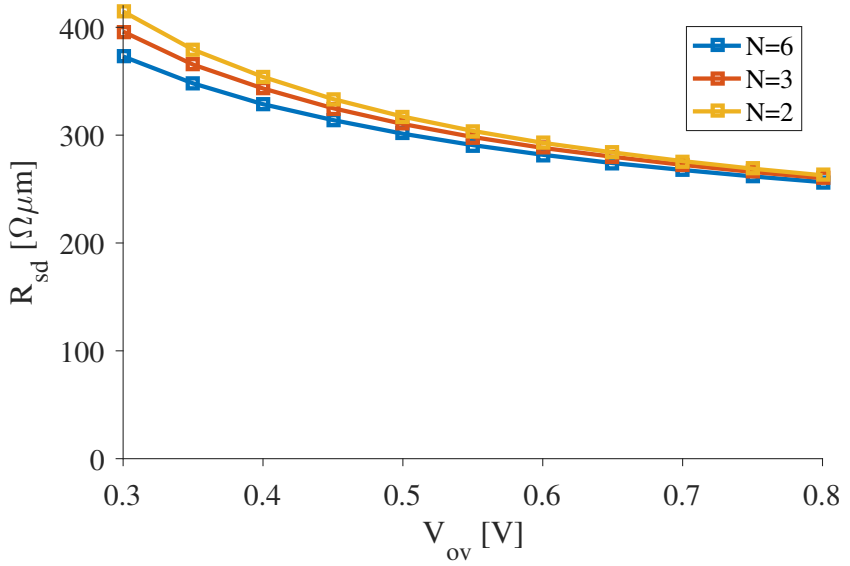

Fig. 6.3: Full mobility model $R_{sd}(V_{ov})$ for different number of lengths used in the linear interpolation of R_m

Figure 6.4 shows the bias dependence of the access resistance extracted with and without normalization to V_{ov}. When V_{ov} reduces, the impact of the normalization is increased and one extracts higher R_{SD} values.
From $V_{ov} = 0.3\,V$ to $V_{ov,max} = 0.87\,V$, one obtains a decrease of $R_{SD}(V_{ov})$ by $\approx 50\%$.

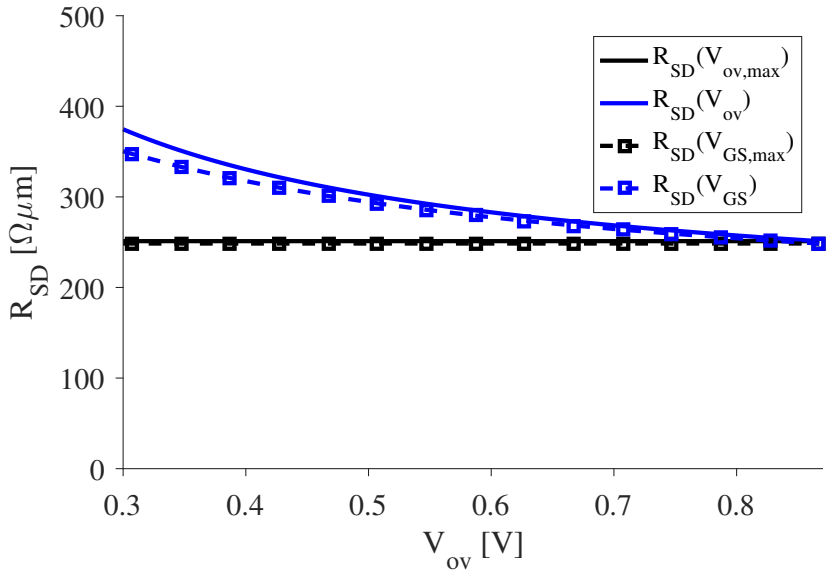

Fig. 6.4: R_{SD} extracted by the total resistance method with (full) and without (dashed squares) V_{ov} normalization for the full mobility model. The dashed curves were downshifted by $V_{TH,mean}$ for easier comparison. Black curves indicate the constant R_{SD} value extracted from $V_{ov,max}$ and $V_{GS,max}$.

6.1.3 Impact on Q_i extraction

Figure 6.5 shows the charge Q_{ext} extracted by integration of $C_{gg,norm}$ (see Eq. (3.10)) without (from $V^*_{GS} = 0\,V$) and with (from $V^*_{ov} = -V_{TH,mean}$) normalization to the overdrive voltage. Normalizing to V_{ov} doesn't significantly modify the extracted charge (though a small impact will be evidenced in Section 6.4.2).

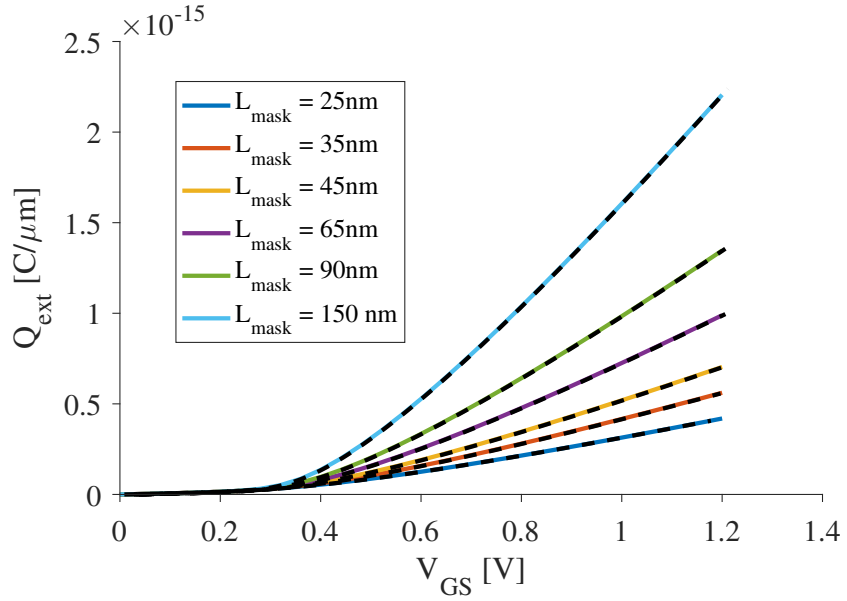

Fig. 6.5: Q_{ext} from integration of $C_{gg,norm}$ without (full) and with (black dashed) V_{ov} normalization. Normalized curves have been plotted agains $V_{GS} = V_{ov} + V_{TH}$ with V_{TH} their respective threshold voltage.

As L_{eff} extraction was also only weakly impacted, (Hyp.4) mostly affects the extraction of the bias dependent R_{SD}. The influence on the extracted mobility will be shown in Section 6.4.
Now (Hyp.4) has been completely removed, one will study the impact of the inner fringing capacitance on L_{eff},Q_i and mobility extraction.

6.2 Impact of inner fringing on L_{eff} extraction

There exist many different effective length extraction methods, either from I-V, C-V measurements or TCAD simulations, most of them being initially designed for bulk transistors [49]. In FDSOI literature, one mostly finds the usual linear interpolation of the gate capacitance against the gate length as used in this work [4, 50]. In [41] Severi et al. also proposed to use $C''_{gg,norm} = C_{gg} - C_{gg}(V_{FB})$ to extract the effective length L_{eff} as defined from a threshold doping concentration (V_{FB} is the flatband voltage). This method wss then applied to UTBB FDSOI MOSFET's down to 45 nm in [42].

In this section, we will highlight the perturbation of this usual linear interpolation method by the inner fringing term. In Section 3.4, Eq. (3.11) was used to extract L_{eff} from $C_{gg,norm}(V_{GS,max}, V_{DS} = 0V)$. After normalization to V_{ov}, Eq. (3.11) is rewritten as

$$C_{gg,norm}(V_{ov,max}, L_{eff}) \approx C_{ggi}(V_{ov} = V_{ov,max}, L_{eff}) \approx C'_{ox}(L_g - \Delta L)$$

with (Hyp.3) assumed valid. However, this is not the case in FDSOI and from Section 5.1.2 one must now write:

$$C_{gg,norm}(V_{ov,max}, L_{eff}) \approx C_{ggi}(V_{ov,max}, L_{eff}) - C_{gge,if}(V_{ov,min}) \tag{6.1}$$

$$\approx C'_{ox}(L_g - \Delta L) - C_{gge,if}(V_{ov,min}) \tag{6.2}$$

One thus has an additional inner fringing term that perturbs the extraction and can potentially lead to an overestimated ΔL. In [46], Benakkez et al. therefore stated that, contrary to bulk devices, one cannot extract L_{eff} with confidence from this method.

It is thus attempted here to verify the extracted L_{eff} by TCAD simualtion results. In [51], it is proposed to extract L_{eff} from the points where the free carrier density in the channel begins to deviate for different V_G voltages. As shown on figure Fig. 5.12, this definition cannot be applied to our structure as the gate voltage modulates the carrier density in the underlaps, well beyond the channel length L_g. In [52], Niu et al. propose another TCAD method, based on the idea that L_{eff} should correspond to the region where the ususal linear channel potential variation can be assumed (in strong inversion). L_{eff} is then extracted from the first extremum of $d^2\phi/dX^2$ where ϕ is the channel potential and X the coordinate along the channel (as in Fig. 2.2).
An attempt at this method is shown in Fig. 6.6 for a $L_{mask} = 25\,nm$ transistor. From the TCAD setup, one has 47 mesh points in $X = [-L_g/2,\ L_g/2]$ for this device. The second derivative of the potential is computed from these points and then spline interpolated to 500 points in the same interval (spline interpolation of the potential before derivation resulted in badly behaved second derivatives). From the first minima of the curve (indicated by datapoints), one gets $L_{eff} \approx 21.9\,nm$, thus $\Delta L = L_g - L_{eff} = 3.6\,nm$.

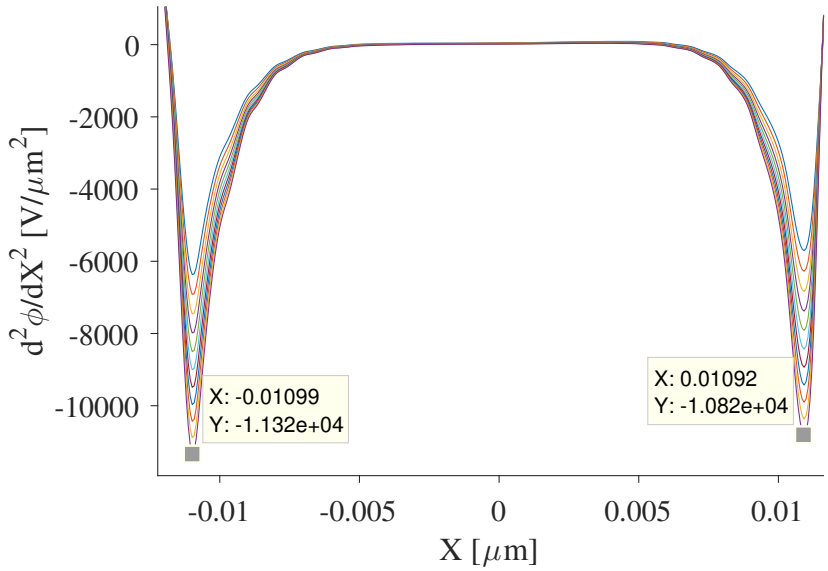

Fig. 6.6: L_{eff} extraction from the second derivative of the channel potential $d^2\phi/dX^2$ at $Y = 0.1\,nm$ below the gate oxide, $V_{GS} = [0.75, 1\,V]$

This result constrasts with $\Delta L = 1.8\,nm$ previously extracted from the gate capactiance. However, it should be taken with care as the TCAD-based method is highly sensitive the number of mesh and interpolation points in the channel. To illustrate this point, reducing the number of points in the channel to 36 (by spline interpolation and sampling) and performing the same method gives $\Delta L = 1.7\,nm$. Therefore, we do not consider the results of this method trustworthy in our case. It would obviously be needed to increase the number of mesh points in the channel, at the cost of higher simulation times.

Nevertheless, Fig. 5.9 showed that the previously obtained $C_{gg,norm}/L_{eff}$ values are well superimposed for all gate lengths in strong inversion, which is not the case for C_{ggnorm}/L_g (not shown). We thus consider the previous L_{eff} extraction satisfying and decide to go on with its values.

6.3 Impact of inner fringing on charge extraction

In this section, one will discuss the contribution of the inner fringing capacitance to the extracted charge. It will be shown significant in short nodes, inducing 10% of relative error on Q_i for a $L_{mask} = 25\,nm$ transistor at $V_{GS} = 0.8\,V$.

In the simple method of Section 3.3, one attempted to extract the inversion charge Q_i as

$$Q_i(V_{GS}) \approx Q_{ext}(V_{GS}) = \int_{V^*_{GS}}^{V_{GS}} C_{gg,norm}(V)dV$$

with V^*_{GS} chosen such that $C_{gge,if}$ is supposed small compared to C_{ggi} (Hyp.6) while $Q_i(V^*_{GS})$ remains negligible (Hyp.5). The variation of V_{TH} with L_g was neglected in this extraction (Hyp.4).

We now normalize all the curves to V_{ov} before the extraction, hence fully taking into account V_{TH} dependence on L_g (the influence of this elimination of (Hyp.4) on charge extraction will be addressed in Section 6.4.2). From the corrected expression of $C_{gg,norm}$ in FDSOI (Eq. (5.3)), one then writes:

$$Q_{ext}(V_{ov}) = \int_{V_{ov}^*}^{V_{ov}} C_{gg,norm} dV \tag{6.3}$$

$$= \int_{V_{ov}^*}^{V_{ov}} [C_{ggi}(V_{ov}) + C_{gge,if}(V_{ov}) - C_{gge,if}(V_{ov,min})] dV \tag{6.4}$$

$$\approx Q_i(V_{ov}) + \int_{V_{ov}^*}^{V_{ov}} [C_{gge,if}(V_{ov}) - C_{gge,if}(V_{ov,min})] dV \tag{6.5}$$

$$\approx Q_i(V_{ov}) + Q_{par}(V_{ov}) \tag{6.6}$$

With the conventional method, the extracted charge Q_{ext} is thus composed of the inversion charge Q_i and a parasitic charge Q_{par} due to the integration of the inner fringing terms.

The alternative capactiance extraction method discussed in Section 5.2 was shown able to correct for this inner fringing capcitance in the extraction of C_{ggi} (see Figures 5.8 and 5.9). As proposed by Vandermolen et al. [34], it can thus naturally be used to estimate Q_i as

$$Q_{iA}(V_{ov}) = \int_{V_{ov}^*}^{V_{ov}} A_1(V) L_{eff} dV \approx \int_{V_{ov}^*}^{V_{ov}} \overline{C_{ggi}(V)} dV \tag{6.7}$$

The charges extracted from the conventional $C_{gg,norm}$ method (Q_{ext}) and from $A_1 L_{eff}$ (Q_{iA}) are compared in Fig. 6.7. As expected, the $C_{gg,norm}$ method overestimates Q_i in strong inversion due to the integration of the inner fringing contribution [34].

As shown on Fig. 6.8, the relative error introduced by Q_{par} is estimated to reach 30% at $V_{GS} = 0.5V$ and 10% at $V_{GS} = 0.8V$ for $L_{mask} = 25\,nm$. As such, it is seen that (Hyp.6) is a poor assumption in short transistors, where the inner fringing capacitance significantly impacts the intrinsic charge extraction. The important consequences for the extracted mobility will be discussed in the next section.

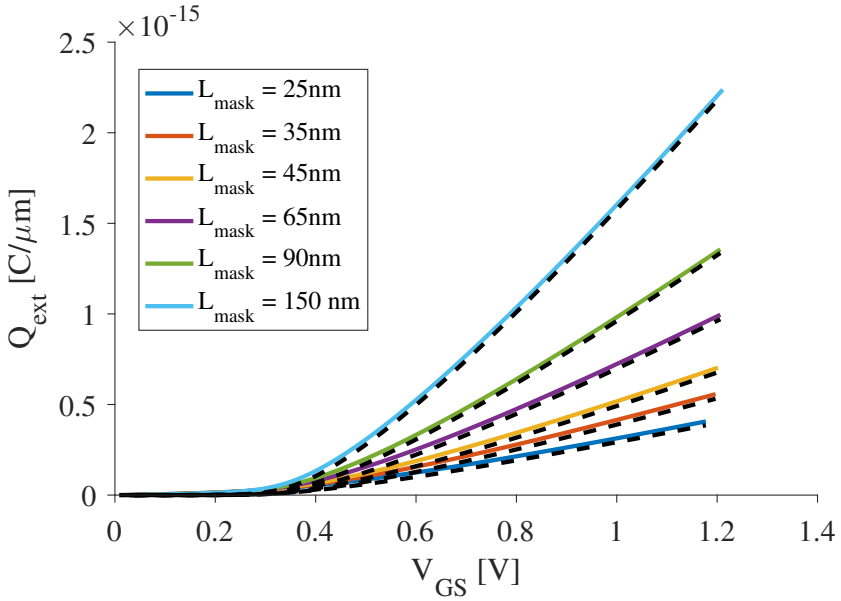

Fig. 6.7: Comparison between $Q_{ext}(V_{GS})$ extracted by integration of $C_{gg,norm}(V_{ov})$ (full) and $Q_{iA}(V_{ov})$ extracted from integration of $A_1(V_{ov})L_{eff} = \overline{C_{ggi}(V_{ov})}$ (black dashed). The curves are plotted against $V_{GS} = V_{ov} + V_{TH}$ with V_{TH} their respective threshold voltage.

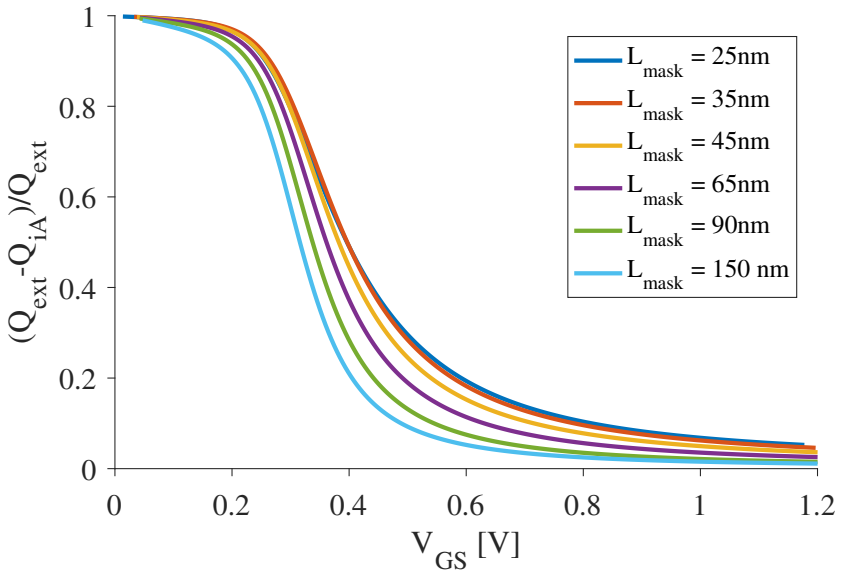

Fig. 6.8: Relative difference between Q_{ext} extracted by integration of $C_{gg,norm}$ and Q_{iA} from integration of $A_1 L_{eff} = \overline{C_{ggi}}$.

6.4 Improved mobility extraction

This section will present improved mobility results using the insights developed earlier in this chapter. Normalization of the extraction to V_{ov} will firslty be seen to have an important influence on the obtained mobility, mostly attributable to its impact on the extracted R_{SD} (see Section 6.1.2).
With this normalization, the alternative capacitance extraction method proposed by Vandermolen et al. will then be confirmed to correct effectively for the inner fringing contribution, yielding much improved extraction results in short transistors. Therefore, after correction for R_{SD} bias dependence and V_{ov} normalization, the inner fringing capacitance will be identified as the major source of apparent mobility degradation in short transistors.

6.4.1 Improved extraction results

Figure 6.9 shows the extracted mobility for the constant TCAD mobility model using integration of $C_{gg,norm}$ or of $A_1 L_{eff} \approx \overline{C_{ggi}}$ (further called "linear interpolation method"), R_{SD} bias dependence being accounted for. The mobility behaviour is well extracted in the long transistor for $V_{GS} > 0.5V$ using $A_1 L_{eff}$, and its underestimation in the short transistor is reduced.

Figure 6.10 shows the same results now with normalization to V_{ov} before the extraction (fully lifting (Hyp.4)). This is seen to have a non-negligible impact on the extracted mobility for $L_{mask} = 25\,nm$. As discussed in Section 6.1.2, the effect is mostly attributable to the extraction of R_{SD} (an additional impact on Q_i extraction will be precised in Section 6.4.2).

With this normalization, the linear interpolation method is now seen to reproduce the constant mobility behaviour well for both long and short transitors over the entire strong inversion range. The relative error between the extracted mobility and the TCAD imposed value is lower than 7.3% and 4.4% for $L_{mask} = 150\,nm$ and $L_{mask} = 25\,nm$ respectively on the $0.3 < V_{ov} < V_{ov,max}$ range (see Fig. A.11 in appendix).

Figures 6.11 and 6.12 show the same results, now applied to the full mobility TCAD model. The extracted mobility in Fig. 6.12 is similar for both transistor lengths. As mentioned in Section 4.2.1,

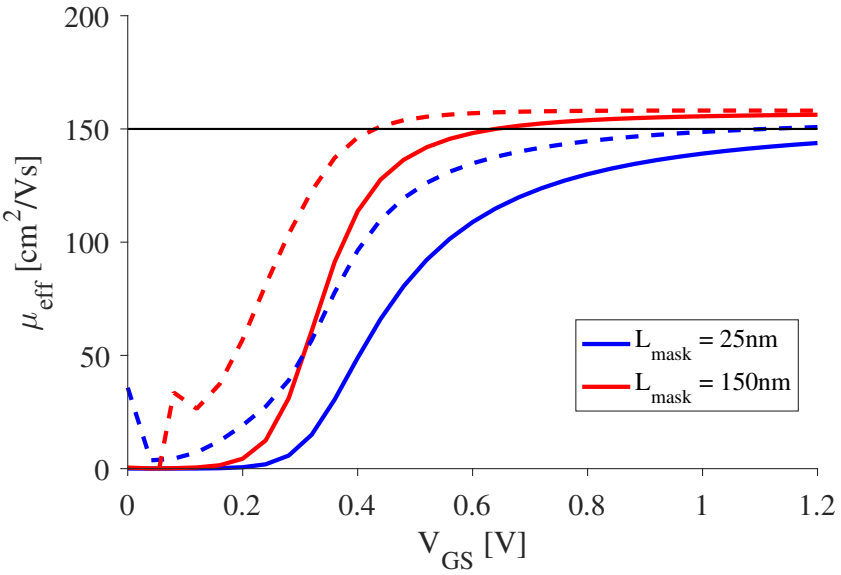

Fig. 6.9: μ_{eff} extracted using $C_{gg,norm}$ integration (full) and $A_1 L_{eff}$ integration (dashed) for the simple mobility model, without initial V_{ov} normalization. The black line indicates the constant mobility $\mu = 150 cm^2/Vs$ implemented in TCAD

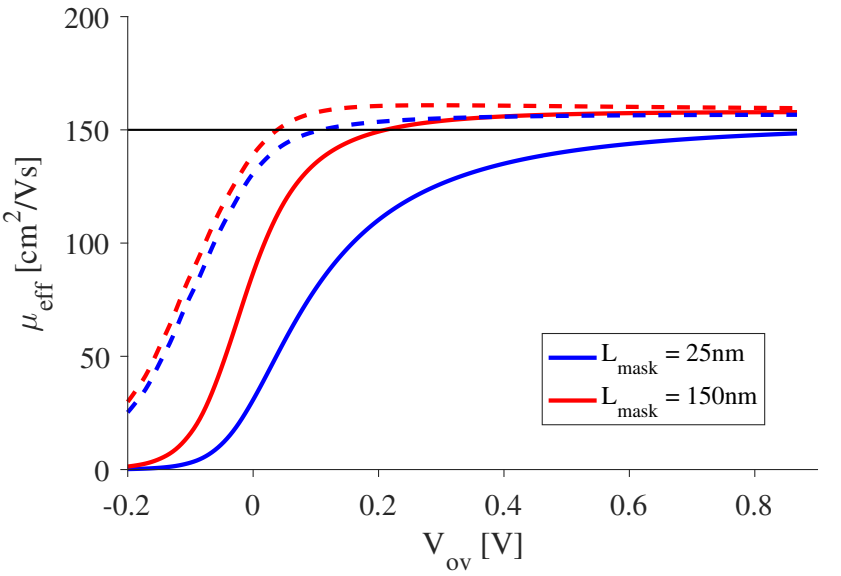

Fig. 6.10: μ_{eff} extracted using $C_{gg,norm}$ integration (full) and $A_1 L_{eff}$ integration (dashed) for the simple mobility model, with initial V_{ov} normalization. The black line indicates the constant mobility $\mu = 150 cm^2/Vs$ implemented in TCAD

this is expected as the doping level in the center of the channel is similar for all lengths, while the mobility degradation due to the high doping of the source and drain diffusions is accounted for through R_{SD} (no neutral defect scattering was introduced in the model). As this S/D doping however lowers μ_{vol} extracted from Eq. (2.3), the comparison is made here against μ_{vol} from a long $L_g = 1\,\mu m$ transistor to minimize its effect.
From Fig. 6.12, the relative error between the extracted mobility and $\mu_{vol,L_g=1\mu m}$ is lower than 8.1% and 5.3% for $L_{mask} = 150\,nm$ and $L_{mask} = 25\,nm$ respectively on the $0.3 < V_{ov} < V_{ov,max}$ range (see Fig. A.12 in appendix).

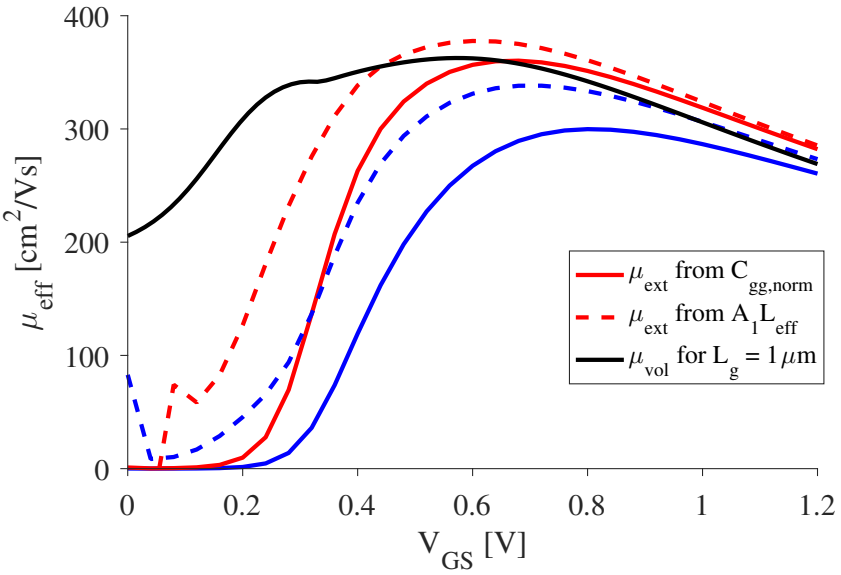

Fig. 6.11: μ_{eff} extracted using $C_{gg,norm}$ integration (full) and $A_1 L_{eff}$ integration (dashed) for the full mobility model, without initial V_{ov} normalization. Blue lines indicate $L_{mask} = 25\,nm$, red lines $L_{mask} = 150\,nm$. The black line indicates μ_{vol} for a $L_{mask} = 1\,\mu m$ transistor.

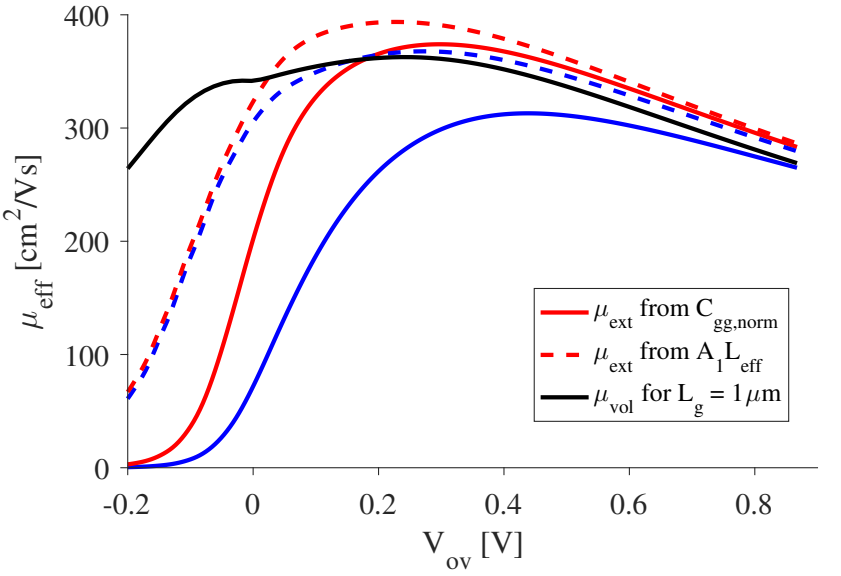

Fig. 6.12: μ_{eff} extracted using $C_{gg,norm}$ integration (full) and $A_1 L_{eff}$ integration (dashed) for the full mobility model, with inital V_{ov} normalization. Blue lines indicate $L_{mask} = 25\,nm$, red lines $L_{mask} = 150\,nm$. The black line indicates μ_{vol} for a $L_{mask} = 1\,\mu m$ transistor.

From these results, it is seen that after normalization to V_{ov} and correction for the R_{SD} bias dependence, the inner fringing capacitance can be identified as the major remaining source of apparent mobility degradation in short transistors. Using the linear extrapolation method effectively corrects for its contribution and enables precise mobility extraction by split CV down to $25\,nm$ in FDSOI transistors. This is considered an important result of this work.

6.4.2 Impact and correction of parasitic charge

The previous results showed how proper V_{ov} normalization and the linear interpolation method enable satisfying split CV mobility extraction by correcting for the parasitic contribution of $C_{gge,if}$ to the charge extraction. Here, the parasitic charge contribution will be studied in more detail using linear interpolation of the extracted charge against L_{eff}. It will be seen that besides the inner fringing capacitance terms, V_{TH} dependence with L_g also introduces error on Q_i when it is not taken into account. Correcting for the constant term ΔQ obtained from linear interpolation of the extracted charge will be shown an effective alternative way to improve the extracted mobility.

From Eq. (6.6), the intrinsic charge Q_i one attempts to extract writes

$$Q_i(V_{ov}) = \int_{V_{ov,min}}^{V_{ov}} C_{ggi}(V)dV = L_{eff} \int_{V_{ov,min}}^{V_{ov}} C'_{ggi}(V)dV \tag{6.8}$$

and is thus proportionnal to L_{eff}. When using the $C_{gg,norm}$ method as in Eq. (6.3), the parasitic contribution Q_{par} results from integration of the inner fringing terms, which are considered independent of the length (Hyp.2). One can therefore also remove this contribution directly from Q_{ext} by interpolating it against L_{eff} as shown on Fig. 6.13.

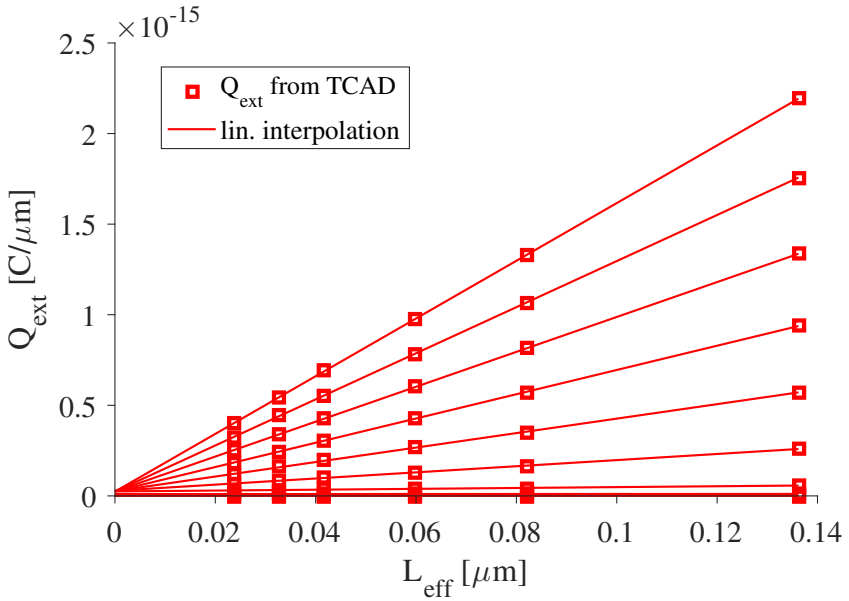

Fig. 6.13: Linear interpolation of Q_{ext} obtained from integration of $C_{gg,norm}$ (starting voltage $V_{ov}^* = -V_{TH,mean}$) for $V_{ov} = -0.3V$ (lower curve) to $0.85V$ (higher curve). Full normalization to the gate voltage overdrive was performed before the extraction

The extracted constant term ΔQ is shown on Fig. 6.14a. Taking the derivative of ΔQ w.r.t. V_{ov}, one retrieves the contribution of the $\overline{C_{gge,if}}$ terms as expected (Fig. 6.14b). Thus, equivalently to the linear interpolation method, one can substract ΔQ to Q_{ext} to retrieve the intrinsic inversion charge Q_i.

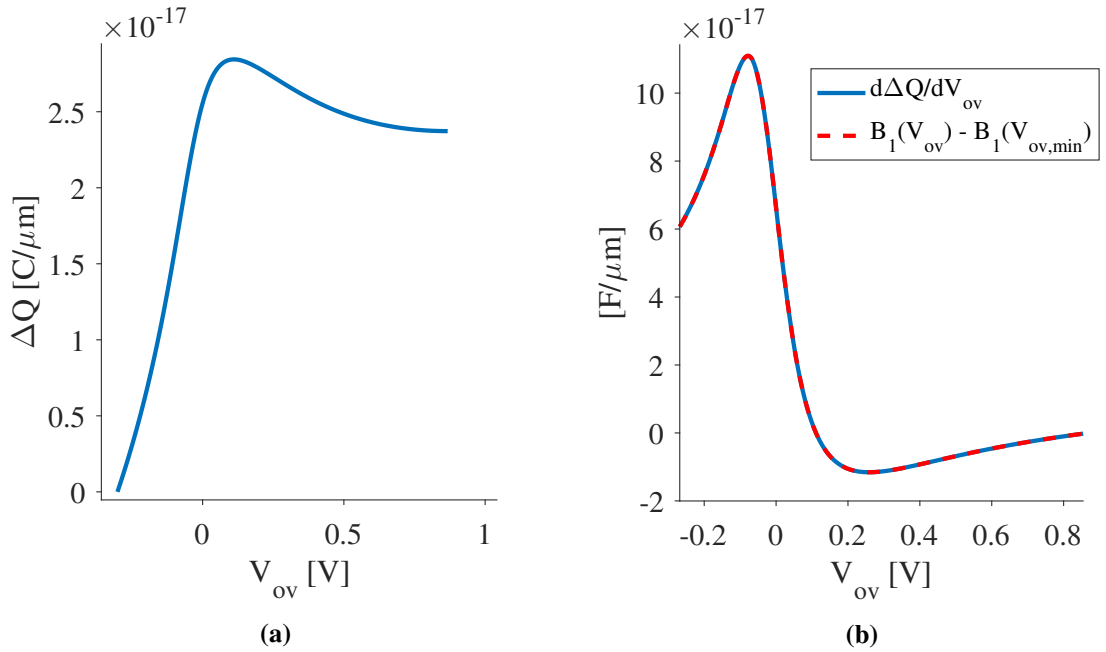

Fig. 6.14: **(a)** Q_{par} extracted from linear interpolation of Q_{ext} against L_{eff} **(b)** $\frac{dQ_{par}}{dV_{ov}}$ compared to the parasitic contribution $B_1(V_{ov}) - B_1(V_{ov,min}) = \overline{C_{gge,if}(V_{ov})}$

This method can also be applied to evaluate the parasitic charge resulting from V_{TH} variation with L_g when it is neglected in the extraction (Hyp.4). Figures 6.15 and 6.16 show ΔQ and $d\Delta Q/dV_{GS}$ obtained from linear interpolation of the extracted charge against L_{eff} for the different charge extraction methods (with and without normalization to V_{ov}).

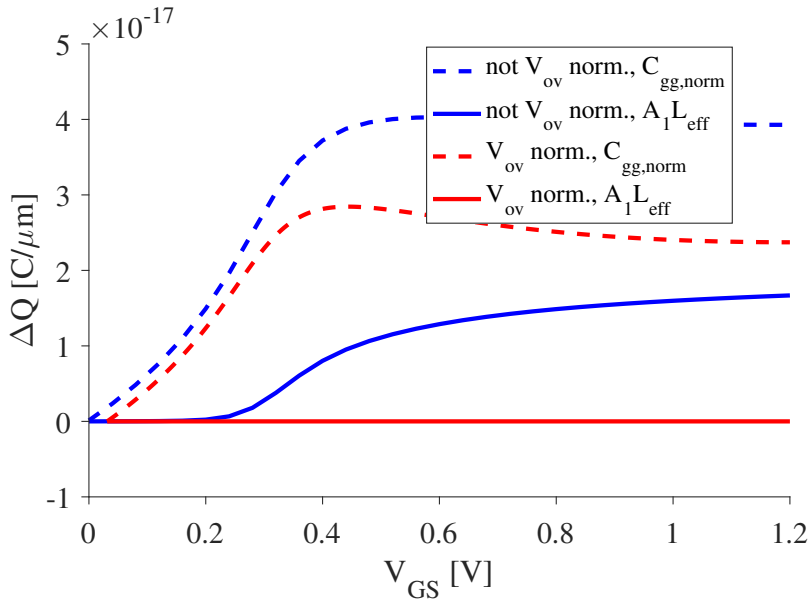

Fig. 6.15: $\Delta Q(V_{GS})$ extracted from linear interpolation of Q_{ext} against L_{eff} for the different Q_i extraction methods, i.e. with or without inital V_{ov} normalization and integrating either $C_{gg,norm}$ or $A_1 L_{eff}$. V_{ov} normalized curves have been plotted against $V_{GS} = V_{ov} + V_{TH}$ with V_{TH} their respective threshold voltage.

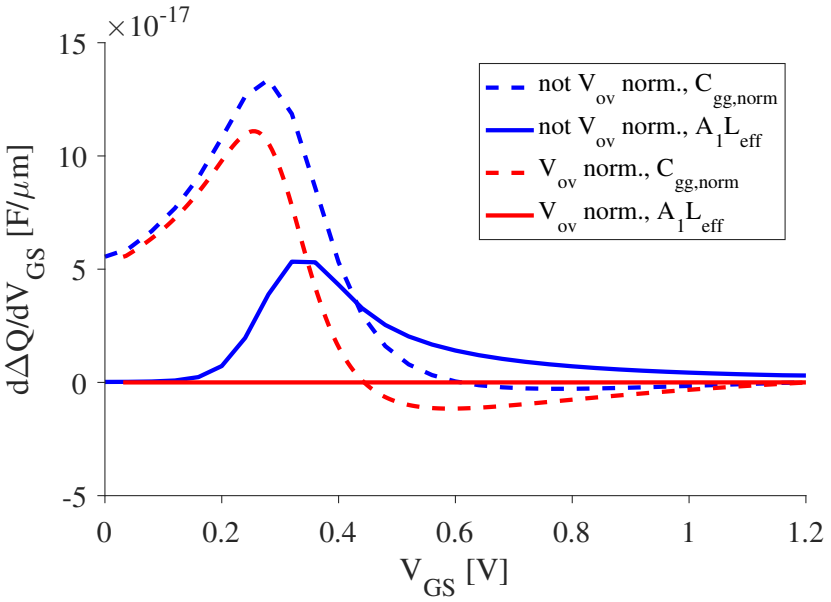

Fig. 6.16: $\frac{d\Delta Q}{dV_{GS}}$ for the different Q_i extraction methods. V_{ov} normalized curves have been plotted against $V_{GS} = V_{ov} + V_{TH}$ with V_{TH} their respective threshold voltage.

As expected, one has $\Delta Q = 0$ in the case of the V_{ov} normalized, linear interpolation method (i.e. using $A_1 L_{eff}$) as

$$Q_{iA} = \int_{V_{ov}^*}^{V_{ov}} A_1(V) L_{eff} dV$$

is per definition direclty proportional to the used L_{eff}. However, when one doesn't normalize the curves to V_{ov} before the integration, we have:

$$Q_{iA} = \int_{V_{GS}^*}^{V_{GS}} A_1(V + V_{TH}(L_{eff})) L_{eff} dV \tag{6.9}$$

$$= \int_{V_{ov}^* + V_{TH}(L_{eff})}^{V_{ov} + V_{TH}(L_{eff})} A_1(V + V_{TH}(L_{eff})) L_{eff} dV \tag{6.10}$$

$$= \int_{V_{GS}^* - V_{TH}(L_{eff})}^{V_{GS} - V_{TH}(L_{eff})} A_1(V) L_{eff} dV \tag{6.11}$$

Thus, because the integration was performed for the same V_{GS} boundaries for all transistors, the corresponding V_{ov} boundaries depend on L_{eff} through the variation of V_{TH} with the gate length. This introduces error on the extracted charge as seen on Fig. 6.15, and is an additional impact of (Hyp.4) on the mobility extraction (besides its (more important) effect on R_{SD} as discussed in Section 6.1.2).

The same reasoning naturally applies to the integration of $C_{gg,norm}$, where ΔQ is then mostly due to the inner fringing terms, but also has a contribution of the V_{TH} dependance on the length.

Simply substracting ΔQ to the extracted charge is an alternative way to correct for both the impact of the inner fringing and of the V_{TH} variation with L_g.
Figure 6.17 shows the obtained mobility using $C_{gg,norm}$ or $A_1 L_{eff}$ and with or without normalization of V_{ov} prior to the extraction. As expected, using $C_{gg,norm}$ and neglecting V_{ov} normalization both result in degraded extraction.
Figure 6.18 shows the same results with ΔQ substracted to the extracted charge. The mobility extraction is much improved for the methods which use $C_{gg,norm}$ or neglect V_{ov} normalization. They now give close results to the best V_{ov} normalized, $A_1 L_{eff}$ based extraction.

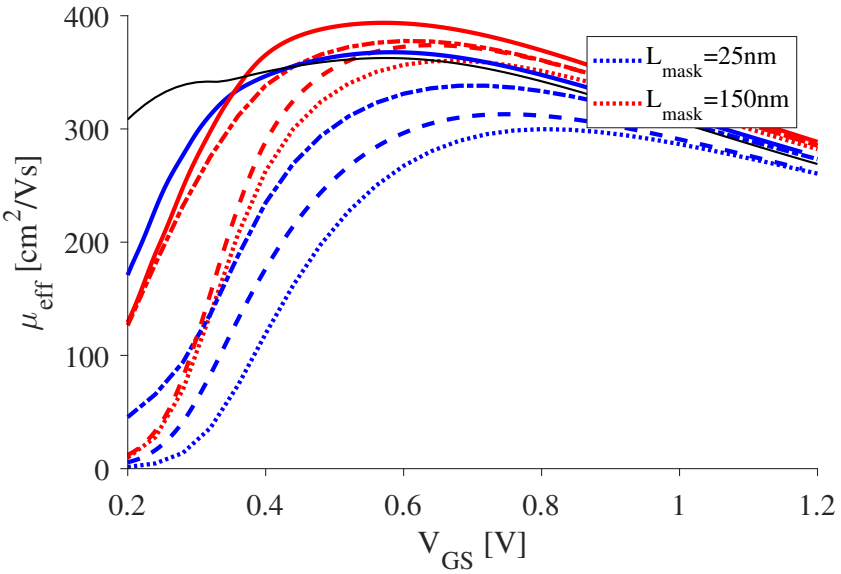

Fig. 6.17: μ_{eff} extracted using $C_{gg,norm}$ (dots) and $A_1 L_{eff}$ (dash-dots) integration without V_{ov} normalization, and $C_{gg,norm}$ (dashed) and $A_1 L_{eff}$ (full) integration with V_{ov} normalization for the full mobility model. The black line indicates μ_{vol} from a $L_{mask} = 1\mu m$ transistor.

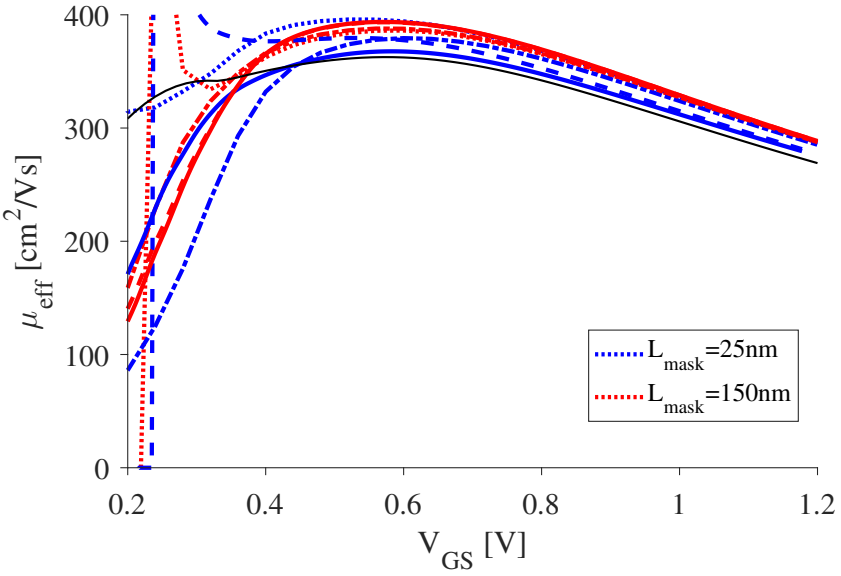

Fig. 6.18: μ_{eff} extracted with correction of ΔQ for the full mobility model, using $C_{gg,norm}$ (dots) and $A_1 L_{eff}$ (dash-dots) integration without V_{ov} normalization, and $C_{gg,norm}$ (dashed) and $A_1 L_{eff}$ (full) integration with V_{ov} normalization. The black line indicates μ_{vol} from a $L_{mask} = 1\mu m$ transistor.

6.5 Summary and conclusion

This chapter studied the impact of the inner fringing capacitance on the split CV mobility extraction. A first step was to normalize the extraction to $V_{ov} = V_{GS} - V_{TH}$ to fully account for V_{TH} variation with L_g and get rid of (Hyp.4). This was seen to have a non-negligible impact on the extracted mobility, mainly attributable to influence on R_{SD} extraction.

One then assessed the impact of the inner fringing on L_{eff} estimation. It was seen to be perturbed by the inner fringing capacitance term at $V_{ov,min}$. Nevertheless, L_{eff} was considered well extracted in

our case.
The contribution of the inner fringing capacitance was shown significant in short transistors. Using $\overline{C_{ggi}}$ as obtained from the alternative capacitance extraction method was confirmed to correct for this contribution. Mobility extraction results in good agreement with the TCAD implemented mobility (less than 10% relative error) were then obtained. This indicates that the inner fringing capacitance, through the parasitic charge it generates, can be identified as the major source of the remaining mobility underestimation by the split CV method in short transistors (after V_{ov} normalization and $R_{SD}(V_{GS})$ correction).

Finally, correcting for the constant ΔQ term obtained from linear interpolation of the extracted charge against L_{eff} was proposed as an alternative way to correct for for both the impact of the inner fringing and of the V_{TH} variation with L_g.

In the next chapter, measurements on 28nm FDSOI transistor will be used to qualitatively back up above insights from the TCAD analysis.

7 Validation on 28FDSOI measurements

In the previous chapter, TCAD simulations were used to assess the limitations of the split CV mobility extraction technique in FDSOI transistors down to $L_{mask} = 25\,nm$. The increased importance of parasitics neglected by the ususal approximations was shown responsible for erroneous mobility extraction in short transistors. Notably, the access resistance bias dependence and the inner fringing capacitance contribution to the extracted charge were identified as the major sources of difficulties. An improved mobilty extraction was then presented and seen to correct for these phenomena. Its different steps are recalled here:

1. Extraction of V_{TH} for all transistor lengths and normalization of C-V and I-V curves to $V_{ov} = V_{GS} - V_{TH}$
2. Extraction of L_{eff} from $C_{gg,norm} = C_{gg} - C_{gg}(V_{ov,min})$ at $V_{DS} = 0\,V$
3. Extraction of the bias dependent $R_{SD}(V_{ov})$ with the total resistance method
4. Extraction of the intrinsic gate capcitance by the linear interpolation method proposed in [34]
5. Computation of the effective mobility

In this chapter, this method will be applied to measurements of 28nm FDSOI transistors.
A quantitative analysis would require several identical measurements on each device such that one can estimate the measurement error and study how it propagates in the extraction. Different sets of devices should also in all rigor be measured to get a statistical insight on the variability of their parameters. In the frame of this work, single measurements on one set of devices with different gate lengths will be used. The aim is to qualitatively back up the insights from the TCAD simulations.
The bias dependence of R_{SD} as extracted with the total resistance method will indeed be retrieved. Moreover, the linear interpolation method proposed by Vandermolen et al. [34] will be confirmed successfull in modeling the gate capacitance C_{gg}. Extracted mobility results with the above corrections will finally be presented.

7.1 Devices description and measurement set-up

The measured devices are 28nm FDSOI UTBB transistors from ST-Microelectronics [25]. Their structure and gate stack were closely reproduced in the TCAD deck, and were thus described in Chapter 2.
The used mask lengths are L_{mask} are 25, 35, 45, 60, 90 and $150\,nm$ and the actual gate length after lithography is given by $L_g = 0.9L_{mask} + 3\,nm$. Each transistor has 10 fingers with $W_{finger} = 2\,\mu m$,

and 6 devices are connected together, giving $W_{mask} = 120\mu m$. The effective with W_{eff} is then given by $W_{eff} = 0.9 * W_{mask}$.

DC I-V curves were measured for $V_{DS} = 50\,mV$ and $V_{GS} = [0.2, 1.2\,V]$ with a $10\,mV$ step.
S parameters were obtained for $V_{DS} = 50\,mV$ and $V_{DS} = 0\,V$ (cold regime), $V_{GS} = [0.2, 1.2\,V]$ with a $10\,mV$ step and $f = [10\,MHz, 35\,GHz]$ with a $99.12\,MHz$ step.

The measured S-parameters are de-embedded using the open pad method [53] and then converted to Y parameters. Figure 7.1 shows the obtained imaginary part of Y_{11} versus frequency for a $L_{mask} = 25\,nm$ transistor (port 1 refers to the gate, port 2 to the drain contact, the source and bulk are fixed at the reference ground).

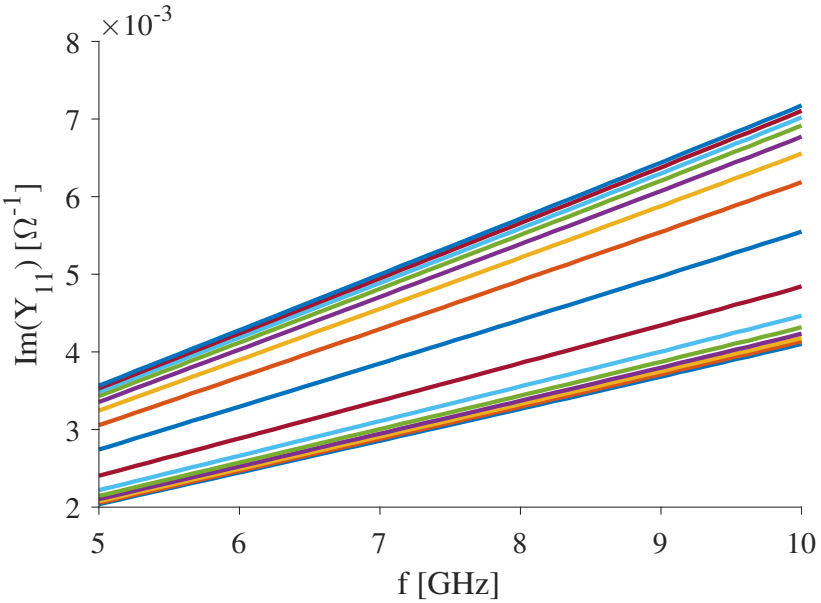

Fig. 7.1: $Im(Y_{11})$ versus frequency for $V_{GS} = -0.2\,V$ (lowest curves) to $1.2\,V$ (highest curve)

The total gate capacitance is then extracted from the slope of $Im(Y_{11}) = 2\pi f C_{gg}$ by linear interpolation against the frequency over $f = [5,\ 10\,GHz]$. The obtained $C_{gg}(V_{GS})$ curves for the different lengths are shown in Fig. 7.2 (note averaging the value of $Im(Y_{11})$ over the same frequency range and dividing it by the pulsation $2\pi f$ gives sensibly same results).

7.2 Threshold voltage extraction and normalization to V_{ov}

Figure 7.3 shows the extraction of the threshold voltage V_{TH} by different methods. I-V and C-V curves were spline interpolated to 500 points between $V_{GS,min} = -0.2\,V$ and $V_{GS,max} = 1.2\,V$.
Extracting V_{TH} from the maximum of dC_{gg}/dV_{GS} resulted in difficulties as the dC_{gg}/dV_{GS} curve is seen perturbed by periodic oscillations (see Fig. A.13). Moreover, even after smoothing by a moving average filter, an increase in V_{TH} is obtained when reducing the length from $L_{mask} = 65\,nm$. A similar result was obtained by Vandermolen in [34]. The origin of this is unclear, and might stem from an increased importance of the parasitic bottom channel [38].
The extraction of V_{TH} might also be perturbed by a measurement error on C_{gg}. Its value cannot be estimated here as no repeated measurements were available. One can cite similar measurements from [54], where an error of $\pm 7fF$ on the total gate capacitance C_{gg} was estimated. Such a value would in our case represent a variation of the order of $\pm 10\%$ of $C_{gg}(V_{GS} = V_{TH})$ for $L_{mask} = 25\,nm$.

From these elements, it is decided here to rather use the results from the non-linear optimization method. As seen on Fig. 7.3, its obtained V_{TH} values are close to the ones extracted from dC_{gg}/dV_{GS}

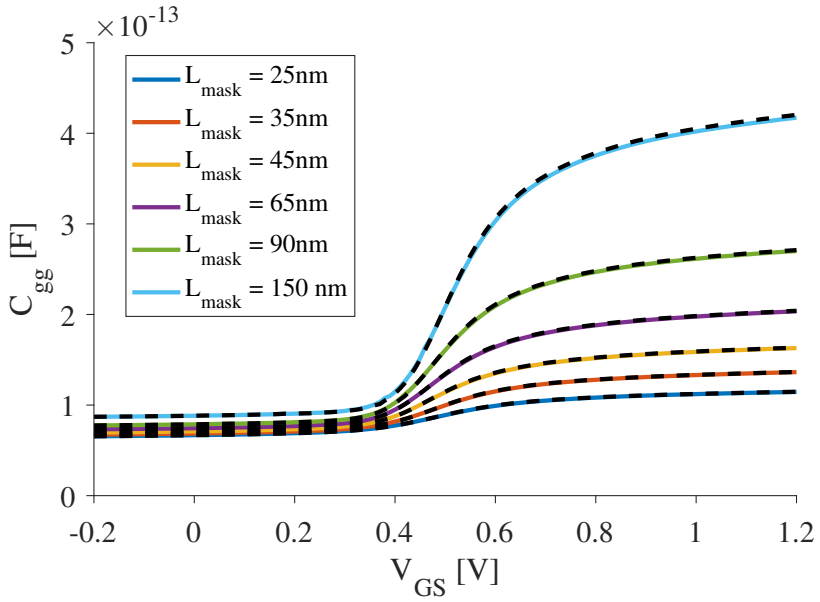

Fig. 7.2: Total gate capacitance C_{gg} versus V_{GS} extracted from linear interpolation of $Im(Y_{11})$ against $2\pi f$ for $f = [5,\ 10\,GHz]$ (colors) and from averaged value of $Im(Y_{11})$ over $f = [5,\ 10\,GHz]$ divided by $2\pi f$ (black dashed)

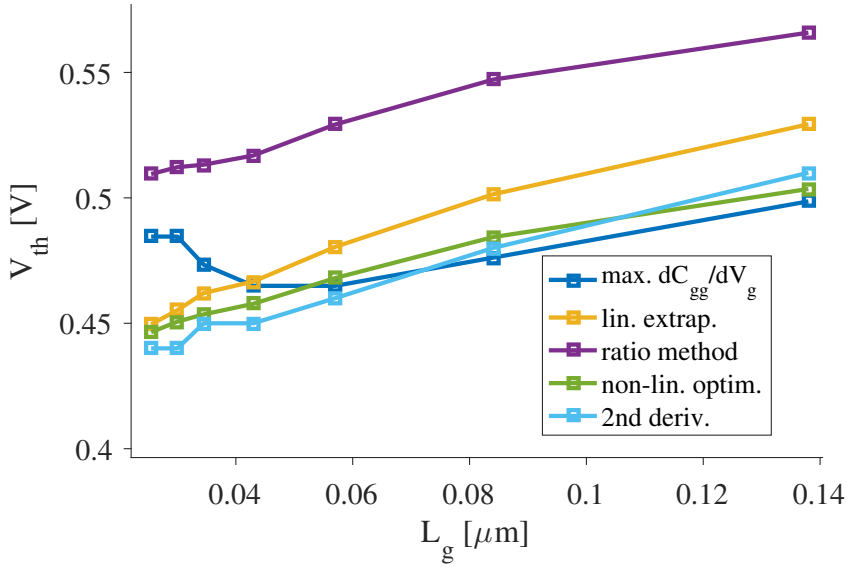

Fig. 7.3: V_{TH} extracted by several methods: maximum gate capacitance derivative, linear extrapolation, ratio method, non-linear optimzation and second derivative method. The g_m/I_d method gives erroneous results which are thus not shown here (note no further efforts were made in correcting them).

for $L_{mask} > 65\,nm$ and do not show an increase for lower lengths.

I-V and C-V curves are then normalized to $V_{ov} = V_{GS} - V_{TH}$ and spline interpolated from $V_{ov,min} = V_{GS,min} - V_{TH,mean}$ to $V_{ov,max} = V_{GS,max} - V_{TH,mean}$ (see Section 5.2.1). The result is shown in figures 7.4 and 7.5. $C_{gg,norm}$ obtained as

$$C_{gg,norm}(V_{ov}) = C_{gg}(V_{ov}) - C_{gg}(V_{ov,min}) \tag{7.1}$$

with $V_{ov,min} = -0.67\,V$ is also shown on Fig. 7.5.

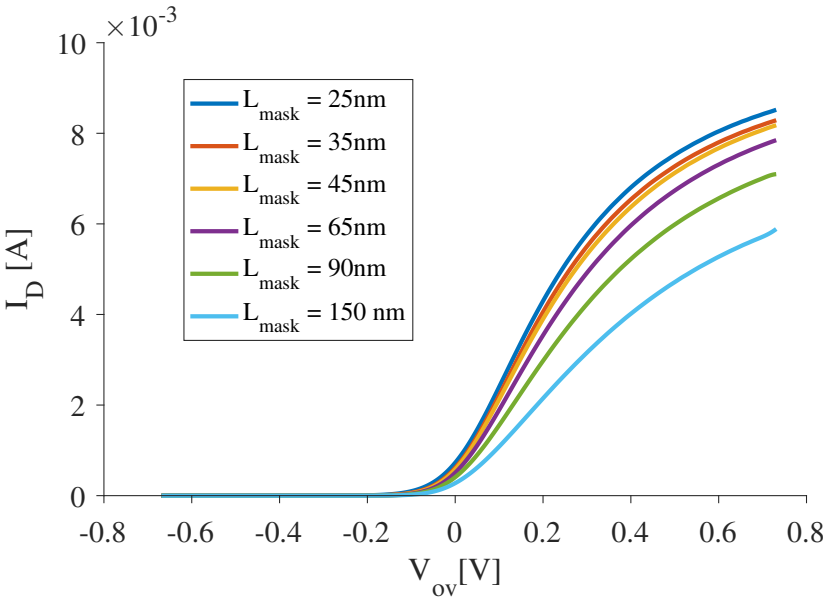

Fig. 7.4: Measured drain current I_D versus $V_{ov} = V_{GS} - V_{TH}$ for the different transistor lengths. $V_{DS} = 50\,mV$

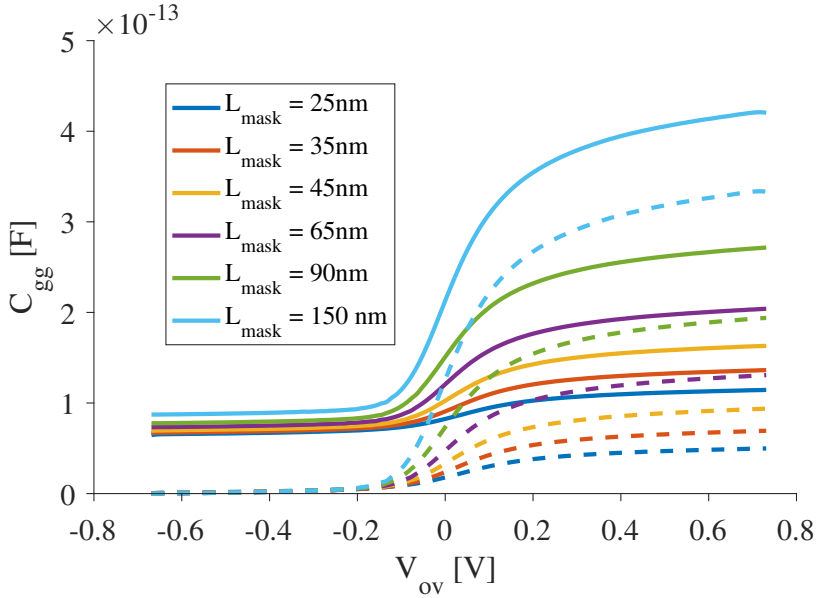

Fig. 7.5: Measured total gate capacitance C_{gg} and $C_{gg,norm}$ versus V_{ov}, $V_{DS} = 50\,mV$.

7.3 Extraction of L_{eff}

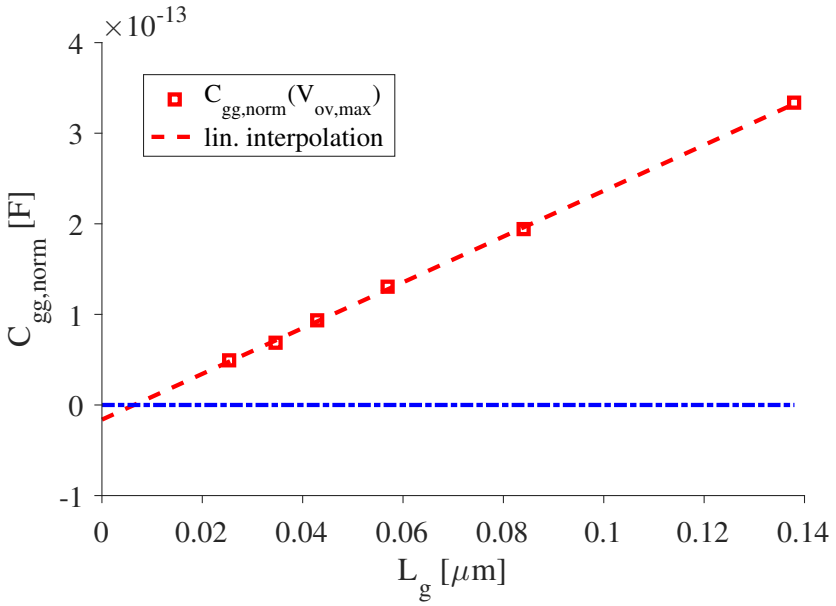

Fig. 7.6: L_{eff} extraction from linear interpolation of measured $C_{gg,norm}(V_{ov} = V_{ov,max}, V_{DS} = 0\,V)$ versus L_g data. The blue line indicates the zero on the capacitance axis.

Figure 7.6 shows the extraction of L_{eff} from linear interpolation of $C_{gg,norm}(V_{ov} = V_{ov,max}, V_{DS} = 0\,V)$ against L_g. Using all lengths, one obtains $\Delta L = 6.5\,nm$, with the four smallest ones $\Delta L = 7.5\,nm$ and with three smallest ones $\Delta L = 6.6\,nm$. It should again be underlined that the extraction might be impacted by measurement errors on the gate capcitance and by errors in the threshold voltage extraction (both impacting the value of $C_{gg,norm}(V_{ov,max})$). It is therefore preferable to use the largest number of available lenghts to extract L_{eff}.

7.4 Access resistance $R_{SD}(V_{GS})$ extraction

Figure 7.7 shows the extraction of R_{SD} with the total resistance method for different overdrive voltages in strong inversion. As discussed in Section 4.2.1, application of this method assumes that μ_{eff} is independent of the gate length (such that R_m can be considered linear with respect to L_{eff}).
Note that the linear interpolation of R_m will not only be impacted by possible μ_{eff} variation with L_{eff}, but also by uncertainty on L_{eff} and V_{TH} extraction for the different transistors.

Figure 7.8 nevertheless shows an extracted $R_{SD}(V_{ov})$ behaviour in agreement with the tendency from TCAD results. R_{SD} decreases by a significant 42% from $V_{ov} = 0.2\,V$ to $V_{ov} = 0.7\,V$ (when using all gate lengths). This figure also assesses the linearity of R_m. Using only the three smallest gate lenghts results in an increase of the extracted R_{SD} value by 6.5% at $V_{ov} = 0.7\,V$, rising to 13% at $V_{ov} = 0.2\,V$.

7.5 Gate capacitances

Figure 7.9 shows the linear interpolation of the total gate capacitance $C_{gg}(V_{ov})$ versus L_{eff}. Measurement errors on C_{gg} influence the linear interpolation both directly via the C_{gg} values and indirectly via their impact on L_{eff} extraction.

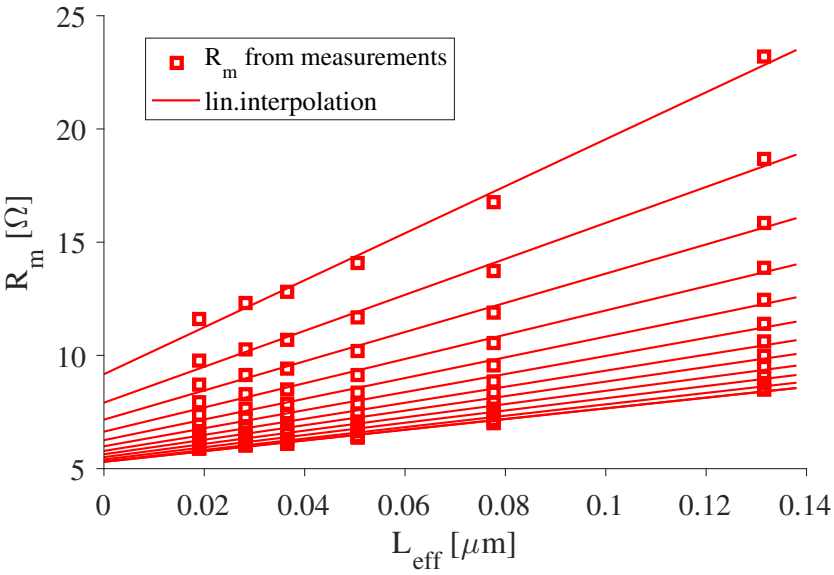

Fig. 7.7: R_{SD} extraction from linear regression of the total resistance $R_m = V_{DS}/I_D$ for $V_{ov} = 0.2\,V$ (higher curve) to $V_{ov} = 0.7V$ (lower curve). V_{TH} was extracted with the non-linear optimization method.

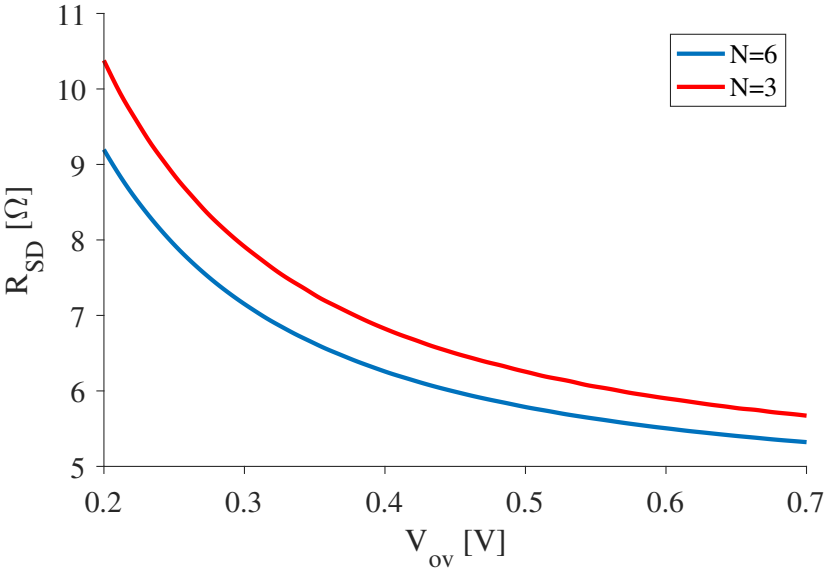

Fig. 7.8: R_{SD} from linear regression of the measured $R_m(V_{ov})$ for different number of lengths N (starting from the smallest one). V_{TH} was extracted from the non-linear optimization method.

Nevertheless, the ability of the linear interpolation method to model the gate capacitance is confirmed here for both long and short transistors. The gate capacitance is reconstructed from its linear interpolation coefficients with less than 2.5% relative error for all lenghts and overdrive voltages (see Fig. A.20 in appendix). Figures 7.10 and 7.11 show the results for $L_{mask} = 150\,nm$ and $L_{mask} = 25\,nm$ (results for all lengths can be found in Appendix A.2 , figures A.14-A.19).

One remarks here the important contribution of parasitics to C_{gg} for $L_{mask} = 25\,nm$, which outweighs the intrinsic part on the entire voltage range.

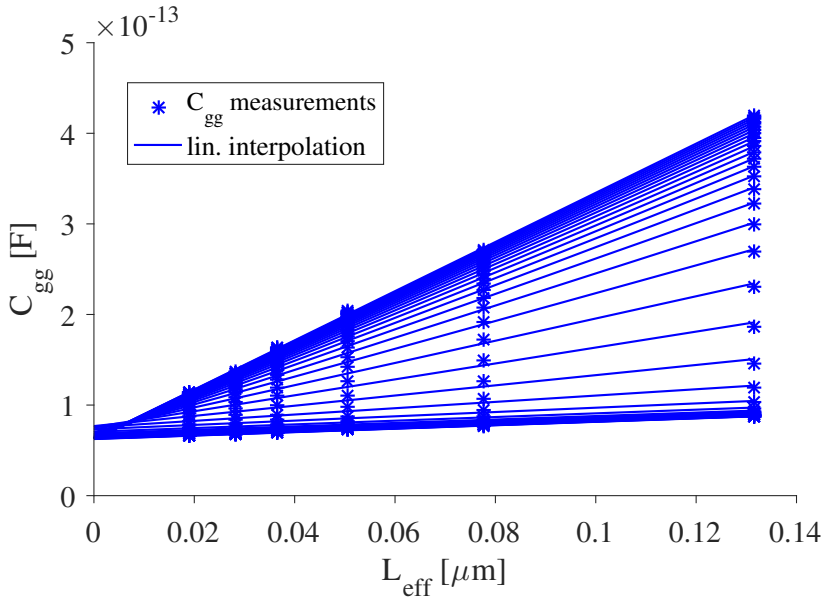

Fig. 7.9: Interpolation of the total gate capacitance C_{gg} against L_{eff} for V_{ov} from $V_{ov,min}$ (lowest curve) to $V_{ov,max}$ (highest curve)

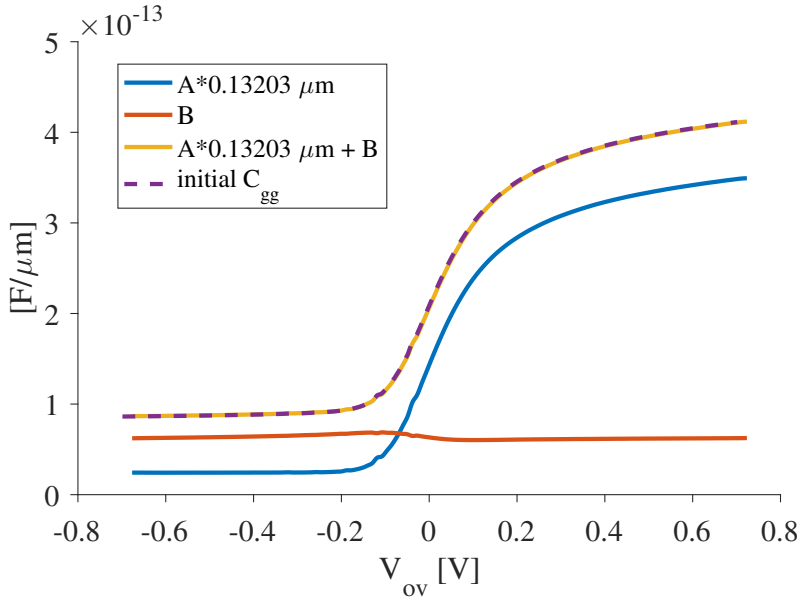

Fig. 7.10: Modeling of the total gate capacitance C_{gg} by the linear interpolation method. The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 150\,nm$, $L_{eff} = 132\,nm$

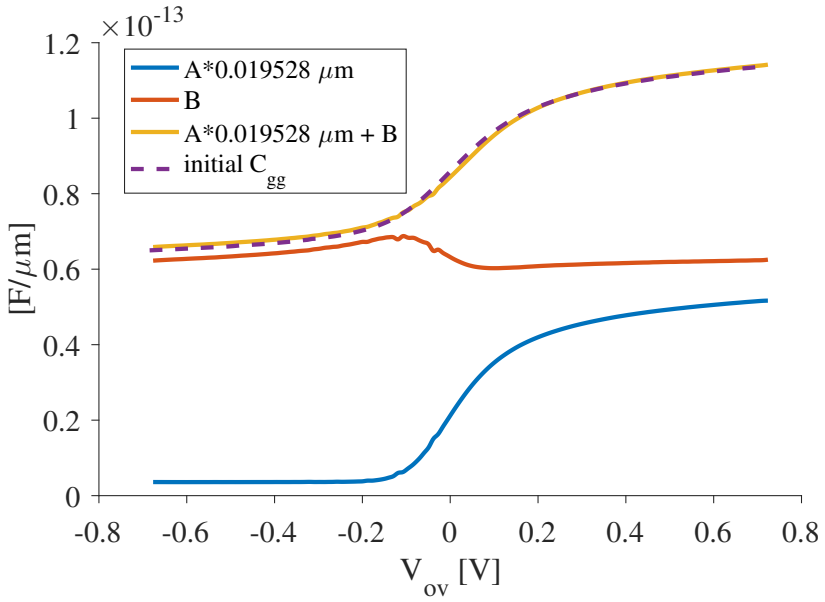

Fig. 7.11: Modeling of the total gate capacitance C_{gg} by the linear interpolation method. The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 25\,nm$, $L_{eff} = 19.5\,nm$

7.6 Mobility results

Figure 7.12 shows the mobility obtained using $C_{gg,norm}$ with ΔQ correction and using $A_1 L_{eff}$ from the linear interpolation of C_{gg}. Normalization to V_{ov} and correction for the bias dependence of R_{SD} are performed in both cases. The reader is referred to Figure A.21 in appendix for the impact of the different corrections on the extracted mobility. Extracted mobilities using V_{TH} from the maximum of dC_{gg}/dV_{GS} are also shown in appendix (Figures A.22 and A.23).

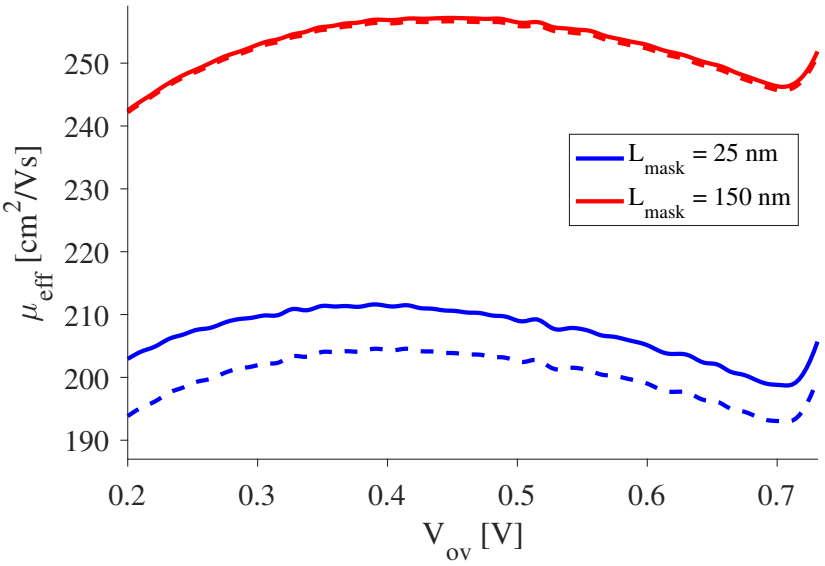

Fig. 7.12: Split CV extracted mobility, V_{TH} extracted from the non-linear optimization method. Dashed: integration of $C_{gg,norm}$, $R_{SD}(V_{ov})$, ΔQ correction, Full: integration $A_1 L_{eff}$, $R_{SD}(V_{ov})$

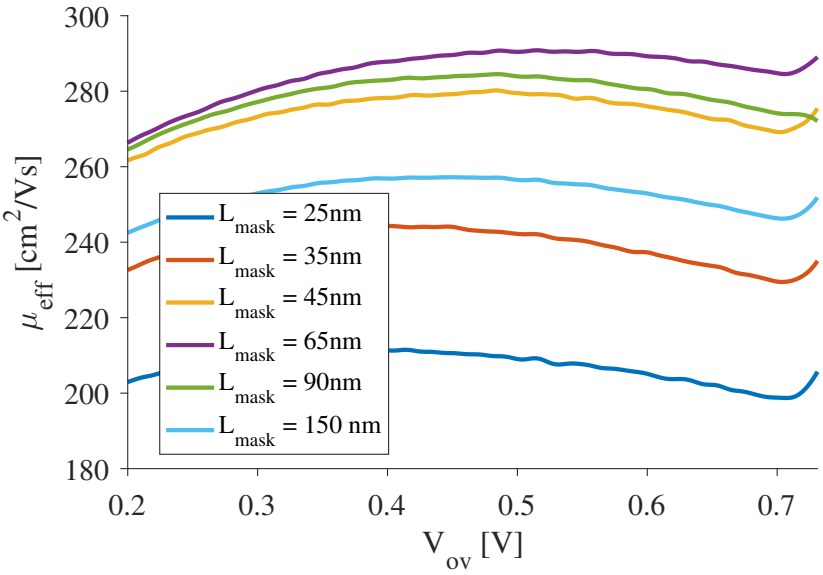

Fig. 7.13: μ_{eff} extracted from the measurements with $A_1 L_{eff}$ integration, correction $R_{SD}(V_{ov})$ and full V_{ov} normalization. V_{TH} was extracted with the non-linear optimization method

Figure 7.13 shows the extracted mobilities for all transistor lenghts. One retrieves the expected behaviour and qualitative mobility values (quantitative discussion is difficult here as, it would again require to account for measurement uncertainty and variability). The unexpected increase near $V_{ov,max}$ is not considered physical. It might be attributable to the extrapolation of the curves near $V_{ov,max}$ during normalization to V_{ov}. One also remarks that the maximum mobility is extracted for $L_{mask} = 65\,nm$ (the same result was obtained using dC_{gg}/dV_{GS} extraction of V_{TH}, see Fig. A.23). This could be due to mechanical stress in the channel, more pronounced in short nodes and thus leading to an optimum L_{eff} in terms of mobility. The effect of the back channel (as for V_{TH} extraction from dC_{gg}/dV_g) might also be a possible explanation. Assessing these hypotheses would again require more extensive measurements.

7.7 Summary and conclusion

In this chapter, the improved mobility extraction method developed from TCAD simulations was applied to measurements of 28nm FDSOI transistors. The purpose was to back up the insights of the TCAD simulations in a qualitative manner.

The important bias dependence of R_{SD} as extracted with the total resistance method was indeed retrieved and seen to have major impact on the extracted mobility. Moreover, the linear interpolation method from Vandermolen et al. [34] was confirmed successfull in modeling the gate capacitance C_{gg}. Extracted mobility results with the above corrections were finally presented, showing qualitatively expected values and behaviour.

It was underlined throughout the extraction that a meaningful quantitative discussion would require estimation of the measurement errors and device variability. In the frame of this work, the single measurements on one set of devices were nevertheless sufficient to retrieve the main tendencies from the TCAD analysis.

8 Conclusion and outlook

Carrier mobility extraction is challenging in advanced transistors as the relative importance of parasitics rapidly increases with reduction of the dimensions. Extraction methods initially designed for long transistors must thus be adapted by incorporating proper extraction and correction of these parasitics for highly scaled devices.
This work aimed at studying the application of the well known split CV method in advanced FDSOI transistors with gate lengths down to $L_{mask} = 25\,nm$. TCAD simulations were proposed as a useful tool to assess the method at its different steps. Indeed, they make it possible to study its intrinsic limitations reliably, free of possible measurement or de-embedding artifacts, and can provide the link with the device physics.

A two-dimensional TCAD simulation structure was provided by CEA-Leti, with geometry and doping profiles considered close to 28FDSOI technology. Its inital constant mobility model was complemented by a more physical, qualitatively correct mobility behaviour. Both models were then used to assess the performance of the mobility extraction procedure.

A simple conventional split CV method was firstly applied to the TCAD extracted I-V and C-V curves. The extraction is valid in strong inversion and linear regime. In these conditions, one has

$$\mu_{eff} = \frac{L_{eff}^2 I_D}{Q_i V_{DS}^{'}}$$

with $V_{DS}^{'} = V_{DS} - R_{SD} I_D$. Computing the effective mobility μ_{eff} thus requires the extraction of the effective length L_{eff}, inversion charge Q_i and access resistance R_{SD}.

The inversion charge Q_i is ideally obtained by integration of the intrinsic gate capacitance, and thus requires the elimination of parasitics from the total gate capacitance C_{gg}. As classically done, one defined:

$$C_{gg,norm}(V_{GS}, L_{eff}) = C_{gg}(V_{GS}, L_{eff}) - C_{gg}(V_{GS,min}, L_{eff})$$

with $V_{GS,min}$ chosen in accumulation. Assuming the following usual contributions to the total gate capacitance:

$$C_{gg} = C_{ggi}(V_{GS}, L_{eff}) + C_{gge,ov} + C_{gge,of}(L_{eff}) + C_{gge,if}(V_{GS})$$

one obtained

$$C_{gg,norm}(V_{GS}, L_{eff}) \approx C_{ggi}(V_{GS}, L_{eff}) + C_{gge,if}(V_{GS})$$

which already showed the parasitic contribution of the inner fringing capacitance. The latter expression relies on the following assumptions:

- (Hyp.1) The outer fringing and overlap capacitances $C_{gge,of}$ and $C_{gge,ov}$ are considered independent of the gate voltage
- (Hyp.2) The inner fringin capacitance $C_{gge,if}$ is taken independent of the length L_{eff}
- (Hyp.3) The inner fringing capacitance $C_{gge,if}$ is assumed shielded in accumulation regime (at $V_{GS} = V_{GS,min}$)
- (Hyp.4) The threshold voltage variation with L_{eff} is assumed low enough for the extraction to be performed at the same V_{GS} for all transistors.

The inversion charge Q_i was then computed as

$$Q_i(V_{GS}) \approx \int_{V_{GS}^*}^{V_{GS}} C_{gg,norm} dV$$

thus further assuming:

- (Hyp.5) $Q_i(V_{GS} = V_{GS}^*)$ is negligible
- (Hyp.6) $C_{gge,if}$ is small with respect to C_{ggi} for $V_{GS} > V_{GS}^*$

The effective length was then computed as classically from linear interpolation of $C_{gg,norm}$ in strong inversion and $V_{DS} = 0\,V$

$$C_{gg,norm}(V_{GS} = V_{GS,max}) \approx C_{ggi}(V_{GS} = V_{GS,max}) \approx C_{ox}^{'}(L_g - \Delta L)$$

relying again on (Hyp.1 - 4).

The series resistance R_{SD} was extracted at maximum gate voltage (assuming (Hyp.4)) with the total resistance method, considering

- (Hyp.7) The mobility μ_{eff} is assumed independent of L_{eff}
- (Hyp.8) R_{SD} is extracted as a single value, considering no dependence on V_G.

With the above described steps, the conventional method was seen unable to extract the effective mobility correctly from TCAD simulations of a $L_{mask} = 25\,nm$ FDSOI transistor. This thus motivated the deeper study of its limitations for short devices proposed in this work.

TCAD simulations were used to evaluate the validity of the different assumptions in short transistors. They evidenced the increased impact of underlap-related parasitics neglected by the above approximations, as represented on Fig. 8.1. The main insights from the TCAD simulations were verified qualitatively on 28FDSOI measurements to back up the analysis.

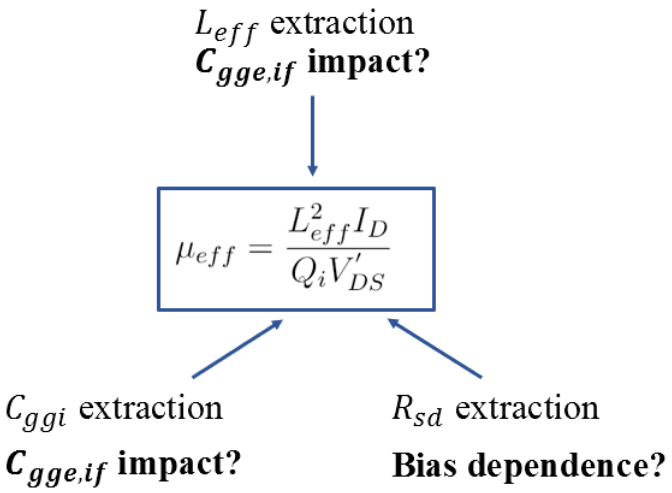

Fig. 8.1: Impact of parasitics on split CV μ_{eff} extraction

One firstly studied the importance of the series access resistance R_{SD}. The total resistance method was used to extract R_{SD} in function of the gate bias from TCAD I-V curves. The excellent linearity of the total resistance R_m against L_{eff} showed that the underlying (Hyp.7) was verified in our TCAD simulations. This was attributed to the absence of neutral defect scattering in the model.

The extracted R_{SD} showed a significant decrease with V_G (by 50% from $V_{ov} = 0.3\,V$ to $V_{ov} = 0.87\,V$), in agreement with previous analyses from FDSOI measurements which had linked this behaviour to the turning on of underlap parasitic access transistors. This dependence with the gate bias was seen to have a major impact on the extracted mobility values and their evolution with V_G, making (Hyp.8) unsuited in short transistors.
While previous articles have discussed the influence of this behaviour on the low-field mobility μ_0 extracted with the Y function, notably showing it generates an erroneous mobility degradation with L_{eff}, this effect has to the author's knowledge up to now been neglected in split CV $\mu_{eff}(V_G)$ extractions.

The important bias dependence of R_{SD} as extracted with the total resistance method was well retrieved from the available 28FDSOI measurements.
The linearity of the total resistance R_m against L_{eff} was not as good as in the TCAD simulations. While this could de attributed to dependence of μ_{eff} on L_{eff}, measurement error and variability are also part of the picture and should be taken into account for quantitative interpretation. Nevertheless, this bias dependence of the access resistance was confirmed to have a major impact on the mobility extracted from the measurements, in good agreement with the observations from TCAD simulations.

The UTSOI compact model offers a parameter to describe the R_{SD} bias dependence in a similar manner as proposed in [11] (note this effect is however neglected by default). Seen the significance of this variation, it would be an interesting continuation of this work to confront this compact model to TCAD simulation and measurements results .

One secondly studied the parasitic contributions to the gate capacitance.
The state of the art of inner fringing capacitance modeling in FDSOI transistors was first reviewed. It was highlighted that in FDSOI (contrary to bulk) the inner fringing capacitance is known not be shielded in accumulation due to the absence of dynamic hole response at usual frequencies. This was verified here by TCAD simulation, and means that (Hyp.3) is not valid in FDSOI. Therefore, the expression of $C_{gg,norm}$ had to be rewritten:

$$\begin{aligned} C_{gg,norm} &= C_{gg}(V_{GS}, L_{eff}) - C_{gg}(V_{GS,min}, L_{eff}) \\ &\approx C_{ggi}(V_{GS}, L_{eff}) + C_{gge,if}(V_{GS}) - \mathbf{C_{gge,if}(V_{GS,min})} \end{aligned}$$

showing the appearance in $C_{gg,norm}$ of an additional inner fringing term in accumulation.

An alternative capacitance extraction method based on linear interpolation of C_{gg} against the gate length has been proposed by Vandermolen et al. and used for split CV mobility extraction from 28FDSOI measurements. This method was assessed in this work, and confirmed able to model C_{gg} with precision (less than 2.5% relative error on C_{gg} values for all considered gate voltages and transistor lengths).
The method proposes a way to discriminate between the different contributions to C_{gg}, with the extracted intrinsic gate and inner fringing capacitances being of particular interest here. The extracted inner fringing capacitance was indeed seen different from zero in accumulation, in agreement with literature and Vandermolen's results.
From TCAD simulation of the device charges, it was further shown that this inner fringing capacitance can be partly linked to gate modulation of the underlap charges.

It was mentioned that a physical charge-based model for the inner fringing was introduced with the UTSOI2.2 compact model to improve its description of short channel capacitances. The results of this work further confirm the importance of this addition. Furthermore, the alternative capacitance extraction method used here could be useful to confront this model both to TCAD and measurements results, and potentially help improve its precision.

One finally studied the impact of this inner fringing capacitance on the mobility extraction. Its contribution to the extracted charge was seen significant in short nodes (10% at $V_{GS} = 0.8\,V$ for $L_{mask} = 25\,nm$), meaning (Hyp.6) cannot be assumed for these devices. The above mentioned alternative capacitance extraction method was confirmed effective to correct for this contribution.

Normalization to the overdrive voltage was performed to fully remove the influence of (Hyp.4) from the extraction. This was seen to have a non-negligible impact on the mobility obtained in short nodes, mainly attributable to the influence on the extracted R_{SD}.

With this full normalization, using the intrinsic gate capacitance from the alternative capacitance extraction method enabled to extract the mobility in good agreement with the TCAD model for all gate lengths (less than 10% deviation from the TCAD implemented mobility in the $0.3 < V_{ov} < 0.87$ range for all transistor lengths). This important outcome thus validates the great interest of this method for capacitance and mobility extraction.

Comparing with results using $C_{gg,norm}$, the contribution of the inner fringing capacitance was thus indicated to be the major remaining cause of mobility underestimation in short transistors (after V_{ov} normalization and bias dependent R_{SD} correction). This has to the author's knowledge not be reported in literature.
Alternatively, performing linear interpolation on the extracted charge was also proposed as a practical way to get rid of parasitic charge contributions and improve the extraction from $C_{gg,norm}$.

These insights on the gate capacitances were evaluated on the 28FDSOI measurements. The threshold voltage V_{TH} extracted from the maximum of dC_{gg}/dV_{GS} was found to increase for gate lengths below $65\,nm$, and the non-linear optimization method was then used instead for the extraction.
The alternative capacitance extraction method was confirmed sucessfull in modeling the measured gate capacitance C_{gg} (less than 2.5% error for all lengths and overdrive voltages). Using this method and correcting for the bias dependent R_{SD}, one finally extracted mobilities with the qualitatively expected values and behaviour.

In summary, the results of this work indicate the importance of the V_{TH} variation with L_g, access resistance bias dependence and inner fringing capacitance contribution to C_{gg} in short transistors. When not properly accounted for, these parasitics can result in underestimation and erroneous behaviour of the mobility extracted by the split CV method in short FDSOI devices. An improved method correcting for these effects was thus proposed and seen able to extract the mobility from TCAD simulations with less than 10% error down to $L_{mask} = 25\,nm$.

In the frame of this work, single measurements on one set of devices were sufficient to retrieve the main tendencies from the TCAD analysis. It should however be stressed that a meaningful quantitative discussion of the experimental results would require repeated measurements on several sets of devices in order to account for measurement error and device variablity.

This preciser information about the method's reliability and expected precision would then enable to compare its results to other extraction procedures as e.g. the Y function method.
One could then also interpret its results in a more quantitative way. Notably, this work hints at the fact that extracted degradation of the apparent mobility with L_{eff}, usually attributed to neutral defect scattering, might be at least partly caused by improper correction of above discussed parasitics (in agreement with results reported for the Y function method).
The improved μ_{eff} extraction could thus result in a more reliable understanding of the mobility degradation phenomena at play in advanced FDSOI nodes, and in turn be beneficial to compact modeling of these technologies.

The presented method is furthermore deemed interesting for characterization of other advanced devices as FinFET's or multiple gate transistors. Indeed, the procedure solely relies on device measurements, and doesn't need any pre-assumed expressions of the inversion charge and mobility dependance on the gate volage. Any bias dependence of the access resistance is also easily taken into account. Furthermore, the method doesn't require precise knowledge of W_{eff}, which might not be known reliably in such devices [22].

It might also be advantageously applicable to other working conditions. The method could for example be suited to study the impact of different back gate biases and conduction by the back channel. Different temperatures (cryogenic, high temperature) could be of interest for specific applications, and also yield better insight on the underlying mobility phenomena [8].

Finally, in a more general way, the approach followed here, i.e leveraging TCAD simulations to assess an extraction procedure at each step, is certainly applicable to other extraction methods. TCAD simulations eliminate potential measurement artifacts and thus enable reliable study of the intrinsic, device-level limitations of the extraction. Comparing their results to the ones from measurements at the different steps might also be helpful to evidence the occurence of measurement issues in the extraction.

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A Appendix

A.1 Additional results from TCAD simulation

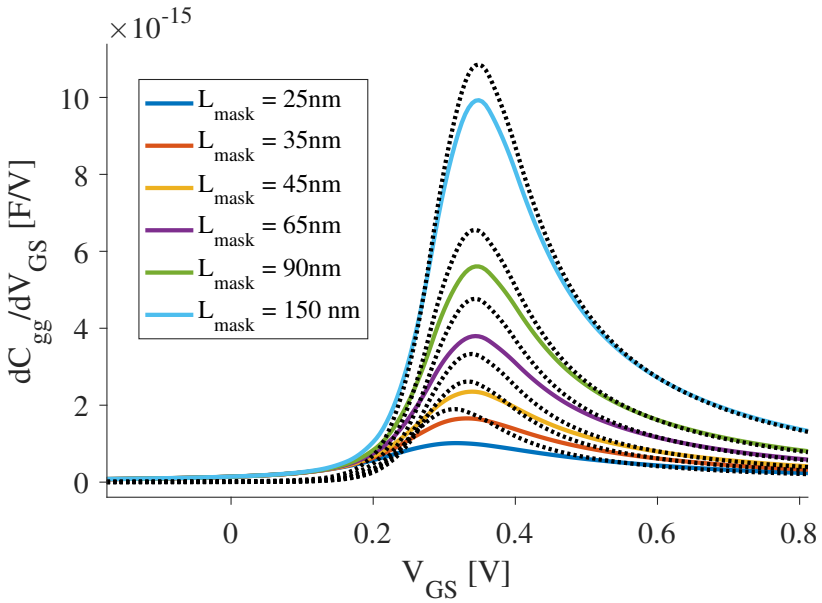

Fig. A.1: Extraction of V_{TH} (TCAD simulation) from dC_{gg}/dV_{GS} (colors) and $d(A_1(V_{GS})L_{eff})/dV_{GS}$ (black points).

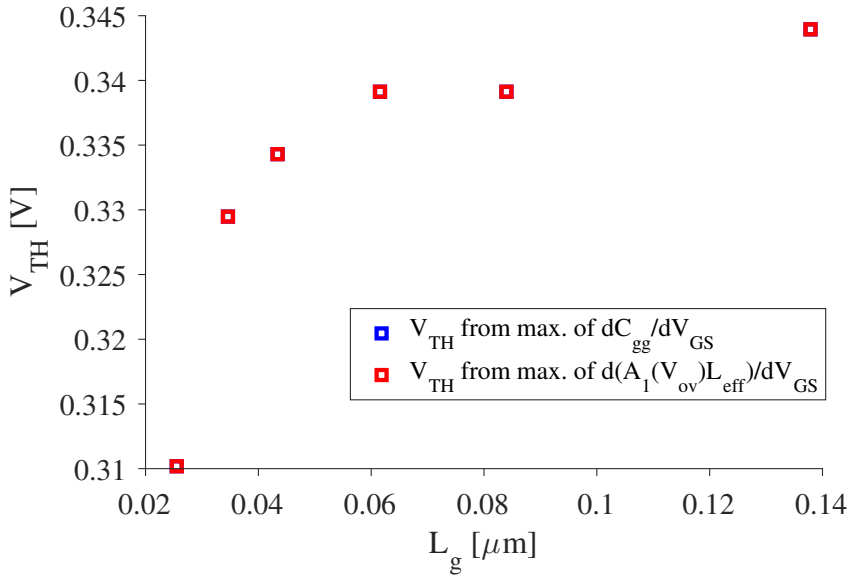

Fig. A.2: V_{TH} extracted from dC_{gg}/dV_{GS} and $d(A_1(V_{GS})L_{eff})/dV_{GS}$. The extracted values are superimposed.

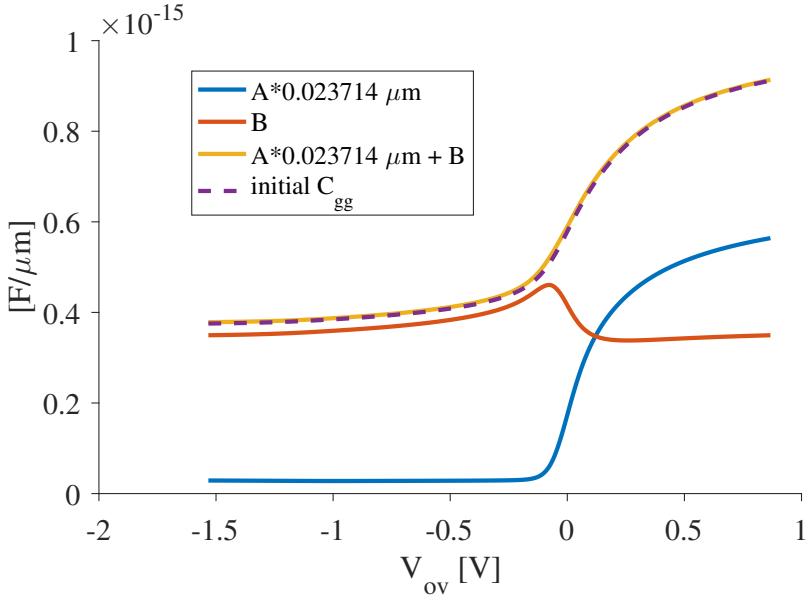

Fig. A.3: Modeling of the gate capacitance C_{gg} by the linear interpolation method (TCAD simulation). The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 25\,nm$

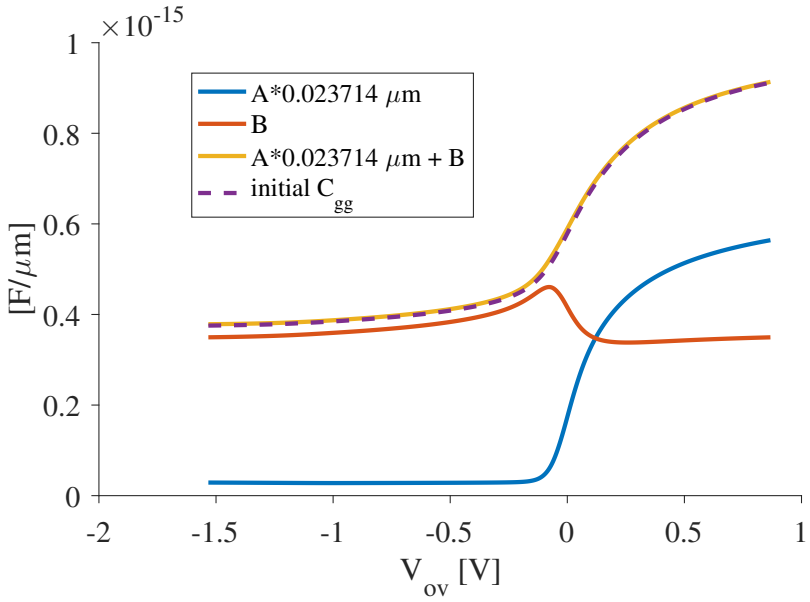

Fig. A.4: Modeling of the gate capacitance C_{gg} by the linear interpolation method (TCAD simulation). The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 25\,nm$

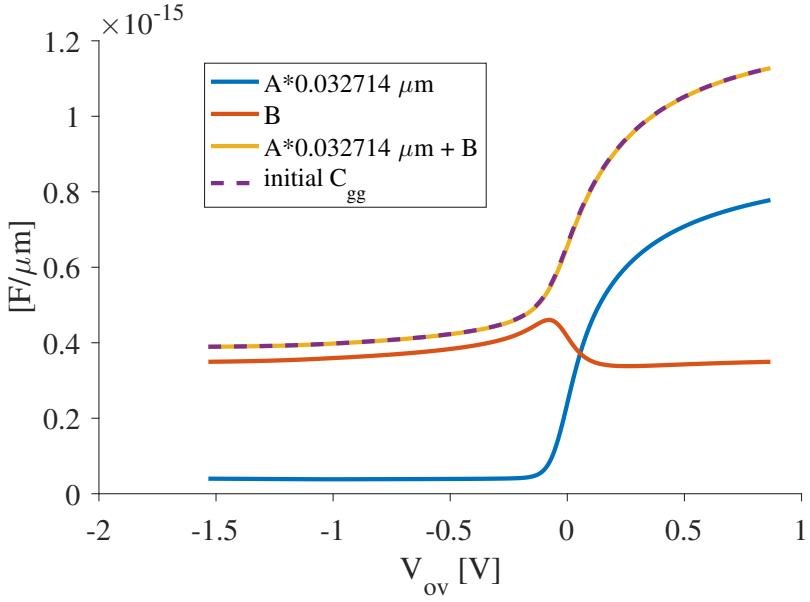

Fig. A.5: Modeling of the gate capacitance C_{gg} by the linear interpolation method (TCAD simulation). The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 35\,nm$

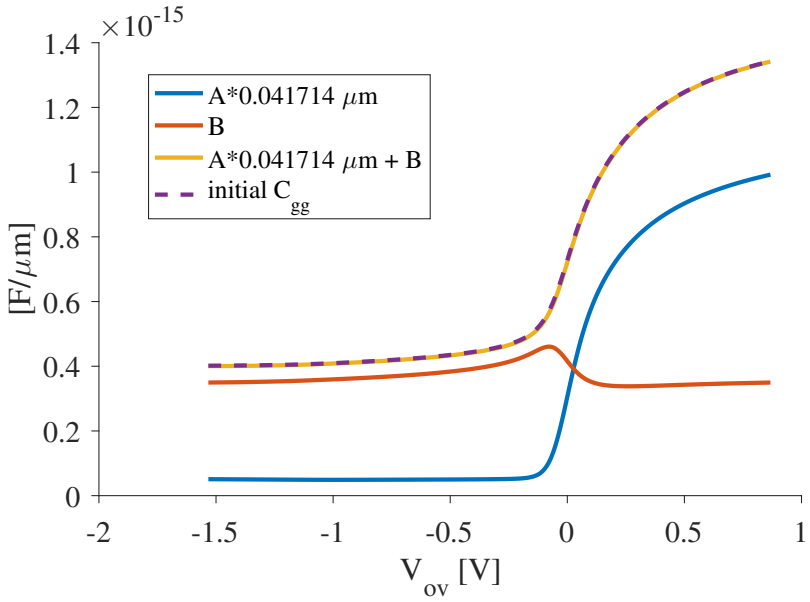

Fig. A.6: Modeling of the gate capacitance C_{gg} by the linear interpolation method (TCAD simulation). The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 45\,nm$

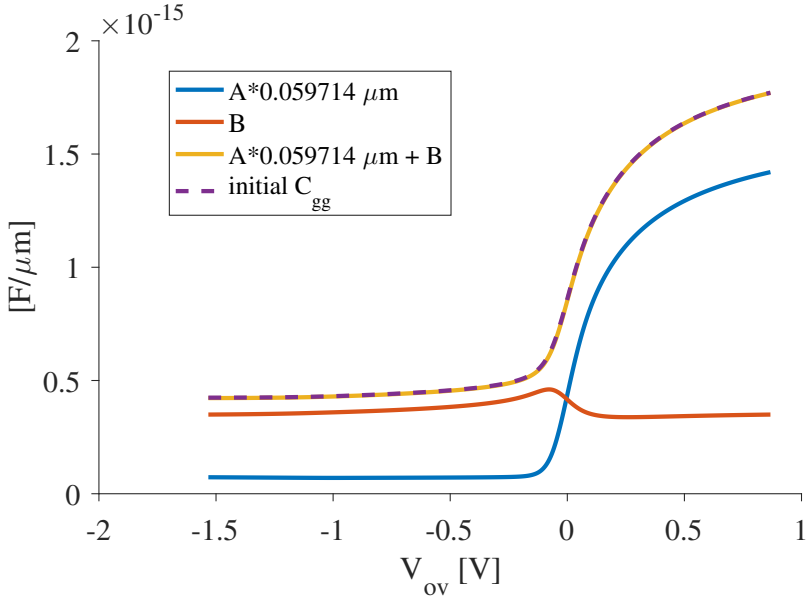

Fig. A.7: Modeling of the gate capacitance C_{gg} by the linear interpolation method (TCAD simulation). The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 65\,nm$

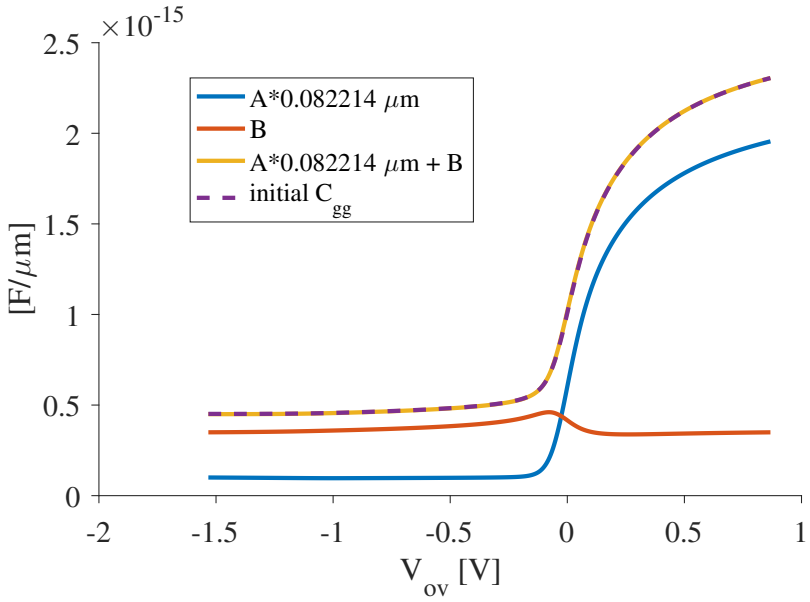

Fig. A.8: Modeling of the gate capacitance C_{gg} by the linear interpolation method (TCAD simulation). The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 90\,nm$

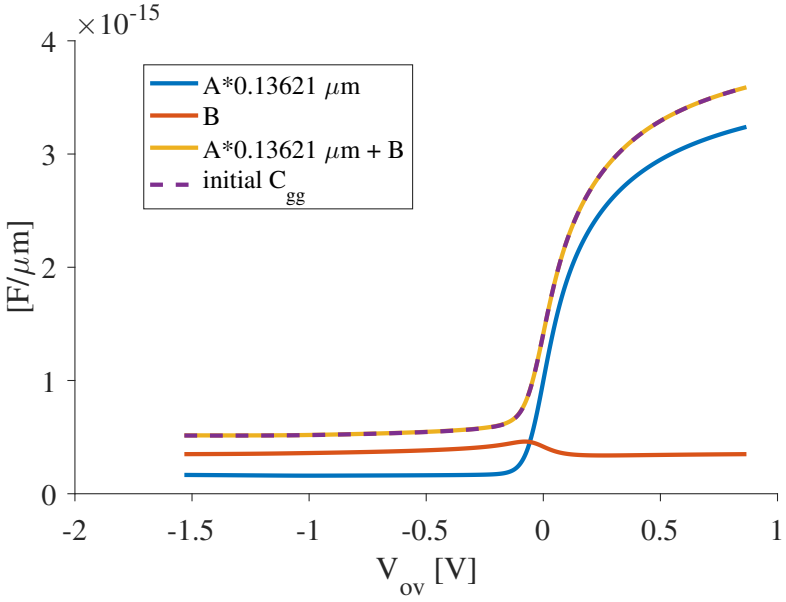

Fig. A.9: Modeling of the gate capacitance C_{gg} by the linear interpolation method (TCAD simulation). The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 150\,nm$

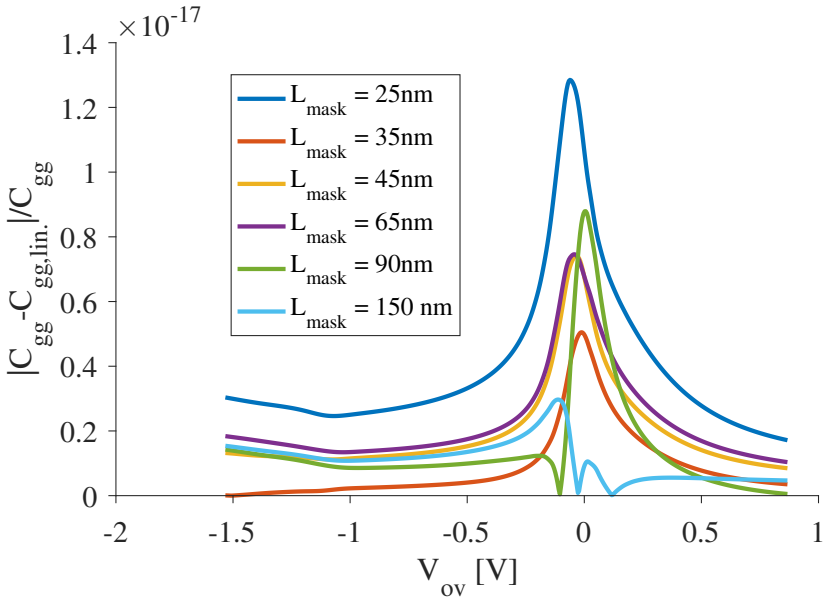

Fig. A.10: Relative error between the total gate capacitance C_{gg} from TCAD and its reconstruction by the linear interpolation method $C_{gg,lin}$

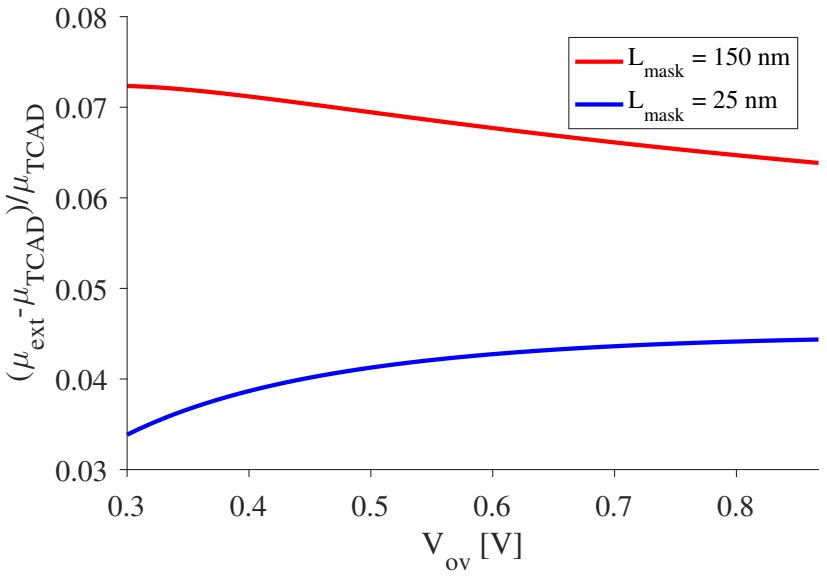

Fig. A.11: Relative error between μ_{ext} from the split CV method (using V_{ov} normalization, $R_{SD}(V_{ov})$ correction and integration of $A_1 L_{eff}$) and $\mu_{TCAD} = 150\,cm^2/Vs$ implemented in the simple TCAD model.

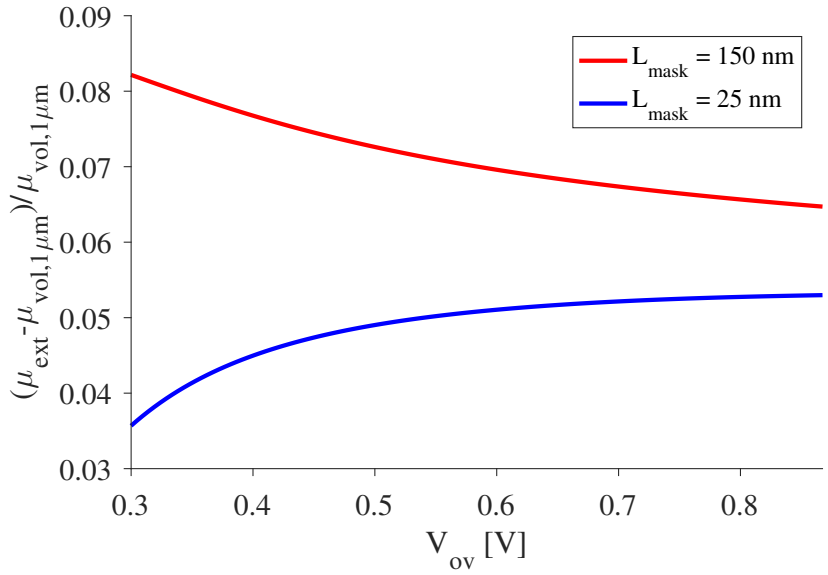

Fig. A.12: Relative error between μ_{ext} from the split CV method (using V_{ov} normalization, $R_{SD}(V_{ov})$ correction and integration of $A_1 L_{eff}$) and μ_{vol} from a $L_g = 1\,\mu m$ transistor with the full TCAD model.

A.2 Additional measurement results

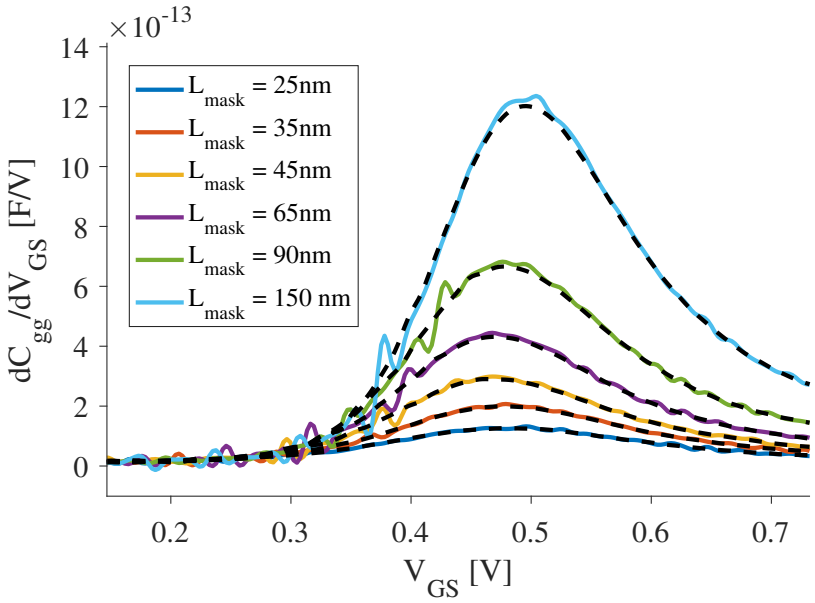

Fig. A.13: Difficulty of V_{TH} extraction from the maximum of dC_{gg}/dV_{GS} (measurements). C_{gg} was spline interpolated to 500 points between $V_{GS} = -0.2\,V$ and $V_{GS} = 1.2\,V$. A moving average filter of length 20 was then used to smooth dC_{gg}/dV_{GS}. Colors show dC_{gg}/dV_{GS} for the different lengths, black dashed the result after smoothing.

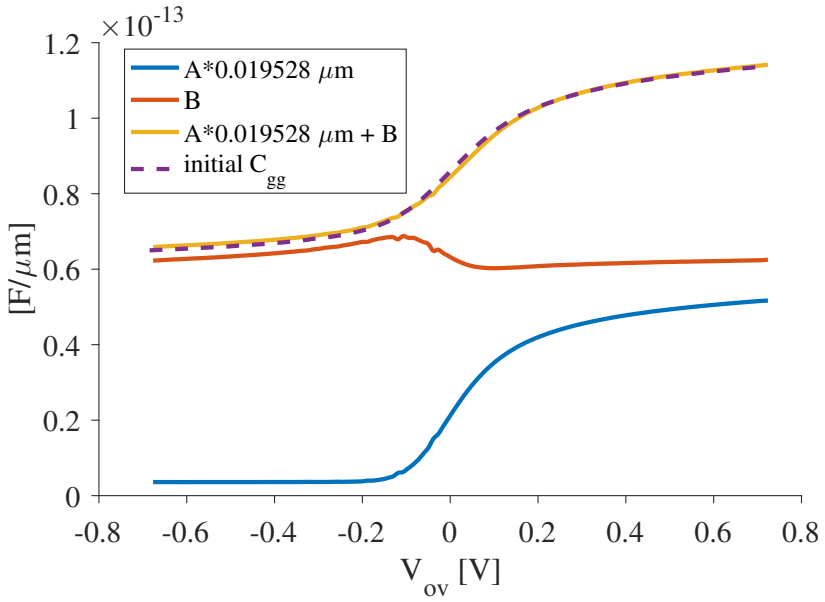

Fig. A.14: Modeling of the total gate capacitance C_{gg} (from measurements) by the linear interpolation method. The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 25\,nm$

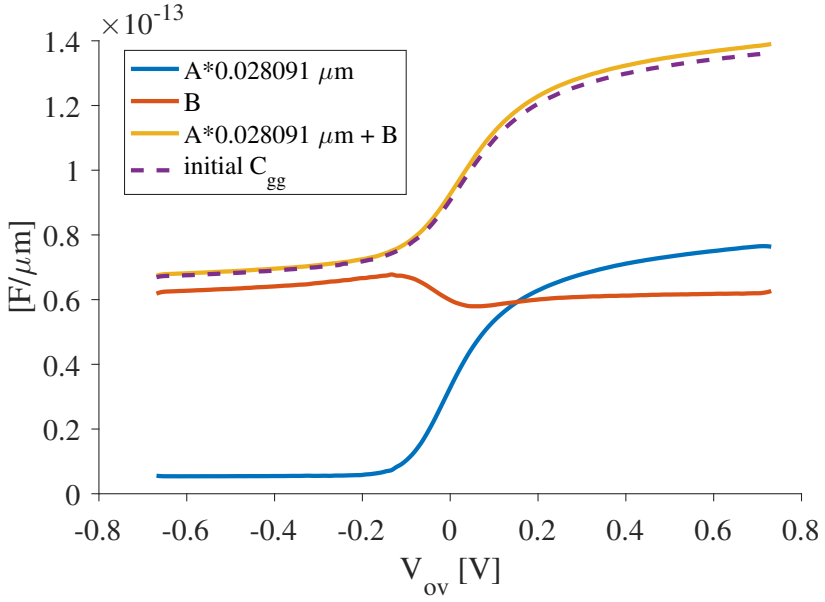

Fig. A.15: Modeling of the total gate capacitance C_{gg} (from measurements) by the linear interpolation method. The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 30\,nm$

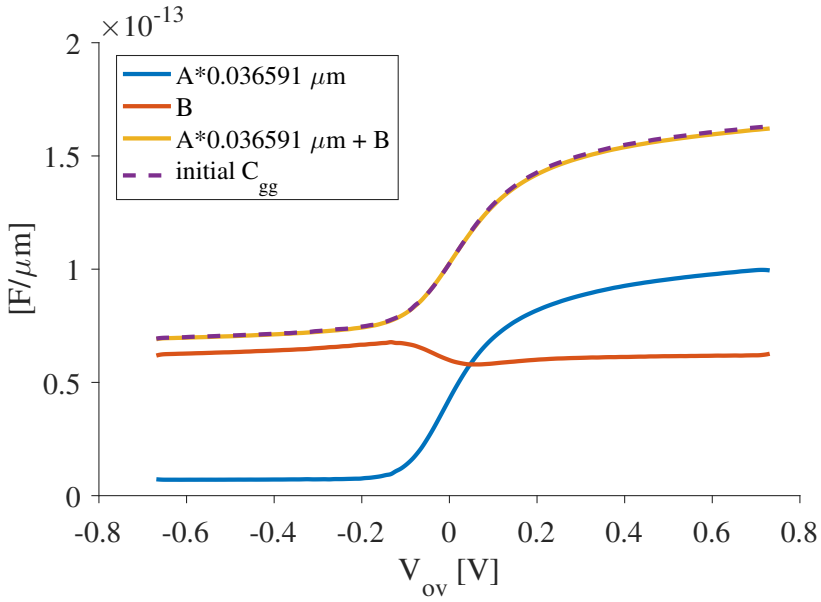

Fig. A.16: Modeling of the total gate capacitance C_{gg} (from measurements) by the linear interpolation method. The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 45\,nm$

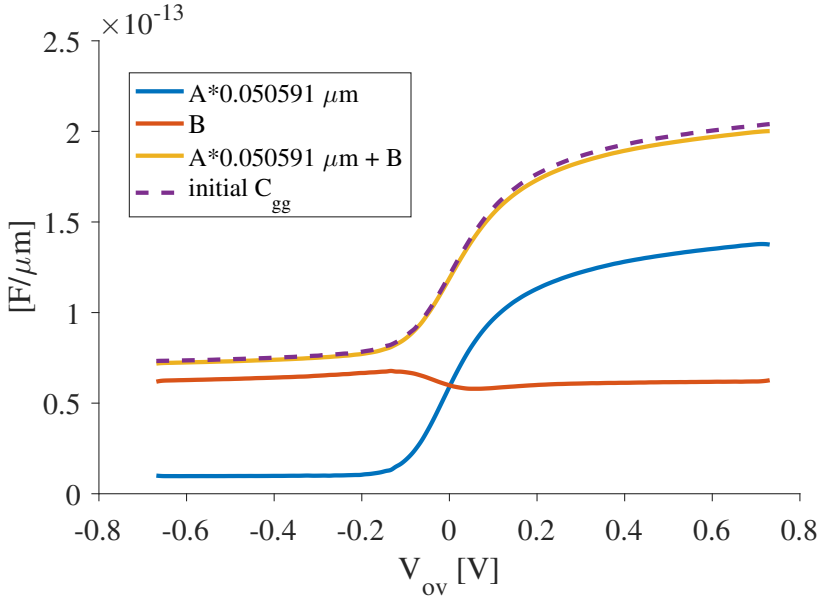

Fig. A.17: Modeling of the total gate capacitance C_{gg} (from measurements) by the linear interpolation method. The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 65\,nm$

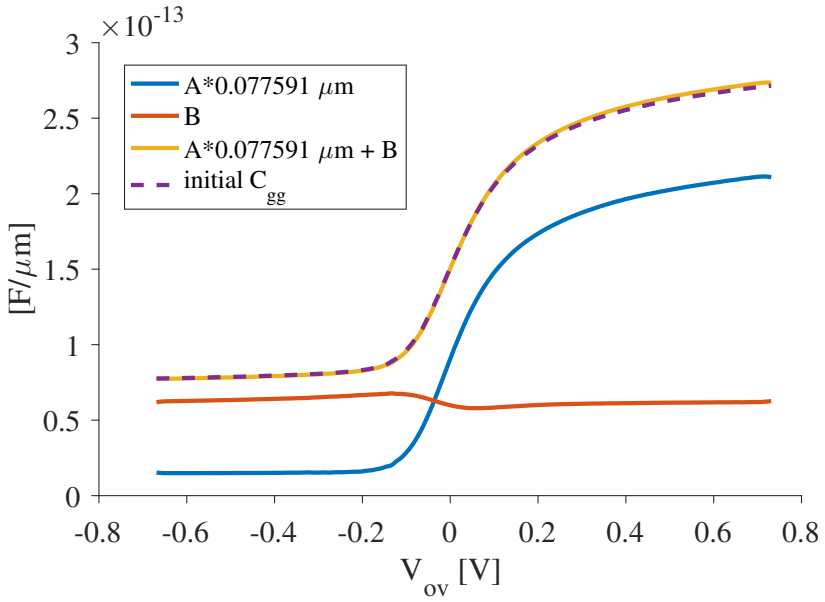

Fig. A.18: Modeling of the total gate capacitance C_{gg} (from measurements) by the linear interpolation method. The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 90\,nm$

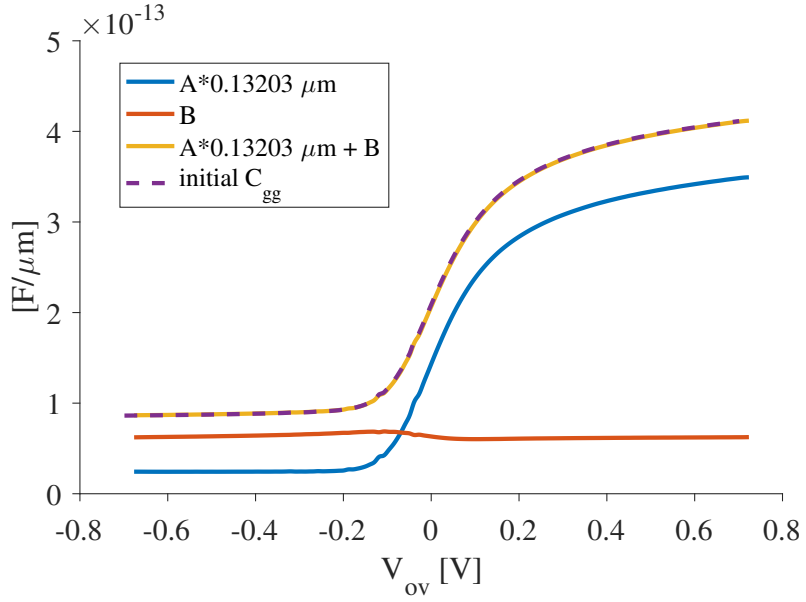

Fig. A.19: Modeling of the total gate capacitance C_{gg} (from measurements) by the linear interpolation method. The inital gate capacitance (dashed purple curve) is well reconstructed from the A and B terms (yellow). $L_{mask} = 150\,nm$

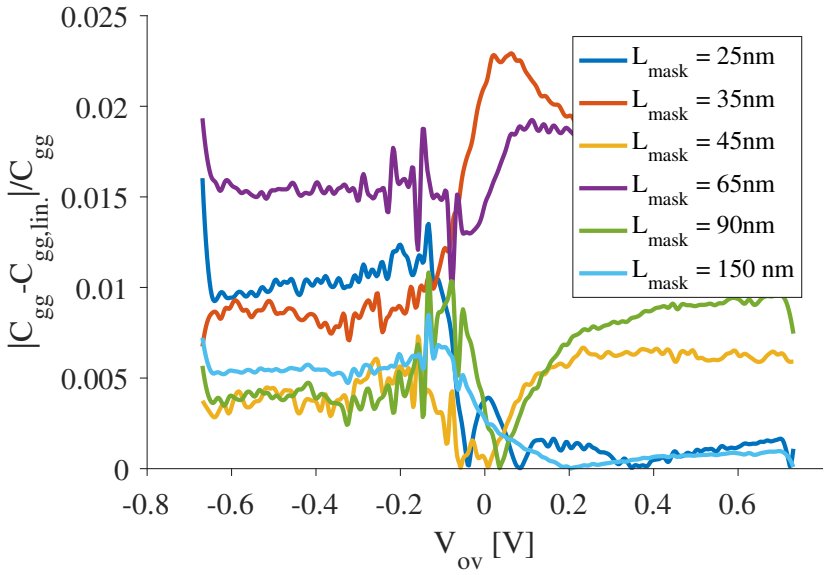

Fig. A.20: Relative error between the measured total gate capacitance C_{gg} and its reconstruction by the linear interpolation method $C_{gg,lin} = A1L_{eff}$

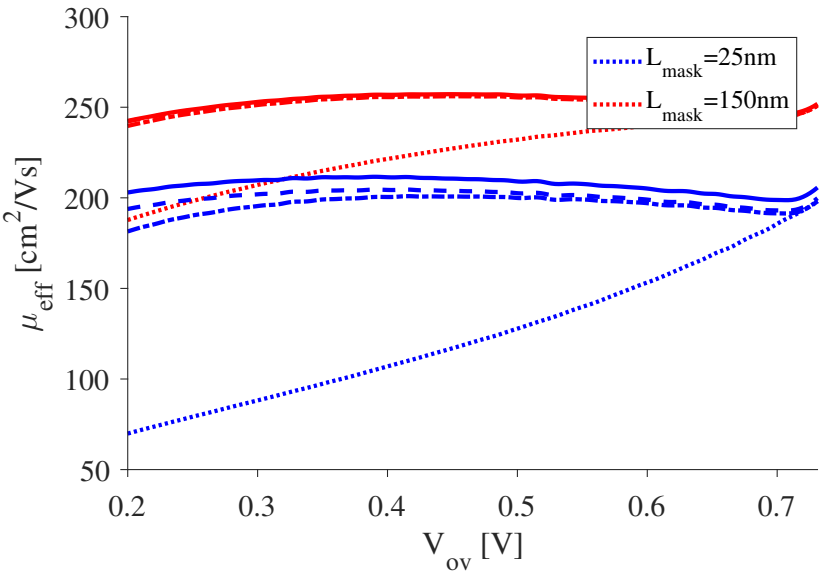

Fig. A.21: Split CV extracted mobility from measurements, V_{TH} extracted from the non-linear optimization method. Dots: $C_{gg,norm}$, constant R_{SD}. Dash-dot: $C_{gg,norm}$, $R_{SD}(V_{ov})$, Dashed: $C_{gg,norm}$, $R_{SD}(V_{ov})$, Q_{par} correction, Full: A_1L_{eff}, $R_{SD}(V_{ov})$

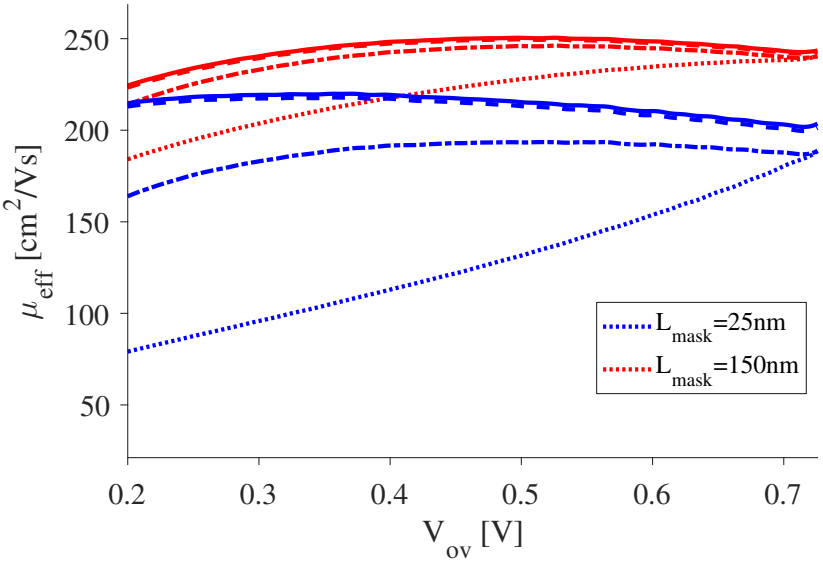

Fig. A.22: Split CV extracted mobility from measurements, V_{TH} extracted from the maximum of dC_{gg}/dV_{GS}. Dots: $C_{gg,norm}$, constant R_{SD}. Dash-dot: $C_{gg,norm}$, $R_{SD}(V_{ov})$, Dashed: $C_{gg,norm}$, $R_{SD}(V_{ov})$, Q_{par} correction, Full: $A_1 L_{eff}$, $R_{SD}(V_{ov})$

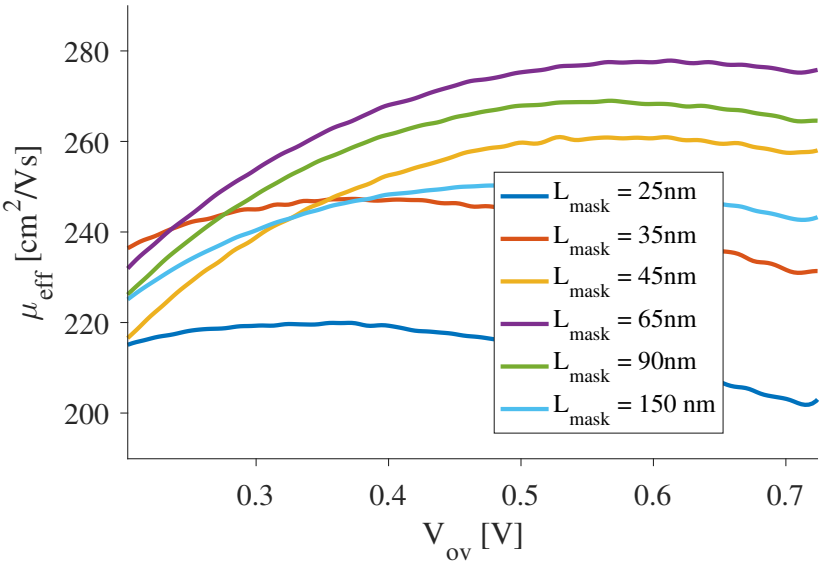

Fig. A.23: μ_{eff} extracted from measurements with $A_1 L_{eff}$, $R_{SD}(V_{ov})$, , V_{TH} extracted from the maximum of dC_{gg}/dV_{GS}

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École polytechnique de Louvain
Rue Archimède, 1 bte L6.11.01, 1348 Louvain-la-Neuve, Belgique | **www.uclouvain.be/epl**