

École polytechnique de Louvain

Porous Silicon Integration in Bulk CMOS with a Post-Process Approach for RF Performance Enhancement

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Abstract

Bulk CMOS technologies remain attractive for RF and millimeter-wave integrated circuits because of their low cost, maturity, and compatibility with large-scale integration. However, standard-resistivity silicon substrates introduce RF losses, capacitive coupling, and substrate-induced parasitics. Porous silicon (PSi) is a promising substrate-engineering solution because of its high effective resistivity and low effective permittivity. With a back-side post-process approach, PSi can be formed after front-end fabrication and locally introduced below RF structures. While this strategy has been demonstrated on SOI substrates, its transfer to bulk CMOS requires a reliable stopping mechanism to prevent the porous front from reaching the front-side devices.

This thesis investigates the use of P- and N-doped regions as a bulk-compatible etch-stop strategy for post-process PSi integration. The proposed approach relies on the reduced porosification of N-type regions and on the depletion regions formed at PN junctions. Experimental observations from porosified PN etch-stop layer candidates show that these patterns can influence the porous front, but also reveal significant non-uniformity along the porous pocket.

To interpret these effects, two-dimensional and three-dimensional COMSOL models are developed. The 2D simulations isolate the effect of local resistivity profiles and show that PN patterns can slow down the porous front. The 3D simulations demonstrate that the finite length of the back-side opening and the metallic grid geometry can induce longitudinal non-uniformity. Modified electrode geometries are therefore proposed to reduce this effect and improve the uniformity of the residual silicon thickness.

Overall, this work shows that P- and N-doped regions are a plausible route toward bulk-compatible post-process PSi integration. However, the final morphology results from a coupling between etch-stop layer design and three-dimensional layout geometry. Further work is required to refine the electrochemical model and experimentally validate optimized doping and grid geometries.

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Chapter 1

Introduction

Complementary Metal-Oxide-Semiconductor (CMOS) technology built on bulk silicon substrates has been a cornerstone of microelectronics for several decades. Its widespread adoption comes from its mature fabrication process, low cost, high yield, and compatibility with large-scale industrial production (Laurent and Desbonnets 2011). However, when the same technology is used for radio-frequency (RF) and millimeter-wave circuits, the silicon substrate itself can become a limiting factor.

The main difficulty comes from the electrical properties of conventional bulk silicon. Standard-resistivity silicon substrates, typically in the range of a few to a few tens of Ωcm , are not sufficiently insulating at radio-frequencies (Eminente *et al.* 2004; Raskin 2009; Rack 2021).

Several substrate engineering strategies have been developed to overcome these limitations. High-resistivity silicon substrates reduce conduction losses by increasing the bulk resistivity. Silicon-On-Insulator (SOI) technologies further improve substrate isolation by introducing a buried oxide (BOX) layer between the active silicon film and the substrate. These solutions have become reference platforms for high-performance RF applications. However, they rely on dedicated starting substrates and are therefore more expensive than standard bulk silicon as they require specific process flows.

In this context, porous silicon (PSi) is an attractive candidate for improving RF performance while preserving the cost advantage of bulk substrates. Depending on several factors, PSi can exhibit a lower effective permittivity than bulk silicon, which reduces capacitive coupling, and a much higher effective resistivity, which reduces substrate losses (Aroutiounian and Ghulinyan 2003). These properties make PSi a promising material for RF substrates.

Despite these advantages, integrating PSi into a CMOS process is not straightforward. If PSi is introduced before front-end fabrication, it must withstand the subsequent thermal and mechanical steps of the CMOS process. This is problematic because PSi is mechanically weaker than bulk silicon, has a different coefficient of thermal expansion, and its porous morphology can be incompatible with standard CMOS processes (Tuyaerts *et al.* 2026; Gautier and Leduc

2014; Capelle *et al.* 2012). These integration issues have limited the use of PSi in industrial CMOS technologies, even though its RF benefits have been known for many years (Welty *et al.* 1998; Sarafis *et al.* 2013).

A more promising strategy, developed by Scheen, Tuyaerts, Rack, *et al.* (2020), consists of introducing PSi after device fabrication, using a back-side post-process approach. In this case, the front-end devices and RF structures are fabricated first, using a conventional process flow. The silicon substrate is then porosified locally from the back-side of the wafer, only below the RF-active regions. Since PSi is introduced at the end of the process, it does not undergo the full CMOS thermal cycle and does not interfere with the fabrication of the front-end devices. This approach has recently been demonstrated on SOI substrates, where the buried oxide and the polysilicon beneath it provide a natural stopping structure for the porosification front (Tuyaerts *et al.* 2026).

Transferring this post-process integration strategy to bulk CMOS is more challenging. In a bulk substrate, the silicon is continuous from the back-side to the front-side active region. Therefore, if back-side porosification is performed without a stopping mechanism, the porous front can either stop too far from the RF structures, leaving a lossy silicon layer, or propagate too far and damage the front-side devices. A bulk-compatible etch-stop strategy is therefore required. Ideally, this strategy should not rely on the addition of a new buried layer, since this would reduce compatibility with standard bulk CMOS. Instead, it should exploit structures that already exist or can be naturally integrated in a CMOS process.

This thesis investigates the use of P- and N-doped regions as a potential stopping layer for post-process PSi integration in bulk CMOS. This solution is attractive from an integration point of view, since transistor wells, schematically shown in Figure 1.1, could potentially be used for the stopping layer. The proposed approach is based on the electrical behavior of PN junctions and on the selectivity of silicon porosification with respect to doping type. By arranging P- and N-doped regions into periodic patterns, the porous front may be slowed down or locally stopped before reaching the front-side devices.

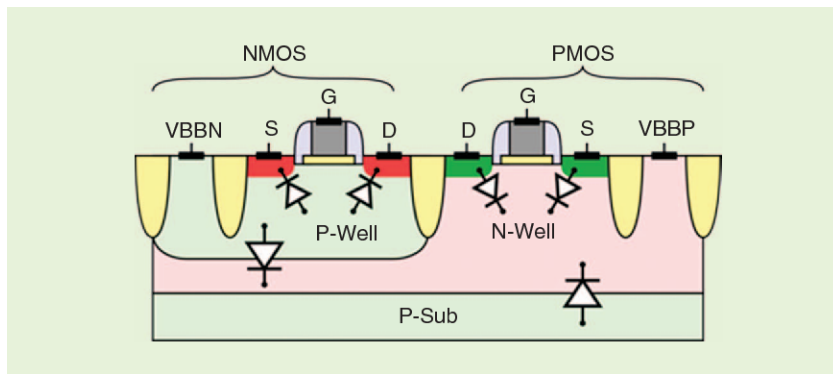


Fig 1.1. Schematic cross-section of CMOS transistors in a bulk technology, from Cathelin (2017).

The objective of this work is to study the impact of the PN doping parameters and of the porosi-

porosification setup geometry through a combination of experimental observations and numerical simulations. The experimental results considered in this work are part of Thibault Fiasse's PhD thesis. These results provide information on the morphology of the porous pockets, the penetration of PSi between the P-type and N-type regions, and the RF response of the resulting substrates. Based on these observations, some porosification non-uniformities are identified and numerical simulations are therefore developed to replicate and interpret these effects. The ultimate goal of the thesis is to propose solutions to mitigate these effects and therefore improve the reliability of the porosification process.

This thesis is structured as follows. Chapter 2 provides the relevant state of the art. It first introduces the RF figures of merit used to characterize substrates, then describes the formation and properties of porous silicon, and finally discusses previous work on PSi post-process integration. Chapter 3 introduces the PN etch-stop layer concept. The physical mechanisms expected to slow down the porous front are described and representative PN implantation candidates are compared through simulated resistivity maps. Chapter 4 presents the experimental implementation of these candidates in three-dimensional layouts. The porosified samples are analyzed using cross-sectional and top-view observations, as well as RF measurements on CPW structures. Chapter 5 then introduces the two-dimensional COMSOL model developed to study the local effect of the PN resistivity profiles on the moving porous front. Finally, Chapter 6 extends the numerical analysis to three dimensions in order to investigate the geometry-induced non-uniformity effects observed experimentally. The main conclusions and perspectives of this work are summarized in Chapter 7.

Chapter 2

State of the art

This chapter will present all the theoretical concepts and technological background needed to understand the context of this work. First, in Section 2.1, the notions relatives to the substrate role in RF will be discussed and the figures of merit used to evaluate substrate performances will be introduced. Then, the porous silicon fabrication process and the main properties that make it attractive for RF circuits will be introduced in Section 2.2. Finally, Section 2.3 will review previous work on the development of the post-process integration of PSi and highlight the remaining challenges addressed in this thesis.

2.1 RF modeling of the substrate

2.1.1 Why the substrate matters at RF frequencies

In RF integrated circuits, signals propagate through conductive metal lines patterned on top of an insulator-semiconductor stack. Unlike in lower frequency circuits, where the substrate acts merely as a mechanical support and its electrical properties are largely irrelevant to circuit function, the substrate plays a critical and active role at RF and millimeter-wave frequencies. This fundamental difference arises because the electromagnetic fields associated with propagating RF signals are not confined to the metal conductors alone. They penetrate all surrounding materials, including the underlying substrate Rack (2021) and Sarafis *et al.* (2013).

The RF performance can be characterized by the insertion losses, which are caused by two main mechanism. The first one is ohmic loss in the metal conductors, due to their finite conductivity. The second one is substrate loss: RF fields penetrating into a conductive substrate induce currents that dissipate energy by Joule heating. As a result, the electrical properties of the substrate directly affect the propagation of RF signals. Standard bulk CMOS silicon, with typical resistivities of a few to a few tens of Ωcm , is therefore a lossy medium for RF propagation. The dielectric permittivity of the substrate also matters. A high relative permittivity

increases capacitive loading and modifies the characteristic impedance of transmission lines. It also promotes parasitic coupling between neighboring devices and signal lines, which is detrimental in mixed-signal systems-on-chip. For these reasons, an ideal RF substrate should combine high resistivity, to suppress conduction losses and crosstalk, with low permittivity, to reduce capacitive coupling (Rack 2021; Sarafis *et al.* 2013; Nabet 2025).

2.1.2 Figures of merit for RF substrates

To compare substrates on a fair and reproducible basis, the RF engineering community has adopted two substrate Figures of Merit (FoMs): the effective resistivity ρ_{eff} and the effective relative permittivity $\epsilon_{r,\text{eff}}$. These are defined as the homogenized electrical parameters of an equivalent uniform material such that a coplanar waveguide (CPW) line implemented on this equivalent material produces exactly the same S-parameters as an identical CPW line implemented on the real, non-uniform substrate (Rack 2021; Lederer and Raskin 2005). This equivalence is necessary because the substrate beneath an integrated circuit is in general not electrically uniform: it is a heterostructure composed of several layers with different electrical properties. Even within a single semiconductor layer, the resistivity is not spatially uniform, as it depends on local doping, interface charge effects, and band-bending phenomena.

Together, these two quantities are central for evaluating whether PSi actually improves the RF environment below CPW structures. Since PSi and crystalline silicon have very different electrical properties, the extracted effective parameters depend on how much of the RF field interacts with each material. Porosification is therefore most beneficial when the porous region extends into the part of the substrate exposed to the CPW fields. In practice, a closer and more complete porous pocket increases the contribution of PSi to ρ_{eff} and $\epsilon_{r,\text{eff}}$, while a remaining crystalline silicon layer next to the CPW limits the RF benefit.

2.2 Porous Silicon

This section introduces the main physical and technological concepts related to porous silicon (PSi). It first recalls how PSi is formed by electrochemical anodization, then discusses the electrochemical regimes involved in silicon dissolution, the classification of porous layers, the main process parameters, and the current-distribution models used to describe electrochemical etching. The section finally summarizes the electrical properties that make PSi attractive for RF technologies.

The section is mostly inspired by Sailor (2012). Section 2.2.5 is mostly based on Scheen (2015) and Section 2.2.6 is mostly based on Ivanov (2018).

2.2.1 History of porous silicon

Porous silicon was discovered in 1956 by the Uhlirs in the Bell laboratories. They were trying to find techniques to electrochemically etch silicon. However, they accidentally observed that, under the appropriate electrochemical conditions, holes appeared in the silicon substrates following the $\langle 100 \rangle$ crystal orientation instead of a uniform dissolution. As no practical application was identified at the time, the discovery was not exploited and the research on porous silicon remained very limited for the following decades. The interest came back in the 1980s, when the high surface area of the material was exploited for applications in sensors and photonics. However, the most significant rise in interest came in the 1990s, following the discovery that the material exhibits photoluminescence at room temperature. This discovery opened up new possibilities for the use of porous silicon in optoelectronic and biomedicine.

Since then, the fabrication process has been improved and nowadays, porous silicon is used in a wide range of applications including membranes, drug delivery systems, and RF isolation layers (Welty *et al.* 1998; Vercauteren *et al.* 2021).

2.2.2 Fabrication of PSi

PSi can be obtained using several families of processes. Dry etching techniques can be used when highly directional structures are required, while wet electrochemical approaches are generally used to form porous layers over larger areas. Among wet processes, stain etching relies on spontaneous chemical oxidation and dissolution of silicon, sometimes assisted by a catalyst (Scheen 2015). The process of interest in this work is anodization, another wet process, where silicon dissolution is driven by an externally imposed current.

During anodization, the silicon wafer is placed in an electrochemical cell and brought into contact with an electrolyte, usually based on hydrofluoric acid (HF). The silicon acts as the anode, where oxidation and dissolution occur, while a counter-electrode closes the electrical circuit. The electrolyte is commonly composed of HF diluted in water, often with an additional wetting agent such as ethanol or isopropanol (IPA). The wetting agent lowers the surface tension of the solution and therefore improves the penetration of the electrolyte into the pores.

Two-electrode and three-electrode cells can be used. In a two-electrode configuration, the silicon wafer is the working electrode and the cathode is the counter-electrode. A current is imposed between both electrodes, as schematically shown in Figure 2.1. The counter-electrode is typically made of an inert material such as platinum, so that it does not dissolve in the electrolyte. In a three-electrode configuration, an additional high-impedance reference electrode is introduced. This allows to control the current and the potential of the concentration at the same time, which is useful for detailed electrochemical studies.

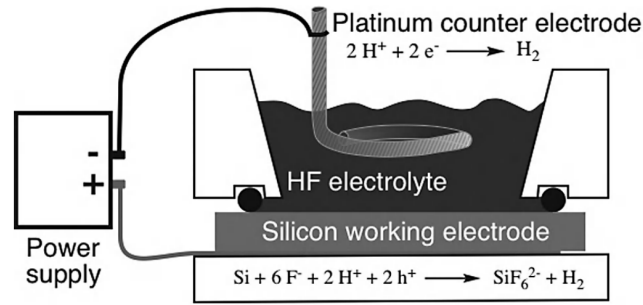


Fig 2.1. Schematic of a two-electrode electrochemical cell used for silicon anodization, adapted from Sailor (2012).

2.2.3 Electrochemistry of silicon dissolution

Silicon porosification is an electrochemical process. In an HF bath, crystalline silicon is not spontaneously dissolved under normal conditions because its surface is passivated by Si–H bonds. During anodization, holes are supplied to the silicon/electrolyte interface. These holes weaken the Si–H bonds, allowing fluorine species to form Si–F bonds. The subsequent breaking of Si–Si bonds leads to the release of soluble fluorosilicate species and to the formation of pores (Scheen 2015). The main steps of the microscopic reaction mechanism are illustrated in Figure 2.2.

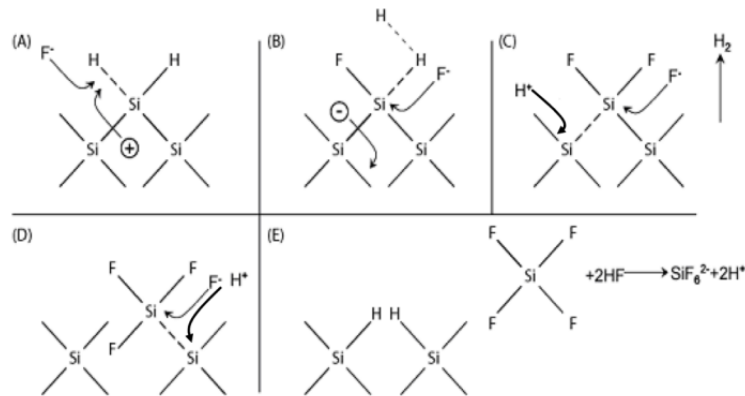
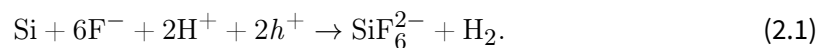


Fig 2.2. Schematic mechanism of PSi formation in hydrofluoric acid, adapted from Scheen (2015).

The porous-formation regime is commonly associated with a two-electron dissolution reaction:



In this regime, the supply of holes is localized at the pore tips. The pore walls remain mostly passivated by Si–H bonds, which favors the progression of pores into the silicon rather than uniform dissolution of the entire surface.

The electrical field and the band bending along the pore walls create a space-charge region (SCR) along the silicon/electrolyte interface. The SCR is thinner near the pore tips, where

the electric field is stronger. Holes can therefore more easily reach the pore tips than the pore walls, which promotes directional pore growth. When the current density is increased, more holes become available at the surface and lateral dissolution of the pore walls becomes more significant. Above a critical current density, the holes are so abundant that the surface dissolves uniformly. This corresponds to the electropolishing regime, generally associated with a four-electron reaction:

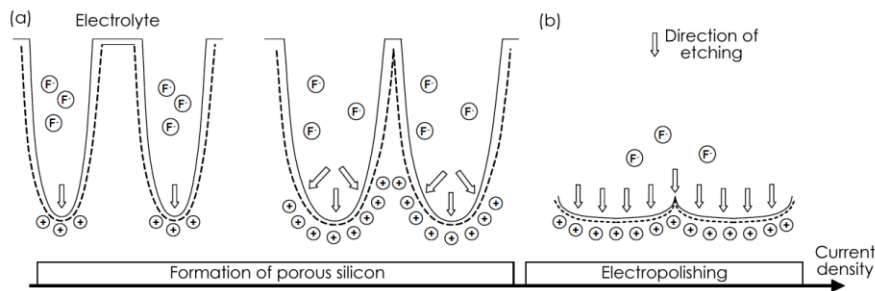


Fig 2.3. Transition from PSi formation to electropolishing as the current density is increased, adapted from Scheen (2015).

A typical current-voltage curve for silicon anodization is shown in Figure 2.4. The porous-formation and electropolishing regimes are separated by a transition region. For the context of this work, the process must remain in the PSi formation regime.

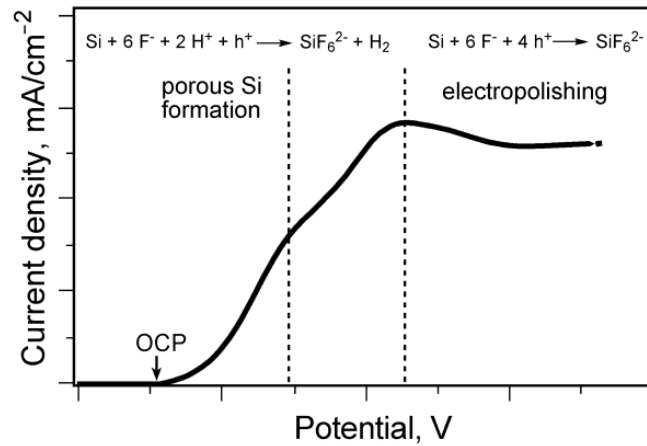


Fig 2.4. Typical current-voltage curve for silicon anodization, showing the porous-formation regime, the transition region and the electropolishing regime, adapted from Sailor (2012).

2.2.4 PSi classification

PSi can have different mechanical, optical, and electrical properties, depending on the pores geometry and on the porosity of the layer.

The pores are classified depending on their width:

1. **Micropores** have widths smaller than 2nm
2. **Mesopores** have widths between 2nm and 50nm
3. **Macropores** have widths larger than 50nm

Another important parameter is the porosity, defined as the ratio between the pore volume and the apparent volume of the porous layer.

1. The **open porosity** is the volume of pores accessible to a given probe molecule
2. The **closed porosity** is the volume of inaccessible pores
3. The **total porosity** is the addition of both porosities

In the case of electrochemically formed porous silicon, all pores are formed by contact with the electrolyte during formation. As a result, there is no closed porosity in anodized PSi.

2.2.5 Influence of process parameters

Several parameters influence the etching rate, pore diameter, pore orientation, and final porosity of the silicon layer. On the wafer side, the crystal orientation, doping type, and doping concentration are key parameters. On the electrochemical cell side, the electrolyte composition and the applied current density strongly affect the resulting morphology.

Doping type is particularly important for this work, because PN regions are investigated as possible stopping structures. As presented before, anodic dissolution of silicon requires holes at the silicon/electrolyte interface. In P-type silicon, holes are majority carriers and can be supplied more easily to the surface, which favors porosification. In N-type silicon, holes are minority carriers. In the dark, the hole supply is therefore strongly limited, and the porosification rate is much lower. Illumination can partially overcome this limitation by generating electron-hole pairs, but this is not the operating condition considered in this thesis.

Doping concentration also affects the space-charge region at the silicon/electrolyte interface. Increasing the doping concentration has two effects. First, for P-type substrates, it increases the number of holes and so it increases the porosification. Second, it reduces the SCR width and modifies the ability of holes to reach the pore walls. As a result, in heavily P-doped silicon, holes can reach a larger fraction of the surface, which tends to promote lateral dissolution and larger pore diameters. In contrast, lower doping or reduced hole availability favors more localized dissolution at the pore tips.

The applied current density determines the electrochemical regime, as shown in Figure 2.3 and Figure 2.4. At low current density, the porosification regime dominates and the pore

walls remain passivated. Increasing the current density increases the flux of holes toward the interface and usually increases both pore diameter and porosity. If the current density becomes too high, the process can enter the electropolishing regime, where the surface is dissolved uniformly instead of forming a porous network.

The electrolyte composition affects both the reaction kinetics and the transport of reactive species. HF provides the fluorine species required for silicon dissolution. The addition of ethanol or IPA improves wetting and facilitates the penetration of the electrolyte into the pores. This improves the renewal of reactive species at the pore front and helps maintain a more homogeneous porosification.

Finally, the pores can preferentially grow along the $\langle 100 \rangle$ and $\langle 113 \rangle$ crystallographic directions. Depending on the substrate orientation, pores can therefore appear vertical or inclined. This anisotropy is particularly present when the porosification is limited by the current. If the hole supply is sufficient, the porosification will take place in several directions and the whole porous region will appear isotropic at the macroscopic scale.

2.2.6 Current-distribution models

Electrochemical systems can be modeled at different levels of complexity depending on which physical limitations are considered. This distinction is important because the COMSOL models developed later in this thesis rely on a primary current distribution formulation. (Ivanov 2018)

The **primary current distribution** only accounts for ohmic conduction in the electrolyte and in the electrode. Concentration gradients in the electrolyte and activation overpotential are neglected. The current density is therefore obtained from Ohm's law:

$$\mathbf{i}_l = -\sigma_l \nabla \phi_l, \quad \nabla \cdot \mathbf{i}_l = 0, \quad (2.3)$$

$$\mathbf{i}_s = -\sigma_s \nabla \phi_s, \quad \nabla \cdot \mathbf{i}_s = 0, \quad (2.4)$$

where σ_l and σ_s are the electrolyte and silicon conductivities, while ϕ_l and ϕ_s are the electrolyte and silicon potentials. This approximation is suitable when the reaction is limited by the current value.

The **secondary current distribution** still neglects concentration gradients in the electrolyte but includes electrode kinetics through the interfacial overpotential:

$$\eta = \phi_s - \phi_l - E_{eq}. \quad (2.5)$$

The local current density is then related to the overpotential through a kinetic law, such as Butler-Volmer kinetics. This level of modeling is useful when charge-transfer limitations at the interface are expected to play a significant role.

The **tertiary current distribution** also includes species transport in the electrolyte. In that case, ionic fluxes are governed by different phenomena, modeled for example through the Nernst-Planck equation:

$$\mathbf{N}_k = -D_k \nabla c_k - z_k u_k F c_k \nabla \phi_l + c_k \mathbf{u}, \quad (2.6)$$

where c_k , D_k , z_k and u_k are the concentration, diffusion coefficient, charge number and mobility of species k , and $\mathbf{u}$ is the fluid velocity. This approach is more complete but also requires more parameters and a higher computational cost.

2.2.7 Electrical properties of PSi

The interest of PSi for RF applications comes from the strong modification of the effective electrical properties of the substrate. Since the porous layer is a mixture of silicon and air, its effective permittivity is much lower than the one of bulk silicon. Depending on the porosity and on the fabrication conditions, effective relative permittivity in the range of a few units can be obtained. For example, PSi layers with porosities between about 40% and 90% can lead to effective relative permittivity significantly below the value of crystalline silicon, with values between 2.5 and 6.5 (Scheen, Tuytaerts, Van Overmeere, *et al.* 2025).

The effective resistivity of PSi can also be much larger than the one of the starting wafer. This increase is related to the reduction of the continuous crystalline silicon cross-section and to the large density of defects and traps located on the pore walls. These traps can pin the Fermi level and reduce the number of mobile carriers participating in conduction. As a consequence, PSi can behave as a highly resistive material even when it is formed from initially doped silicon (Scheen, Tuytaerts, Rack, *et al.* 2020; Aroutiounian and Ghulinyan 2003; Nabet 2025).

2.3 Integration of PSi

As stated in the introduction, even though PSi has attractive electrical properties, its integration into a CMOS-compatible process is challenging. If PSi is fabricated before the front-end process, it must withstand the full thermal and mechanical constraints of CMOS fabrication. High-temperature annealing can modify the Si-H passivation of the pore walls and can induce mechanical stress because PSi and crystalline silicon do not have the same mechanical resistance and coefficient of thermal expansion. The brittleness of PSi can then lead to wafer bending, cracking or fracture (Capelle *et al.* 2012). Another difficulty is surface roughness. A porous layer fabricated before device processing generally requires planarization before subsequent deposition or lithography. This increases process complexity and can be incompatible with standard foundry process flows (Gautier and Leduc 2014; Tuytaerts *et al.* 2026). For this

reason, the idea of forming the porosification region after processing the front-end device emerged.

2.3.1 Post-process porosification

The key idea of post-process porosification is to invert the fabrication sequence. Instead of forming PSi first and fabricating the RF structures on top of it, the RF structures are fabricated first using a conventional process flow. The silicon substrate is then porosified locally from the back-side, underneath the regions of interest. This approach prevents the porous layer from being exposed to high-temperature front-end processing and avoids direct contact between the front-side devices and the HF-based electrolyte.

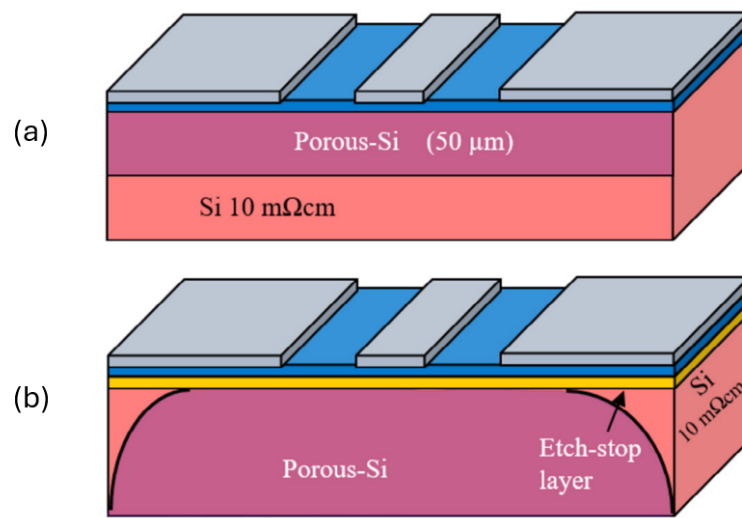


Fig 2.5. Schematic of a CPW transmission line built on top of (a) pre-process PSi and (b) post-process PSi, adapted from Scheen, Tuyaerts, Rack, et al. 2020

In the first post-process demonstrations developed at UCLouvain, back-side anodization was used to transform the silicon substrate into PSi below RF CPW structures (Scheen, Tuyaerts, Rack, et al. 2020). The porosification is localized by a back-side mask and grows approximately isotropically from the exposed openings. In contrast with a pre-process porous layer, the post-process porous pocket will extend through the whole substrate thickness below the RF structures while the front-side is isolated. The difference between both integration routes is summarized in Figure 2.5. In 2.5(a), the result of the pre-process PSi is a layer of 50 μm is atop of the Si while in 2.5(b), the porosification starting from the back-side makes the whole thickness porous below the structures.

2.3.2 Porosification of low-ρ wafers

The first implementation of this post-process technique used heavily doped P⁺ silicon wafers with a nominal resistivity of 10 mΩ cm to 20 mΩ cm. This low resistivity was chosen to ensure

a nearly uniform current distribution across the wafer. During back-side porosification, the current is injected from an electrode placed at the wafer edge, as shown in Figure 2.6. If the silicon substrate is too resistive, porous pockets close to the electrode receive more current than pockets located near the wafer center, leading to non-uniform porosification depth.

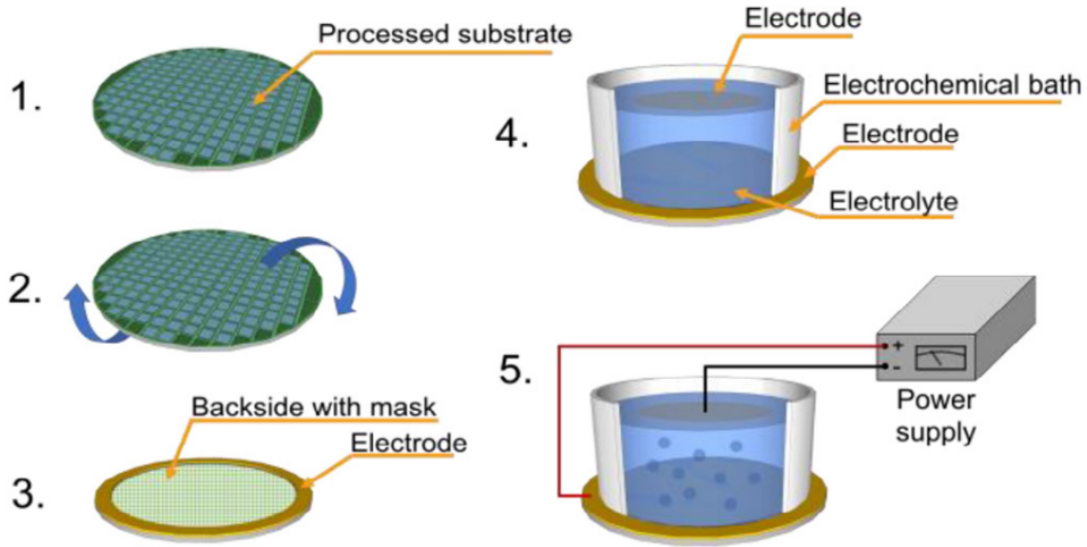


Fig 2.6. Schematic of post-process PSi fabrication from Scheen, Tuyaerts, Rack, et al. (2020)

This behavior can be understood with the simplified resistance model shown in Figure 2.7. For a pocket located far from the current-injection electrode, the current must travel laterally through a longer silicon path before reaching the porosification region. As the voltage drop must be the same along all current paths, the ratio of the currents at the edge and at the center can be written as

$$\frac{I_{edge}}{I_{center}} = 1 + \frac{R_{Si}}{R_e} \quad (2.7)$$

If the silicon resistance is negligible compared with the electrolyte resistance, this additional path does not significantly affect the current distribution. This is the case for P⁺ wafers.

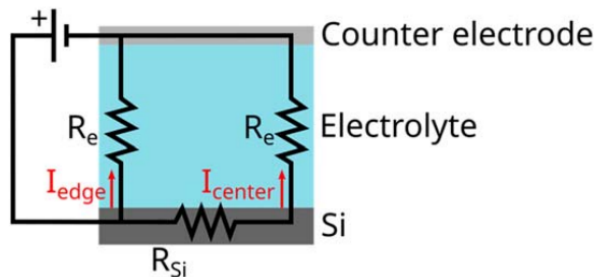


Fig 2.7. Equivalent circuit of the porosification setup, extracted from Scheen, Tuyaerts, Van Overmeere, et al. (2025)

However, the use of highly doped P⁺ wafers is not ideal for industrial CMOS integration. Such substrates can introduce contamination risks in production lines and are not representative of standard bulk or high-resistivity CMOS substrates. This limitation motivated the development

of post-process porosification on standard-resistivity silicon.

2.3.3 Porosification of standard-resistivity wafers

Standard-resistivity silicon wafers, typically in the range of 10–20 Ωcm , are more compatible with industrial CMOS processes and avoid the contamination risks associated with P^+ substrates. However, their higher resistivity makes current distribution during back-side porosification much less uniform.

Scheen, Tuyaerts, Van Overmeere, *et al.* (2025) studied this issue experimentally and with three-dimensional finite-element simulations. Wafers with resistivities of 0.004 Ωcm , 0.24 Ωcm and 15 Ωcm were porosified under comparable conditions. The porosified depth was then measured as a function of the distance from the current-injection electrode. The results showed that the depth ratio between the wafer center and the wafer edge decreases strongly as the substrate resistivity increases. For standard-resistivity wafers, the current distribution becomes too non-uniform if only an edge electrode is used.

To overcome this limitation, a conductive metal grid is deposited on the wafer back-side in the inter-die regions. The grid acts as a low-resistance current distributor in parallel with the silicon. Instead of forcing the current to travel laterally through a high-resistivity wafer, the grid distributes the potential over the wafer back-side and supplies the porosification openings more uniformly. Experimental validation on three-inch wafers and simulations extended to 300 mm wafers showed that this approach can restore a nearly uniform porous depth across the wafer (Scheen, Tuyaerts, Van Overmeere, *et al.* 2025).

An idealized schematic top-view of a wafer with the back-side grid deposited is displayed in Figure 2.8. There is one porous pocket in each die. The resist protects the wafer from the electrolyte except the openings from which the porosification will start. The resist is also above the metallic grid and ring but is not represented for readability. The electric contact is still done by the metallic ring, as in previous experiments.

2.3.4 Etch-stop layer and geometric effect

Post-process porosification also requires a stopping structure near the front-side. Without such a structure, the porous front could continue propagating until it damages the RF metallic patterns or the active devices. In SOI substrates, an additional polysilicon layer can be introduced beneath the BOX to act as an effective stopping layer for the porosification front. Due to its resistivity higher than crystalline silicon, only a small part of the total current density will flow through it and its etching will therefore be negligible compared to the porosification of the silicon (Tuyaerts *et al.* 2026).

The role of the etch-stop layer is twofold. It must protect the front-side structures from the

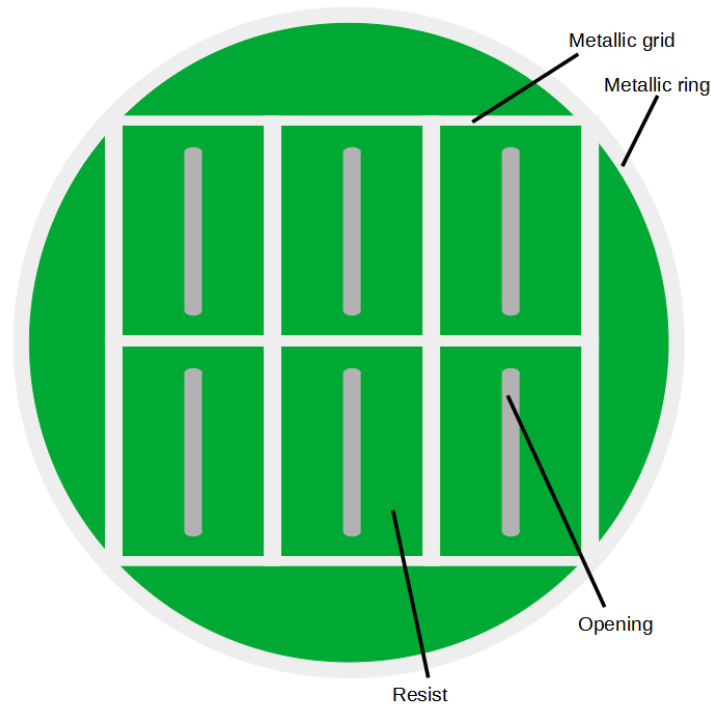


Fig 2.8. Idealized schematic top-view of a wafer with back-side grid. The resist is not represented above the grid and the ring for readability. The structures are not on scale.

HF-based electrolyte, while allowing the PSi to replace as much of the lossy silicon volume as possible. The residual non-porosified silicon thickness below the RF structures should indeed be minimized, because this remaining silicon still contributes to the effective resistivity and effective relative permittivity sensed by the CPW.

A limitation of the polysilicon layer as an etch-stop is the creation of a non-uniformity in the remaining non-porosified thickness. Indeed, as shown in Figure 2.9, the current path from the center of the pocket to the electrode (2.9 (a)) has a really small cross-section for a long distance and is thus seen very resistive compared to the path from the side of the pocket (2.9 (b)). This results in a thicker non-porosified region at the center of the pocket. This effect, called the geometric effect, is a problem because it will probably degrade the RF performance just above this zone which is exactly where the structures of interest are located (in our case, CPW).

This can be seen on SEM images from Tuybaerts *et al.* (2026), in Figure 2.10. After the porosification, the crystalline Si layer remaining in the middle of the pocket is more than 5 times thicker than on the side, confirming that this could deteriorate the effective parameters of the resulting substrate.

2.3.5 RF performance of post-process PSi

The porous pockets reduce the amount of conductive silicon below the transmission lines. This leads to reduced effective permittivity and improved effective resistivity compared with

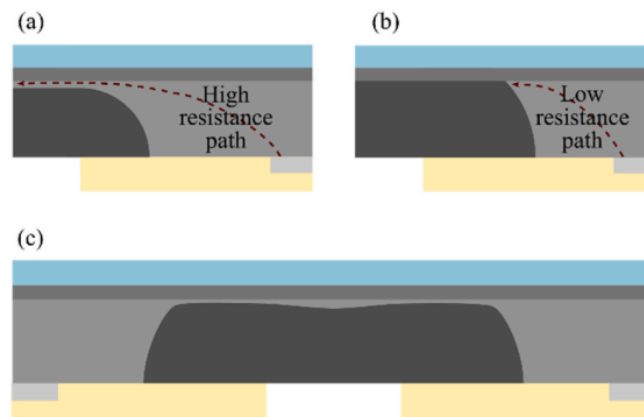


Fig 2.9. Schematic representation of the geometric effect observed near an etch-stop layer, adapted from Tuybaerts et al. (2026).

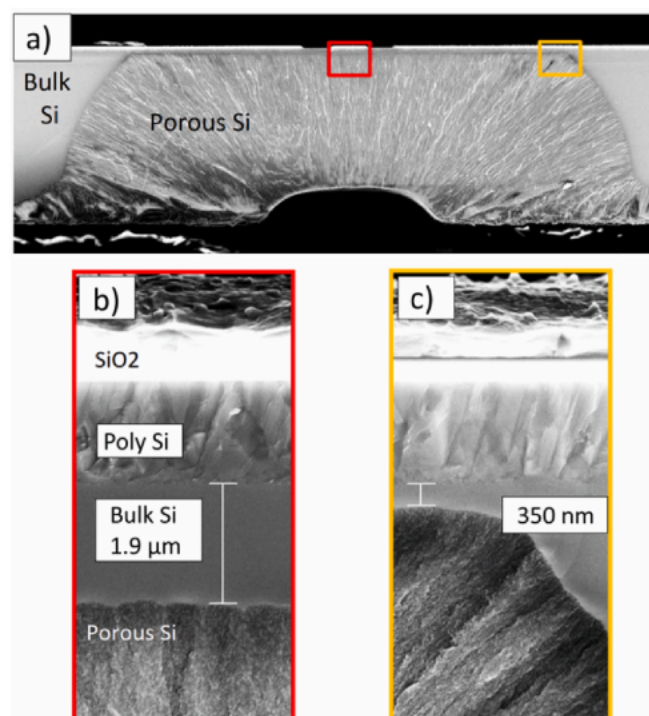


Fig 2.10. SEM observation of a residual non-porosified silicon layer after post-process porosification near an etch-stop layer, adapted from Tuybaerts et al. (2026).

standard silicon substrates. The post-process PSi fabricated by Tuybaerts *et al.* (2026) exhibits an effective relative permittivity of $\epsilon_{r,\text{eff}} = 4.3$ and an effective resistivity above $3 \text{ k}\Omega\text{cm}$ at 5 GHz. These characteristics can be compared to trap-rich technology (TR-SOI), which is a reference in the RF-SOI technologies. According to Rack (2021), this technology exhibits $\epsilon_{r,\text{eff}} = 10$ and an effective resistivity above $10 \text{ k}\Omega\text{cm}$ at 5 GHz. The PSi is then an interesting alternative as it can provide a lower $\epsilon_{r,\text{eff}}$ than the TR-SOI. The lower ρ_{eff} value can seem problematic but substrates with effective resistivities above $3 \text{ k}\Omega\text{cm}$ contribute in a negligible way to the insertion losses compared to the ohmic losses from the metallic CPW lines.

This tends to prove that the PSi substrates can have really interesting RF performance while being implemented in BULK technology for a lower cost.

2.3.6 Toward post-process PSi integration in bulk CMOS

The previous developments show that post-process PSi can be integrated on standard-resistivity wafers if the current distribution is homogenized by a back-side metallic grid, and that excellent RF properties can be obtained when the porous front is stopped close to the RF structures. The remaining challenge is the transfer of this approach to bulk CMOS.

In bulk CMOS, the continuous silicon substrate does not contain a buried oxide or a continuous polysilicon etch-stop layer below the front-side. Adding such a layer would strongly reduce the compatibility with standard bulk processes. Therefore, a different stopping strategy will be investigated in this work.

Chapter 3

P- and N-doped regions as a bulk etch stop layer

The post-process PSi integration demonstrated on SOI substrates by Tuyaerts *et al.* (2026) relies on a critical structural feature of SOI technology: the buried oxide (BOX) layer. Thanks to this layer, a polysilicon layer can be deposited right below the BOX without compromising the functioning of the circuit. As the porosification front progresses from the wafer back-side through the substrate, it stops naturally at the polysilicon interface, because of the electrical resistivity difference. Indeed, the resistivity of the polysilicon is very high compared to the one of crystalline silicon. The current flowing through the layer is then very limited.

In a standard bulk CMOS substrate, no such continuous protecting layer could be added. The silicon is continuous from the back-side to the active transistor layer on the front-side. If the back-side porosification process is applied without modification, the porous front will have no natural stopping mechanism and will either reach and damage the front-side devices, or require a precisely timed process stop. Of course both of these situations are not suitable for an industrial integration. A replacement for the etch-stop strategy is therefore essential before the post-process PSi process can be transferred to bulk CMOS technology.

A candidate that emerges from the physics of the electrochemical anodization process and from the bulk CMOS technology itself is the use of an alternating layer of P- and N-doped regions. As will be shown in this chapter, the electrical characteristics of the alternation of these regions could be able to stop the porosification front. Furthermore, it could be done without any additional deposited layer or structural modification of the substrate. Indeed, the wells of the bulk CMOS transistors that are on the front-side will be reached from the back-side in the case of a porosification process.

This chapter first presents the physical mechanisms by which PN patterns may slow down or stop the porosification front. Representative doping candidates are then compared through their simulated resistivity maps. The goal is not to identify a final optimal structure from the

resistivity maps alone, but to have a first insight about which candidates provide a promising compromise between etch-stop robustness and RF performance as, in the optimal case, the wells of the transistors should be used.

3.1 Physical origin of the etch-stop mechanism

To understand why alternating P- and N-type regions can act as an etch-stop, it is necessary to recall the fundamental mechanism governing the dissolution of silicon in HF-based electrolytes. As discussed in Section 2.2, the electrochemical dissolution of silicon requires the presence of holes (h^+) at the silicon surface. In the absence of holes, the silicon surface remains passivated by Si-H bonds that are stable against spontaneous HF attack, and no dissolution occurs.

Of course, the availability of holes at any given point in the silicon is governed by the current supply and not by the presence of HF. Two regions of silicon that are in contact with the electrolyte can therefore behave completely differently during anodization if they differ in their ability to supply holes to the surface.

In P-type silicon, holes are the majority carriers and are driven toward the Si/electrolyte interface by the applied electric field. The surface is continuously supplied with holes, the dissolution reaction proceeds, and porous silicon forms.

In N-type silicon under the same current supply, the situation is fundamentally different. Holes are minority carriers. Without any additional hole-generation mechanism, as the hole concentration at the interface is at a negligible level, the dissolution reaction is then also negligible and the N-type silicon remains theoretically intact and passivated. In practice, it can be said that the porosification is very selective to the P-type region compared to the N one, as the etching rate is greatly reduced in the second one compared to the first, rather than saying that the N are not etched.

We have therefore a mechanism that avoids the porosification in the N regions but it does not help about the P regions. The role of the PN alternation is therefore to restrict the current supply to the remaining P-type paths.

Depletion regions are created between adjacent P- and N-type regions because of the band bending due to the junction. These depleted regions contain few mobile carriers and therefore behave as high-resistivity barriers. During porosification, they are expected to reduce the lateral current supply toward the P-type regions located between adjacent N-type barriers. In the structures considered here, depletion regions are expected at the interfaces between the N-doped regions and the surrounding P-type material. This includes the lateral PN interfaces between adjacent wells, as well as the interface between the N-doped regions and the P-type substrate. The flow of current from the substrate to the N regions will then also be reduced.

As the porous front progresses into a P-type region located between two N-type barriers, the remaining non-porosified silicon path connecting the active front to the bulk becomes increas-

ingly constricted. The current must then flow through a narrower region between two depleted PN interfaces. This increases the local access resistance and reduces the current density available at the porosification front. This mechanism will be referred to as the "bottleneck effect" in the following sections.

The proposed stopping layer therefore relies on two complementary mechanisms. First, the N-type regions exhibit a much lower porosification rate because of the limited hole supply. Second, the depletion regions formed at the PN interfaces reduce the current supply to the adjacent P-type regions. These two mechanisms are summarized schematically in Figure 3.1. In Figure 3.1(a), the N-type region is protected by both its poor hole supply and the surrounding depleted interfaces. In Figure 3.1(b), the P-type region is progressively isolated laterally by the neighboring N-type regions, so that the current supply is restricted through a narrow path underneath the remaining silicon.

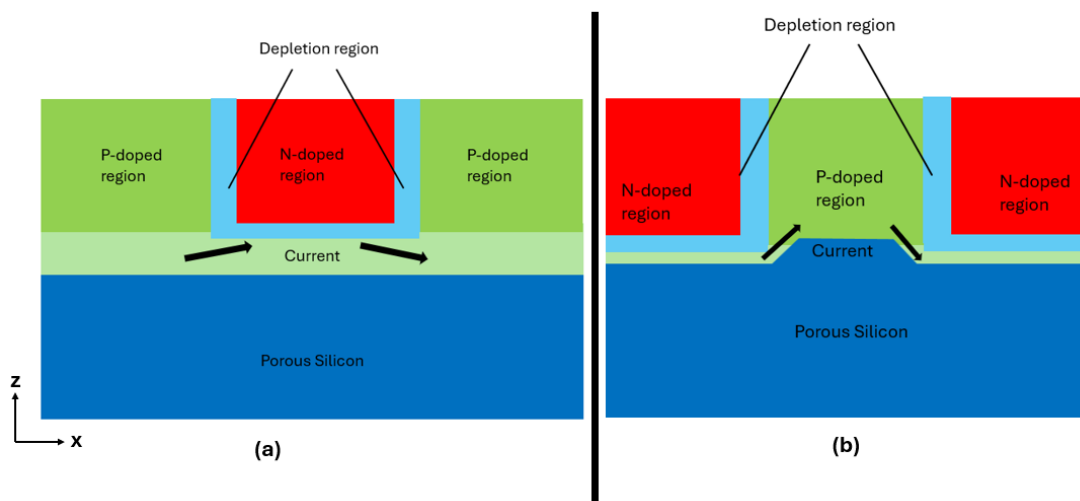


Fig 3.1. Schematic representation of the two mechanisms contributing to the PN etch-stop effect: (a) reduced porosification of a N-type region due to the limited hole supply and surrounding depleted interfaces; (b) current bottleneck in a P-type region laterally confined by neighboring N-type barriers.

These mechanisms should not be interpreted as ideal blocking effects. N-type silicon are still slowly being attacked and depletion regions still allow leakage current. Consequently, if the stopping layer remains in contact with the electrolyte for a sufficiently long time, the porous front may eventually cross the barrier and reach the front-end structures. Nevertheless, the expected delay compared with a uniformly P-type substrate makes PN regions a promising candidate for a bulk-compatible porosification stopping layer, alongside the availability of the wells of the bulk CMOS transistors.

3.2 Representative doping candidates

The previous section introduced the physical mechanisms by which PN patterns can slow down or stop the porous front. The next step is to identify which doping profiles and lateral dimensions provide a suitable compromise between stopping efficiency and RF performance. The ideal structure should prevent the porous silicon from reaching the front-end devices, while still allowing the porous region to extend sufficiently close to the RF field region in order to reduce substrate losses.

Preliminary research was done to define representative doping parameters that would reproduce order of magnitudes of the industrial implantations of the transistor wells¹. Four types of candidates stand out with varying doses, presented in Table 3.1. The implantation energy controls the depth of the implanted dopant profile, while the dose controls the amount of implanted dopant.

Candidate	E_N [keV]	E_P [keV]	D_N [10^{12} at./cm ²]	D_P [10^{12} at./cm ²]
pn++	190	140	12	3
pn+	190	140	2.8	0.7
n++	190	140	10	0
n+	190	140	2.3	0

Table 3.1: Representative implantation parameters used for the PN stopping-layer candidates.

From now, the variables W_n and W_p will be used as referring to the width of the N regions and of the P regions respectively. The minimum feature size is limited by the available lithography equipment at UCLouvain to approximately 1 μm . There is no strict upper limit, but the selected values must remain representative of well dimensions in bulk CMOS technologies and sufficiently narrow to preserve the bottleneck effect described in Section 3.1. The values investigated in this work are $W_p = \{1, 1.5, 2, 3, 4, 5\} \mu\text{m}$ with $W_n = \{2, 4\} \mu\text{m}$. For clarity, only the results for $W_p = 2 \mu\text{m}$ and $W_p = 4 \mu\text{m}$ with $W_n = 2 \mu\text{m}$ are discussed in this section.

The following heatmaps show the simulated resistivity distributions obtained from the corresponding dopant profiles. Low-resistivity regions correspond to highly doped conductive regions, whereas high-resistivity regions indicate depleted zones. These maps are useful because the local resistivity is a key parameter controlling the current distribution and because the conductivity map will be used as an input for the porosification simulations discussed later. However, the maps must be interpreted carefully: a low resistivity inside an N-type region should not be confused with a high porosification rate, since the electrochemical selectivity of N-type silicon is governed by the limited availability of holes.

One should be careful that, in all the following Figures of this chapter, the z-axis is now pointing downwards to improve the readability of the heatmaps.

Figure 3.2 shows the n+ and n++ candidates for $W_p = 2 \mu\text{m}$. Since no additional P-type region

¹Research done by Thibault Fiasse, 2025 UCLouvain

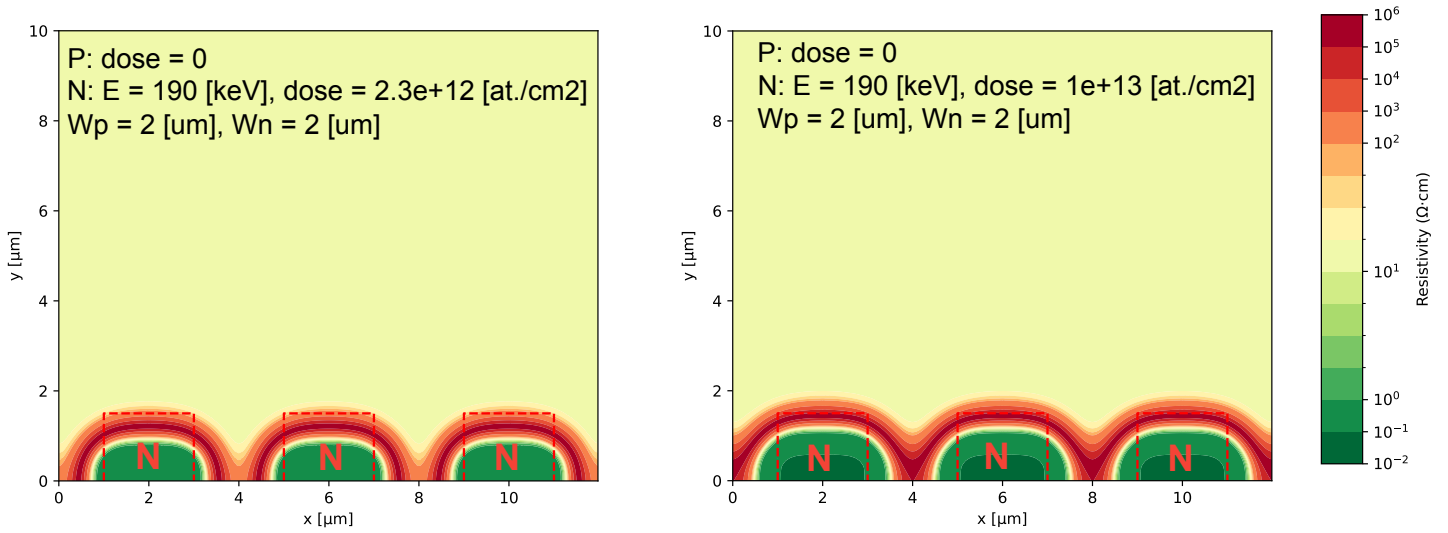


Fig 3.2. Resistivity maps of the n^+ (on the left) and n^{++} (on the right) candidates for $W_p = 2 \mu\text{m}$ and $W_n = 2 \mu\text{m}$

is implanted between the N-type regions, the material between adjacent wells corresponds to the native P-type substrate. The high-resistivity regions surrounding the N-type wells extend significantly and merge laterally. From an etch-stop perspective, this configuration is expected to be highly protective: the N-type wells are closely spaced, and the depleted barriers strongly restrict the current supply through the region between them. As the N dose is higher on Fig 3.2 right-side, the resistivity inside the N regions is lower due to the presence of more dopants and the depletions are wider in this case. This will be true for all the candidates in this section.

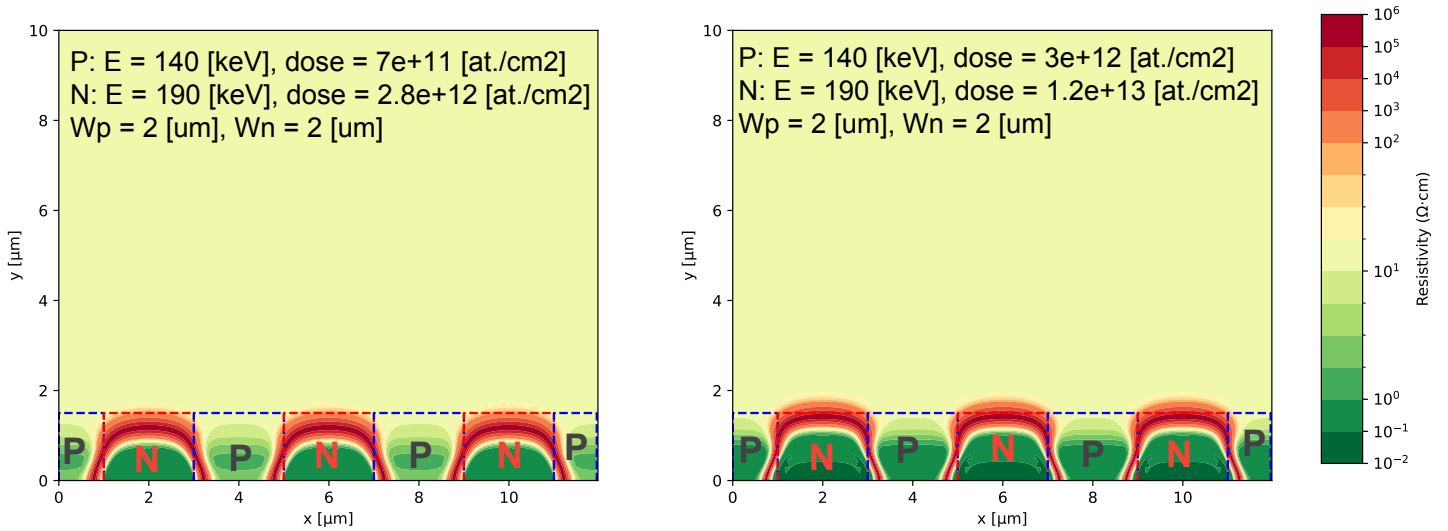


Fig 3.3. Resistivity maps of the pn^+ (on the left) and pn^{++} (on the right) candidates for $W_p = 2 \mu\text{m}$ and $W_n = 2 \mu\text{m}$

Figure 3.3 shows the corresponding pn^+ and pn^{++} candidates. The addition of an implanted P-type region between the N-type wells modifies the resistivity distribution. The P-type region forms a more conductive path between adjacent N-type barriers. This is less favorable for etch-

stop robustness because holes and current can be supplied more easily to the porosification front. However, it may be beneficial from an RF point of view because it allows the porous silicon to penetrate further between the PN structures, reducing the amount of remaining non-porosified silicon below the front-side RF structures.

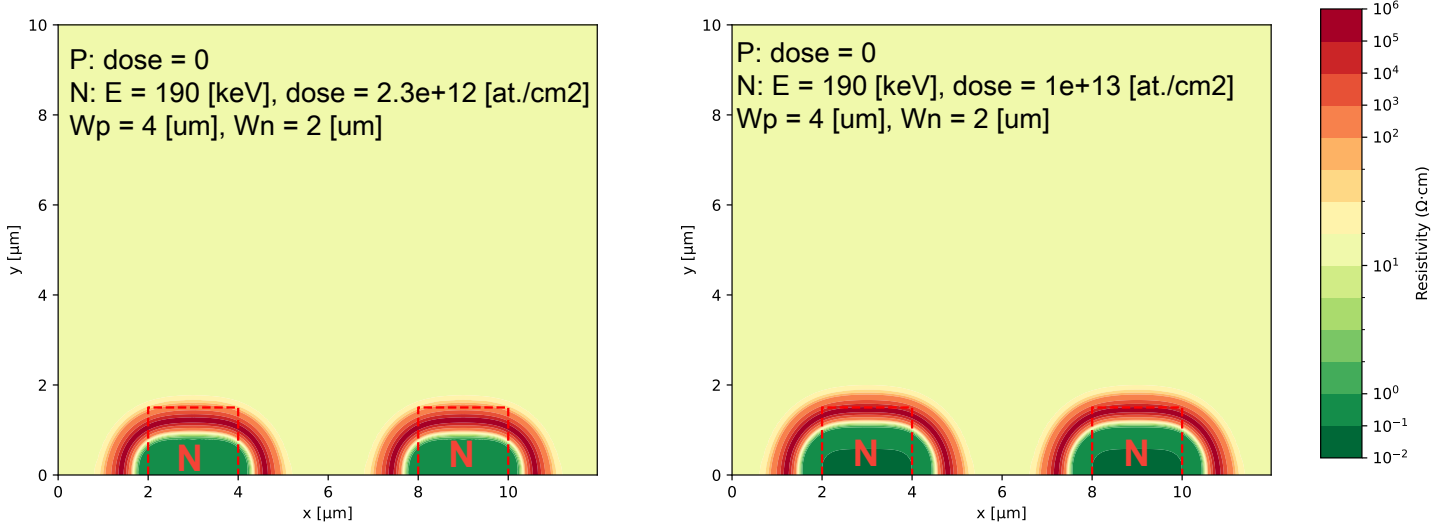


Fig 3.4. Resistivity maps of the n^+ (on the left) and n^{++} (on the right) candidates for $W_p = 4 \mu\text{m}$ and $W_n = 2 \mu\text{m}$

Figure 3.4 shows the n^+ and n^{++} candidates for $W_p = 4 \mu\text{m}$. Compared with Figure 3.2, the N-type wells are further apart. The high-resistivity regions no longer merge completely, and a region close to the native substrate resistivity remains between the wells. This configuration is, again, expected to be less protective than the $W_p = 2 \mu\text{m}$ case, but it may allow a deeper penetration of porous silicon before the current bottleneck becomes dominant.

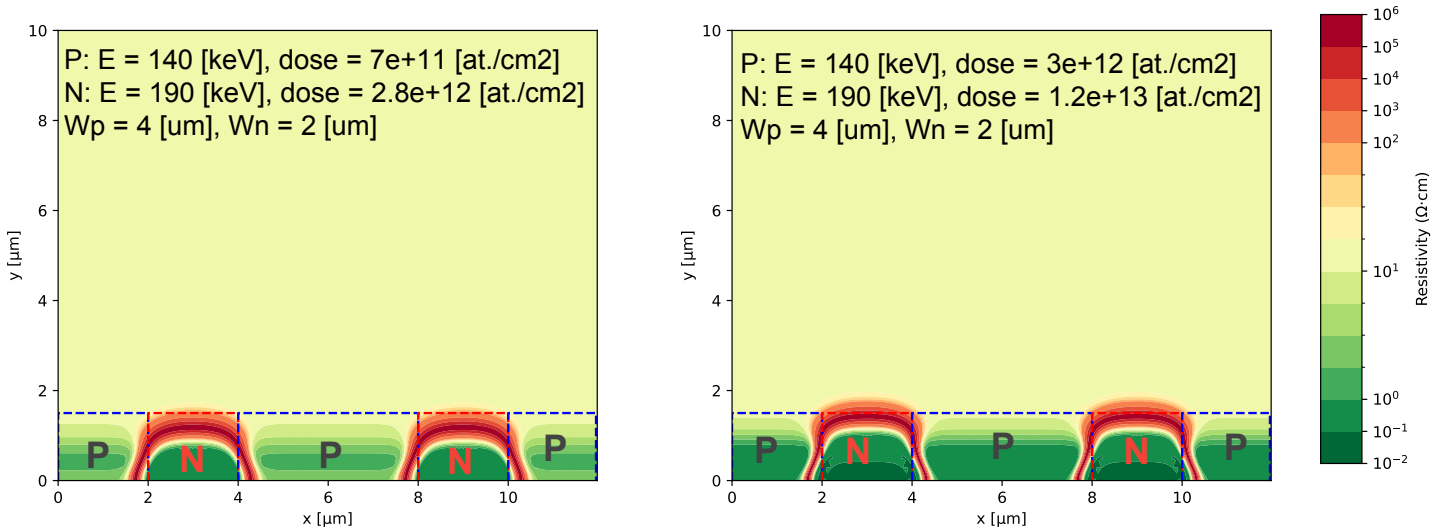


Fig 3.5. Resistivity maps of the pn^+ (on the left) and pn^{++} (on the right) candidates for $W_p = 4 \mu\text{m}$ and $W_n = 2 \mu\text{m}$

Figure 3.5 shows the pn^+ and pn^{++} candidates for $W_p = 4 \mu\text{m}$. These structures provide the

widest P-type conductive region between neighboring N-type barriers. They are therefore expected to be the least robust from a pure etch-stop point of view. However, they may provide the best RF benefit if the porosification remains controlled, because the porous silicon can replace a larger fraction of the silicon volume located between the PN structures.

The comparison of these candidates highlights a fundamental trade-off. Closely spaced N-type regions without additional P implantation provide the strongest high-resistivity barriers and are therefore expected to be the most efficient etch stops. However, they may also stop the porous front too early, leaving a larger volume of non-porosified silicon below the RF structures. Inversely, candidates with wider or more conductive P-type regions may allow deeper porosification between the N barriers, which is favorable for RF performance, but they also increase the risk of locally piercing the stopping layer.

The optimal candidate must therefore balance two requirements: sufficient stopping robustness to protect the front-end devices, and sufficient penetration of porous silicon between the PN regions to minimize the remaining conductive silicon volume. The resistivity maps provide a first indication of this trade-off, but dynamic porosification simulations and experimental cross-sections are required to determine which candidate gives the best compromise.

3.3 Alternative candidates

The candidates discussed so far place the P- and N-type regions close to the front-side surface. This configuration is favorable for protecting the devices, but it may also stop the porous front too early, leaving a significant non-porosified silicon thickness below the RF structures. An alternative strategy is therefore to shift the P-type region deeper into the substrate. In this configuration, the porous front can first progress through this more conductive part of the substrate before reaching a less conductive part that will not get etched too fast while the neighboring N-type regions still provide lateral confinement.

This approach is no longer directly representative of the existing transistor wells, but it is useful for evaluating whether a deeper engineered doping pattern could provide a larger process window: the porous front could penetrate further before being stopped, while still avoiding a complete breakthrough toward the front-side devices because of the easier etch of the P-type regions at the beginning and then slower porosification when becoming really close to the end of the layer.

The idea in this section is then to increase the implantation energy to 750 keV, a value that is quite high but still in the range of the industry (Matsusada Precision 2026). The alternative candidates are based on the pn⁺ and pn⁺⁺ structures, with the new implantation energy. The effect of the annealing temperature is also examined. A higher annealing temperature increases dopant diffusion, which modifies both the lateral width and the depth distribution of the implanted regions. This can either improve or degrade the trade-off between the bottleneck

effect and the accessibility of the P-type region, depending on the initial spacing between the N-type barriers.

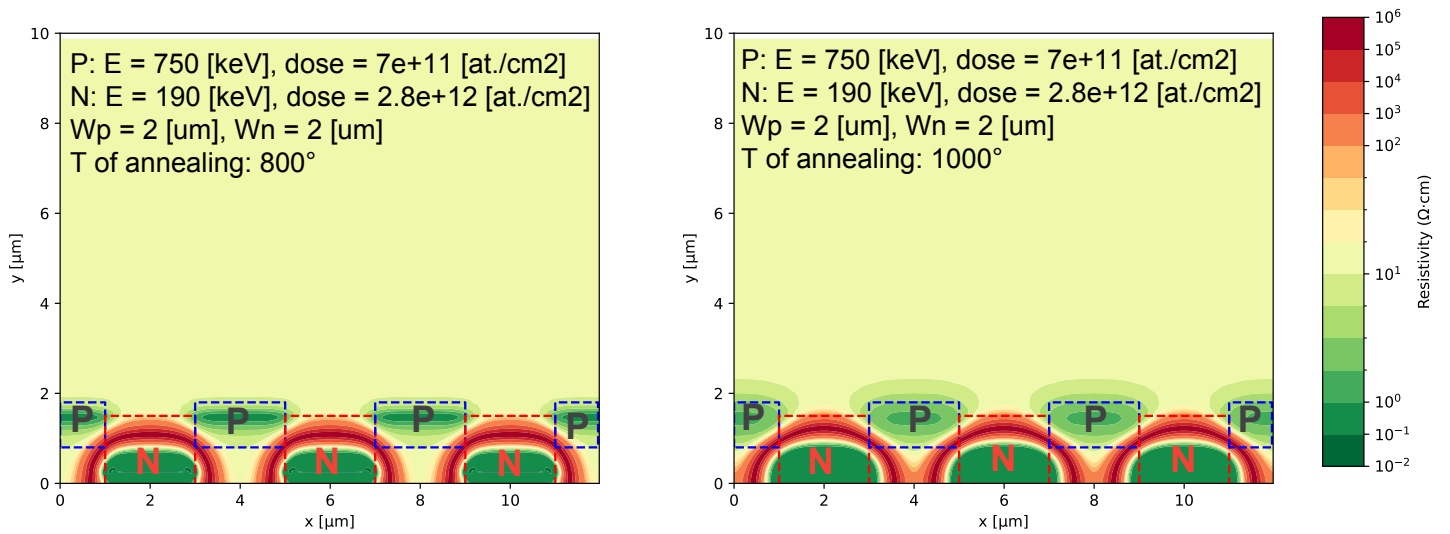


Fig 3.6. Resistivity maps of the pn+ candidate for $W_p = 2 \mu\text{m}$ and $W_n = 2 \mu\text{m}$, comparing annealing temperatures of 800°C (left) and 1000°C (right)

Like in previous section, the difference between the pn+ of Figure 3.6 and the pn++ of Figure 3.7 is the dose and so we see that the p-type regions are larger in the second one and have a lower resistivity. The zone will then get porosified even faster. However, in both cases, the zone between the n-type regions is really tight and it can be expected that the bottleneck effect will be very strong here. In both Figures, it can be seen that the effect of a higher annealing temperature is that the depletion regions join each other. This will not clearly not minimize the remaining silicon part. Those candidates are therefore probably not the best ones to improve this aspect. For the two cases at 800°C, the zones between the N-type regions are also narrow, it will probably not improve a lot the penetration compared to the previous candidates.

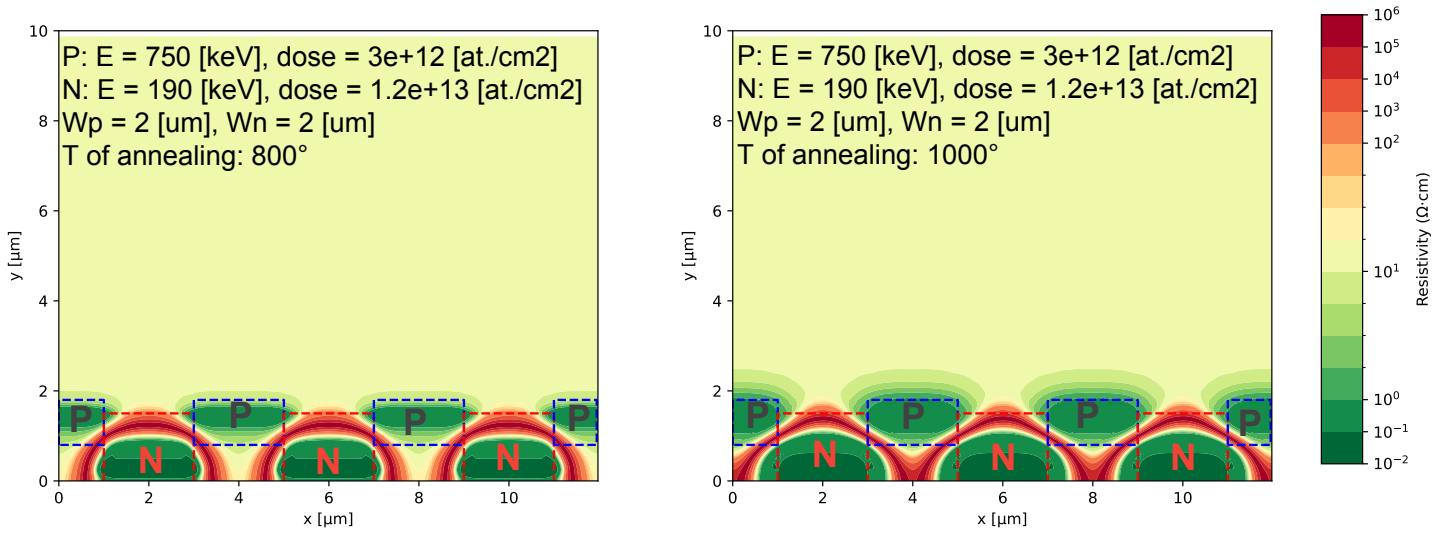


Fig 3.7. Resistivity maps of the pn^{++} candidate for $W_p = 2 \mu\text{m}$ and $W_n = 2 \mu\text{m}$, comparing annealing temperatures of 800°C (left) and 1000°C (right)

For $W_p = 4 \mu\text{m}$, the effect of increased annealing temperature becomes more favorable. As shown in Figure 3.8, the P-type region remains wide enough not to be completely squeezed between the N-type barriers. At the same time, the diffusion of the dopants reduces the effective spacing between the high-resistivity regions, preserving a bottleneck effect. This configuration is therefore expected to offer a better compromise than the $W_p = 2 \mu\text{m}$ alternatives. However, this could also lead to a fast breakthrough of the stopping layer with a total porosification.

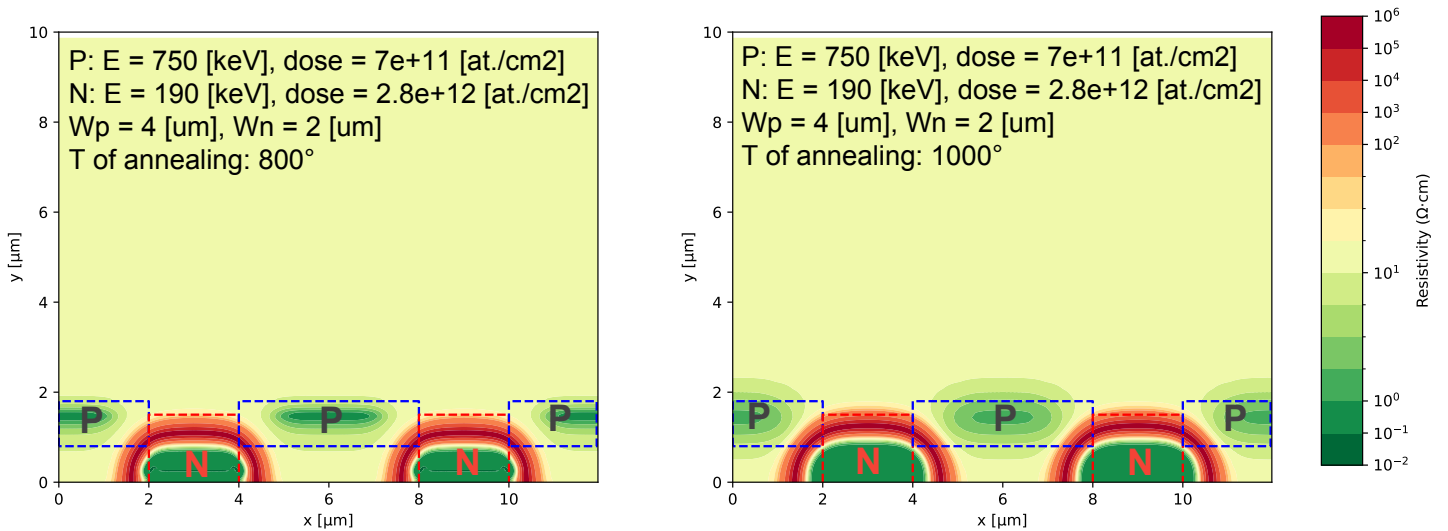


Fig 3.8. Resistivity maps of the pn^+ candidate for $W_p = 4 \mu\text{m}$ and $W_n = 2 \mu\text{m}$, comparing annealing temperatures of 800°C (left) and 1000°C (right)

The same trend is observed in Figure 3.9. From the static resistivity maps only, among the alternative candidates, the $W_p = 4 \mu\text{m}$ pn^{++} structure annealed at 1000°C appears to offer the most favorable compromise in the static resistivity maps. The P-type region remains

sufficiently wide to allow porosification between the N barriers. On the other hand, the lateral spacing between the depleted PN interfaces is smaller than the other thanks to the wider diffusion of the dopants. This geometry is therefore expected to preserve a strong bottleneck effect without stopping the porous front too early.

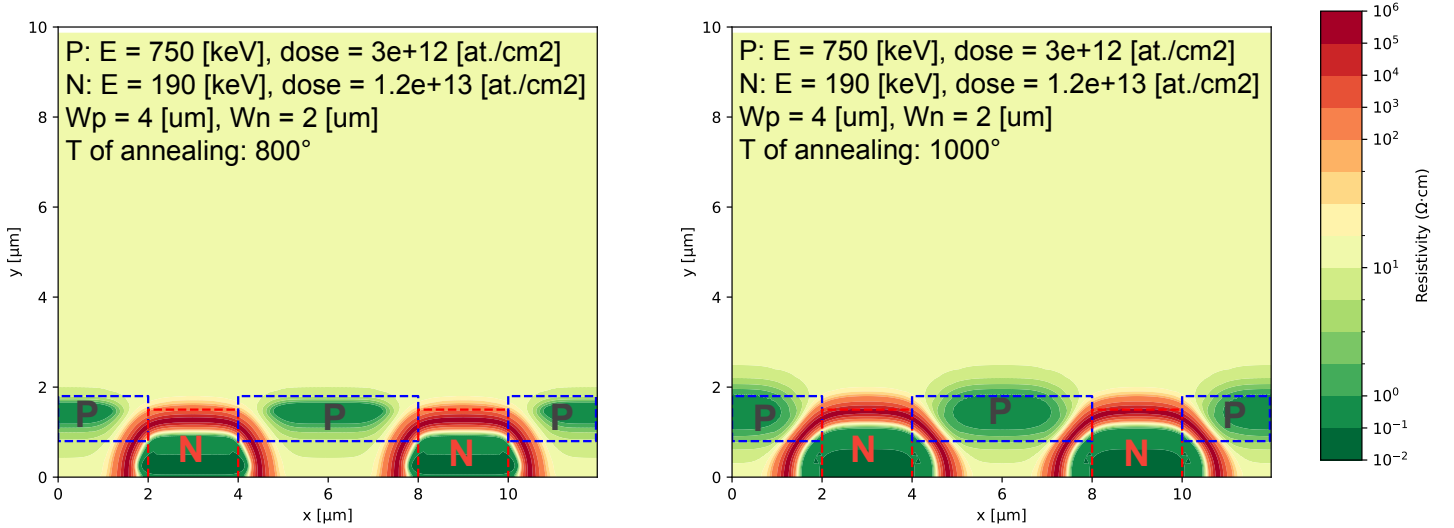


Fig 3.9. Resistivity maps of the pn^{++} candidate for $W_p = 4 \mu\text{m}$ and $W_n = 2 \mu\text{m}$, comparing annealing temperatures of 800°C (left) and 1000°C (right)

This conclusion must remain cautious. The analysis in this section is based only on static resistivity distributions before porosification. During the real process, the geometry evolves as silicon is replaced by electrolyte-filled porous silicon, and the local potential distribution may modify the depletion regions. The most promising candidates identified here must therefore be evaluated with dynamic porosification simulations and, ultimately, with experimental cross-sections after porosification.

3.4 Conclusion

This chapter introduced PN-doped regions as a bulk-compatible etch-stop strategy for post-process PSi integration. The stopping effect relies on two complementary mechanisms. First, the lower porosification rate of N-type silicon due to its limited hole supply, and the high-resistivity depletion regions formed at PN interfaces. Then, P-type regions are laterally confined between N-type barriers, the porous front can therefore also experience a current bottleneck as it progresses toward the front-side.

The comparison of the first representative resistivity maps shows that the most protective candidates are not necessarily the most favorable for RF performance. Closely spaced N-type regions maximize the depletion barrier and enhance the bottleneck effect, but they may prevent the porous silicon from penetrating sufficiently between the wells. Conversely,

wider or more conductive P-type regions can improve the expected RF benefit by reducing the remaining non-porosified silicon volume, at the cost of a weaker stopping margin.

The alternative candidates based on deeper P implantation attempt to improve this trade-off by allowing the porous front to penetrate further while preserving a lateral bottleneck between N-type barriers. The P regions are easier to penetrate as they are above the N-type ones. As a result, it can be expected that the window of time for stopping the porosification while having already a good penetration between the N is bigger than for the first candidates.

The resistivity maps provide a first screening of all the candidates but the final selection must rely on dynamic porosification simulations and experimental validation. Those two points will be investigated further in this work.

Chapter 4

Experimental results

After discussing the theory behind the PN stopping layer for silicon porosification, this chapter presents the first experimental implementation of this concept. The experimental work discussed here follows the process and test structures developed by Thibault Fiasse as part of his PhD thesis. The objective of this chapter is not to redefine the process itself, but to summarize the experimental strategy, highlight the main observations, and identify the issues that motivated the numerical simulations presented in the following chapters.

The chapter is organized as follows. Section 4.1 describes how the two-dimensional PN candidates discussed in Chapter 3 are translated into periodic three-dimensional layouts. Section 4.2 and Section 4.3 summarize the sample preparation and back-side porosification process. Section 4.4 introduces the physical and RF characterization methods. Finally, Section 4.5 discusses the main experimental observations, with particular attention to the penetration of PSi between the PN regions and to the macroscopic non-uniformity effects caused by the three-dimensional geometry.

4.1 Experimental implementation of the PN stopping-layer candidates

As discussed in Chapter 3, the stopping-layer candidate relies on a local modulation of the silicon doping with N- and P-doped regions. In the optimal case, the wells of the bulk transistors will be used to create this barrier. However, for the experimental validation, dedicated test patterns were designed in order to study the influence of the PN geometry independently of a complete transistor layout.

The doping parameter candidates were presented in previous section in 2D with different widths of junctions (W_p for the P-type regions and W_n for the N-type ones) but to implement these over a large area, the regions must be organized into periodic patterns. Two main

geometries are considered.

The first layout consists of parallel PN lines, displayed in Figure 4.1 (a). In this configuration, alternating P- and N-type stripes are repeated along one lateral direction. This geometry is the closest experimental realization of the two-dimensional structures discussed in Chapter 3. The line pattern can be oriented perpendicular to the pocket and the CPW (also called vertical lines), as in Figure 4.2 (c). Although, this will create high conductivity trenches parallel to the field lines generated by the CPW line resulting in elevated substrate losses. Inversely, a parallel orientation, also called horizontal lines, will interrupt the current paths relevant for the RF configurations. Those are displayed in Figure 4.2 (d).

The second geometry is a checkerboard pattern, where P and N regions are alternated in both lateral directions. The P are alternatively squares with W_P or W_N side length while the N regions are rectangles of W_P by W_N , completing the empty spaces. This is represented in Figs 4.1 and 4.2 (a). This pattern is more representative of a fully three-dimensional stop-ping structure, since the current cannot simply follow continuous high-conductivity paths throughout the wafer. It can be therefore expected to provide a more effective blocking of the porosification front and of the signal losses. It is also more representative of a real use of transistor wells. However, it is also more demanding experimentally because the pattern requires a true 3D description and contains a large number of corners. These corners may be rounded during lithography, which can modify the real geometry compared with the ideal mask design and create unwanted current paths. The pattern is also referred as "Flowers" in some experimental results.

A modified checkerboard layout is therefore introduced as a third variant. In this corrected version, the nominal mask dimensions are adjusted in order to compensate for the expected deformation of the pattern after fabrication. The goal is to obtain a fabricated PN distribution that remains as close as possible to the ideal layout. It is shown in Figs 4.1 (c) and 4.2 (b). The design will be referred as D-squares or D-Flowers.

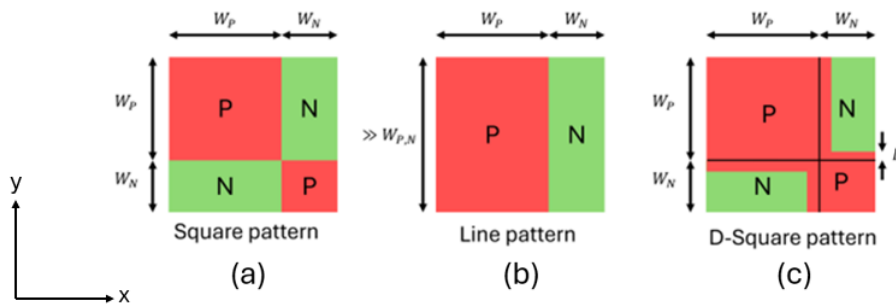


Fig 4.1. Schematic top-view of the PN stopping-layer 3D layouts implemented experimentally, from Thibault Fiasse.

In the experiments, these patterns are not fabricated individually under each device, but are instead implemented as periodic layouts. Inside the same wafer, there will be only one

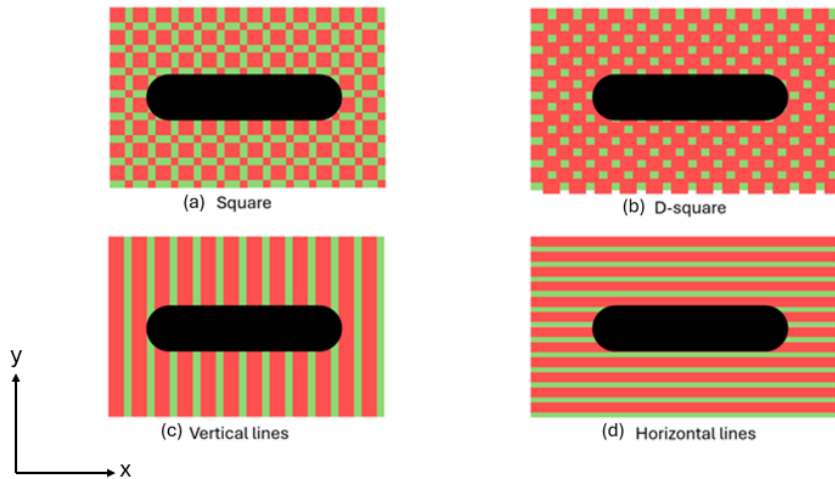


Fig 4.2. Schematic top-view of the PN stopping-layer 3D layouts implemented experimentally with the porous pocket in black, from Thibault Fiasse.

implantation set of parameters (the pn+, pn++, n+ and n++ candidates presented in previous Chapter). Variations of W_P , W_N and of the 3D patterns are introduced between the openings to study their impact. The schematic layer is displayed in Figure 4.3.

4.2 Preparation of the samples for porosification

The wafers are received after implantation of the PN stopping-layer patterns. The front-side process is then performed before the back-side porosification step. A dielectric layer is first deposited on the silicon substrate, and CPW structures are patterned above it. These CPW lines are used as RF test structures because they allow to extract easily the effective resistivity and effective relative permittivity of the substrate from the measured RF response.

A thick quartz layer is then bonded to the wafer above the front-end with the help of wax. This quartz carrier has two roles. First, it protects the front-side during the back-side process. Second, it provides mechanical support during thinning, since the remaining silicon thickness becomes small and hard to handle safely without reinforcement. The wafer is then thinned from the back-side to leave approximately 100 μm of silicon. This step is a key step because, as the porosification will be isotropic, the porous pocket will be as wide as thick. To avoid too much lateral porosification that would limit the density of the devices, it is then important to have a thinner wafer. After thinning, the back-side surface is chemically prepared in order to reduce excessive roughness while preserving sufficient surface texture for the adhesion of the following layers.

Afterwards, an inter-die metallic grid, exactly like the one developed by Scheen, Tuyaerts, Van Overmeere, *et al.* (2025), is deposited. This grid acts as the electrode used to inject the current during the electrochemical process. If the electrode is too close from the opening, there is

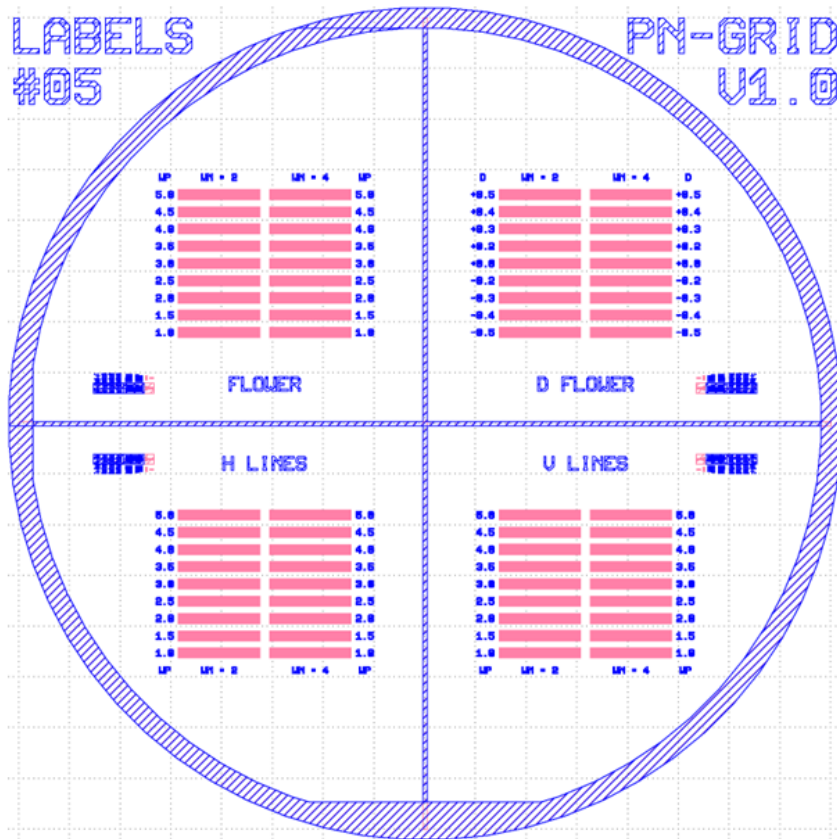


Fig 4.3. Mask layout of the experimental PN test structures. The four quadrants correspond to square/flower, modified square/modified flower, horizontal line and vertical line patterns. Each layout contains several W_p/W_n combinations designed to evaluate the effect of PN geometry on the porosification front. The blue represents the metal while the pink represents the absence of N doping. Layout from Thibault Fiasse.

a risk that the porous reach the electrode and so that the porosification gets short-circuited while if it is too far, the contact resistivity will become too big.

A thick protective photoresist layer is subsequently deposited on the back-side. This resist defines the openings through which the electrolyte can access the silicon. There is one opening per die. The protected regions remain isolated from the HF-based solution, while the exposed regions are available for electrochemical dissolution or porosification. Since HF is highly aggressive toward many materials used in micro-fabrication, the protection of the front-side devices and of the non-porosified regions is a key constraint of the process.

Before the main porosification step, an initial cavity is formed by operating in an electropolishing regime. The purpose of this pre-etched cavity is to improve the current distribution during the following porosification step. Without it, a bigger current density would concentrate at the edges of the opening. The final view of the back-side opening is displayed in Figure 4.4.

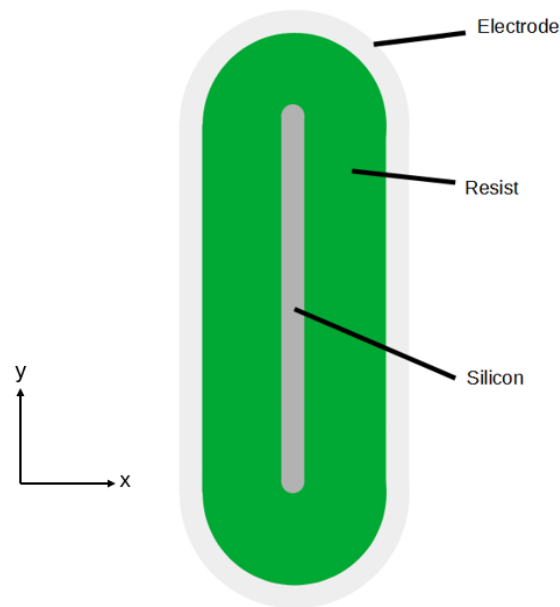


Fig 4.4. *Schematic view of one back-side opening after the preparation of the sample for the porosification*

4.3 The porosification process

The theoretical porosification process was introduced in Section 2.2. In this section, it will be presented in practice for this work. A cross-section in the x-z plane is displayed in Figure 4.5.

The porosification step is performed in an electrochemical cell. The back-side of the wafer is brought into contact with the electrolyte only through the resist openings, while the metallic grid provides the electrical contact required to inject current into the silicon. A counter-electrode is placed at the top of the electrolyte. The anodization reaction then takes place at the

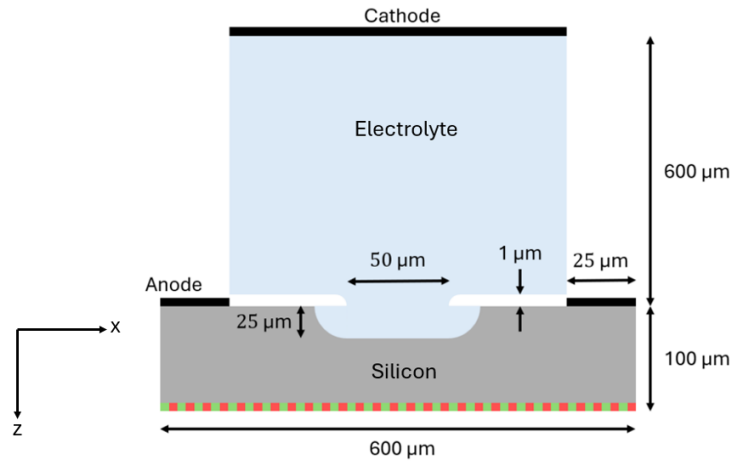


Fig 4.5. Schematic of the porosification setup for one opening. The wafer is upside down (z-axis pointing downwards). Image adapted from Thibault Fiasse

interface between the silicon wafer and the electrolyte in the pre-etched cavity. The schematic is for one opening only and is then reproduced for all the openings shown in Figure 4.3.

The HF-based electrolyte is composed of a 3:1 volume mixture of aqueous HF solution and isopropanol (IPA). The HF solution used for the mixture contained 49 % HF mass in water. IPA is added to the HF-based electrolyte to improve the wetting of the silicon surface. By lowering the surface tension of the solution, IPA helps the electrolyte spread over the silicon and penetrate into the porous network. This improves the renewal of reactive species inside the pores and contributes to a more homogeneous porosification process.

In the experiments, the current is sent with some pauses during porosification. This is important because the reaction requires fluoride species to reach the active silicon interface through the already formed porous region. Stopping the current supply for a sufficient period gives time for the electrolyte to replenish the pores and helps avoid a transition toward unwanted electropolishing during the porosification step. Furthermore, the process is inherently isotropic. Therefore, the PSi will grow laterally as well as toward the etch stopping layer. The surface of the interface is then increasing with the process going on. The total injected current is therefore updated through the whole process in order to aim for a constant current density at the interface. This is a crucial point because the morphology of the PSi depends on this current density. As the morphology of the porous must remain homogeneous in the whole wafer to ensure predictable electrical performances, so is the current density.

4.4 Characterization methods

Two types of characterization are used to evaluate the experimental samples. The first one is physical inspection of the porosified pockets. This is done by cross-sectional imaging using

Scanning Electron Microscope (SEM) and with top-view images obtained by optical microscopy. These images are used to determine whether the porous front stops before the front-side, whether it penetrates between the PN regions, and whether the remaining non-porosified silicon thickness is uniform.

The SEM works with a source of electrons that will send electrons toward the sample. The electrons will get reflected and pass through a detector. This will allow to get a very high-resolution image (Alicandro 2023).

The second one is RF characterization using the front-side CPW structures. Small-signal measurements provide information on the effective substrate resistivity and effective relative permittivity. These RF figures of merit are essential because a good stopping layer is not sufficient by itself: the PSi must also replace enough of the conductive substrate volume sampled by the RF fields to improve the device performance. The RF measurements performed allow us to obtain the S-parameters of the CPW. Those parameters describe the reflected and transmitted RF waves along the CPW line. Thanks to a de-embedding method, they can be converted to the effective resistivity and effective relative permittivity of the substrate (Fadel 2025).

In the present work, the experimental RF results are used mainly as qualitative indicators. Indeed, several process parameters changed during the experimental campaign, and a direct one-to-one comparison between all samples is therefore difficult.

4.5 Experimental observations

The samples analyzed in this section are based on the dopings presented in Table 3.1. They will be named with the same doping names, followed by a number to differentiate them as several samples have the same doping parameters.

4.5.1 Porous pocket morphology and penetration between PN regions

The first set of cross-sections is used to determine whether the porous front can reach the PN stopping layer and whether it can penetrate between the doped regions. This distinction is essential. All of the images presented in this Section are cross-sections in the x-z plane. A structure that stops the porous front too early is safe from an integration point of view, but it may leave a thick layer of bulk silicon below the CPW that could reduce RF performance. Inversely, a structure that allows the porous front to penetrate deeply between the PN regions could provide a better RF benefit, but it also increases the risk of locally piercing the stopping layer.

Figures 4.6 and 4.7 show a first example for the pn++ sample number 2 with $W_p = 1.5 \mu\text{m}$ and

$W_n = 2 \mu\text{m}$ with a square 3D pattern. The global cross-section shows that the porous pocket forms correctly from the back-side opening and progresses toward the front-side. However, the magnified image near the front-side indicates that the PSi does not significantly penetrate between the PN regions. The remaining silicon layer is at a constant value of approximately $1 \mu\text{m}$. This suggests that, for this geometry, the stopping structure is too effective. The current supply to the remaining P-type regions is strongly limited, either because the N-type barriers are sufficiently close together or because the depletion-induced bottleneck becomes dominant before the porous front can fully enter the patterned region.

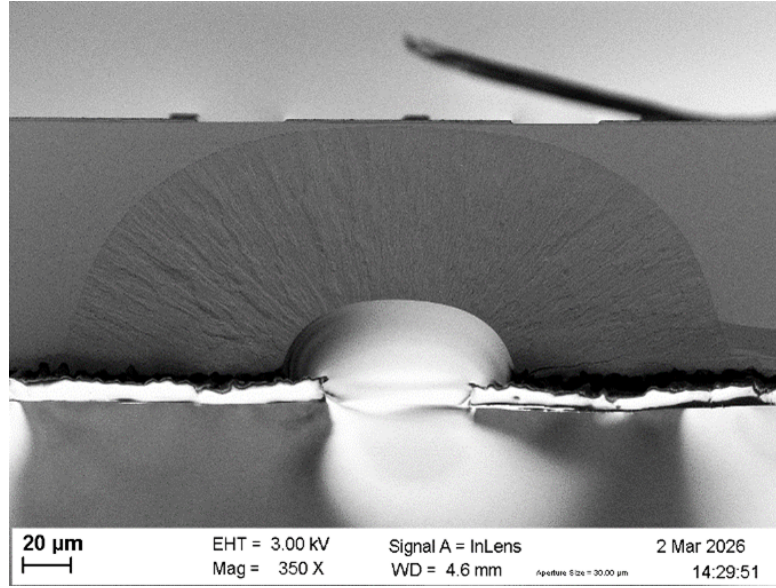


Fig 4.6. Cross-section in the x - z plane of a porous pocket obtained on $pn++$ wafer number 2 with a $W_p = 1.5 \mu\text{m}$, $W_n = 2 \mu\text{m}$ Square PN pattern.

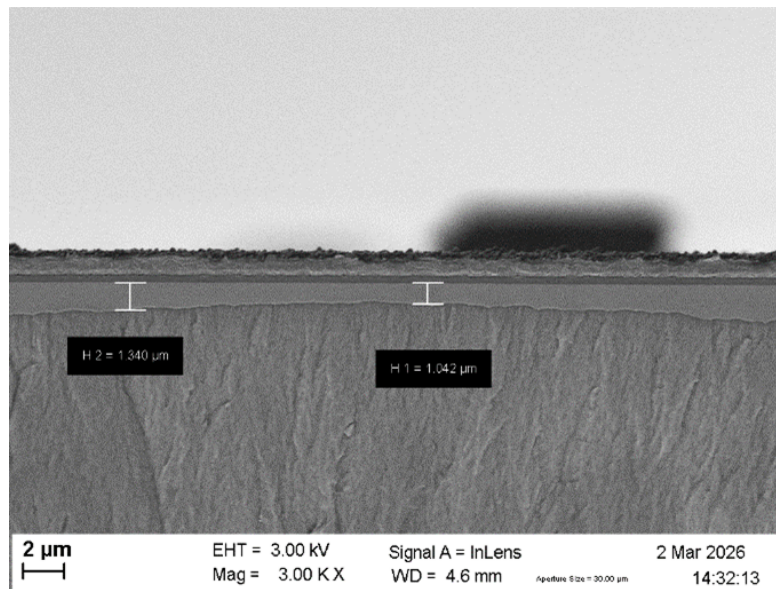


Fig 4.7. Cross-section in the x - z plane of a porous pocket obtained on $pn++$ wafer number 2 with a $W_p = 1.5 \mu\text{m}$, $W_n = 2 \mu\text{m}$ Square PN pattern, zoom on center of the pocket near SiO_2 layer.

Figures 4.8 and 4.9 show a second case for the same $pn++$ sample number 2 with $W_p = 3 \mu\text{m}$

and $W_n = 2 \mu\text{m}$ with a square pattern. In this case, the porous front reaches closer to the front-side patterned region and the magnified view shows a clearer penetration between the PN structures. The remaining silicon layer is oscillating between $1.5 \mu\text{m}$ and 400 nm . Compared with the previous case, the stopping behavior is therefore less abrupt.

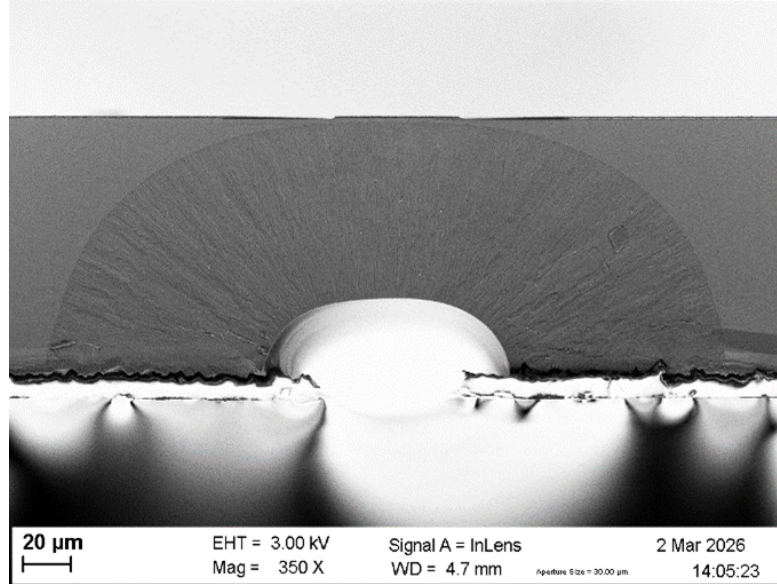


Fig 4.8. Cross-section in the x - z plane of a porous pocket obtained on the $pn++$ wafer number 2 with a $W_p = 3 \mu\text{m}$, $W_n = 2 \mu\text{m}$ Square PN pattern.

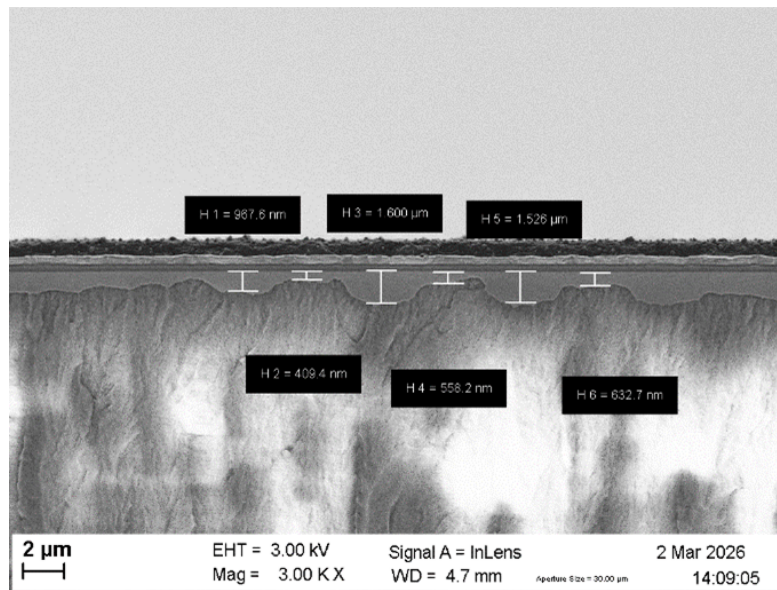


Fig 4.9. Cross-section in the x - z plane of a porous pocket obtained on the $pn++$ wafer number 2 with a $W_p = 3 \mu\text{m}$, $W_n = 2 \mu\text{m}$ Square PN pattern, zoom on center near SiO_2 layer

This comparison highlights the central trade-off introduced in Chapter 3. A more restrictive PN geometry increases the safety margin against over-porosification, but it can leave a larger residual silicon thickness. A less restrictive geometry may improve RF performance by allowing deeper PSi penetration, but it reduces the margin before breakthrough. The experimental cross-sections therefore provide the first qualitative validation that the PN dimensions can

tune the compromise between stopping robustness and RF usefulness.

As the porosification is isotropic, one could think that the point where the front is the closest to the SiO_2 layer is right above the opening. It is however shown in Figures 4.10, 4.11, and 4.12 that the remaining part at the edge of the pocket is only 300 nm while it is oscillating between 300 nm and 1.3 μm at the center. So the porous is closer to the SiO_2 on the edge of the pocket. These images come from the n++ wafer number 2 for the $W_p = 4 \mu m$, $W_n = 2 \mu m$ horizontal line pattern. The global cross-section shows the full porous pocket, while the magnified views compare the center and the edge of the region located close to the front-side.

This could seem counter-intuitive at first sight but, in fact, this type of non-uniform residual layer is consistent with the "geometric effect" described by Tuyaerts *et al.* (2026). In that work, the PSi did not fully reach the etch-stop layer everywhere: the remaining unporosified silicon was thicker at the center of the pocket than near the edge. The effect was attributed to the increased electrical resistance encountered by the current as the porous pocket approaches the etch-stop layer. Near the end of the process, the remaining crystalline silicon path becomes narrow, reducing the available cross-section for current flow and making it more difficult to supply the center of the pocket. The same mechanism is observed in some of these PN stopping-layer experiments. As the porous front approaches the front-side region, the current must pass through a reduced and increasingly non-uniform silicon volume.

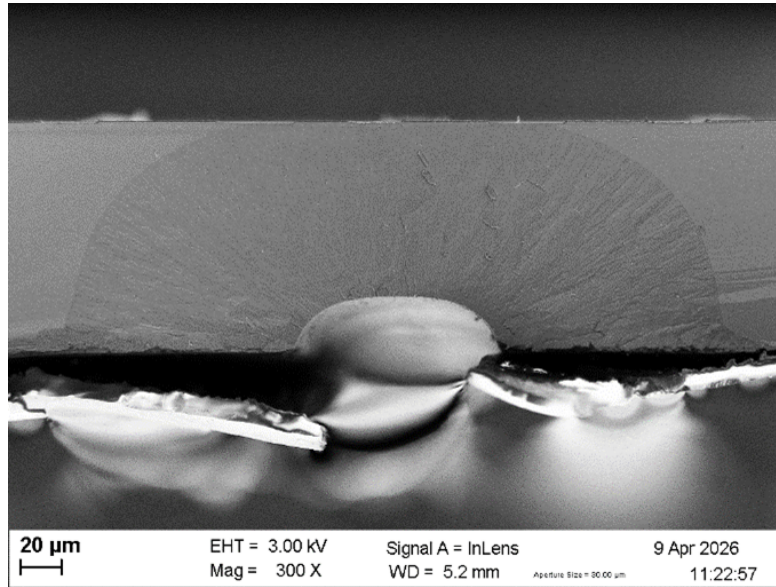


Fig 4.10. Cross-section in the x-z plane of a porous pocket obtained on the pn++ wafer number 4 with a $W_p = 4 \mu m$, $W_n = 2 \mu m$ Horizontal lines PN pattern.

The observation of the geometric effect is very relevant in the context of the RF performance as the remaining unporosified region right below the center of the pocket is also located right below the CPW, where the RF fields are strongest. This remaining conductive volume can therefore still contribute to substrate losses.

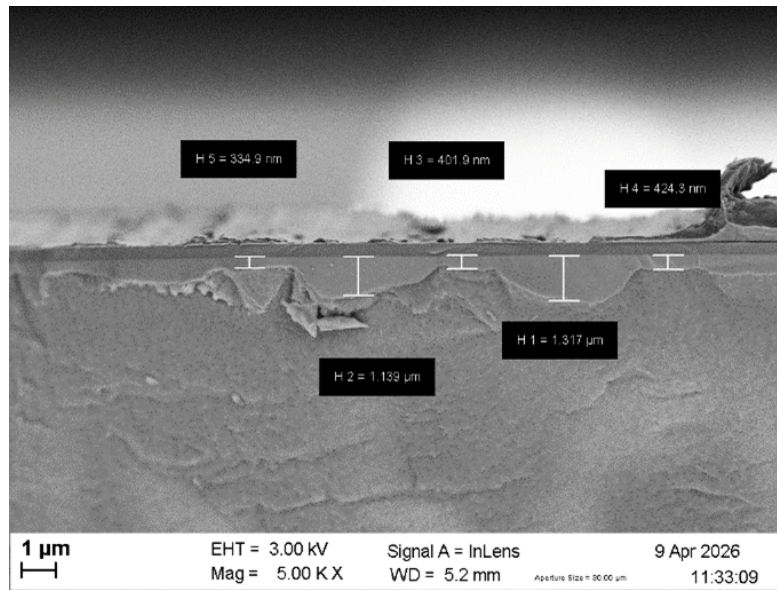


Fig 4.11. Cross-section in the x - z plane of a porous pocket obtained on the $pn++$ wafer number 4 with a $W_p = 4 \mu\text{m}$, $W_n = 2 \mu\text{m}$ Horizontal lines PN pattern, zoom on center near SiO_2 layer

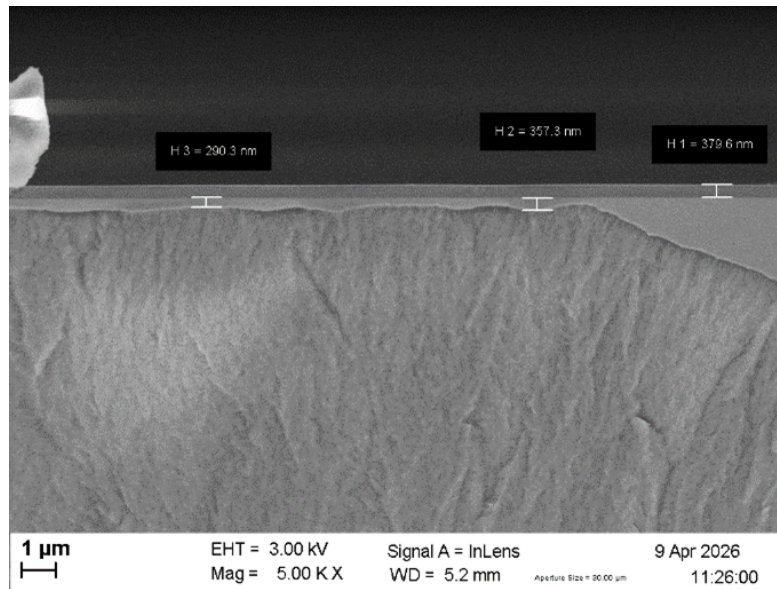


Fig 4.12. Cross-section in the x - z plane of a porous pocket obtained on the $pn++$ wafer number 4 with a $W_p = 4 \mu\text{m}$, $W_n = 2 \mu\text{m}$ horizontal lines PN pattern, zoom on edge near SiO_2 layer

4.5.2 3D geometry effects

The previous cross-sections revealed non-uniformity through the width of the pocket. A second type of non-uniformity appears along the longitudinal direction (y-axis) of the porous opening. The top-views in this Section are all in the x-y plane. Figure 4.13 shows that the porous region is wider near the end of the pocket than in the central part. Since the porosification is approximately isotropic, a larger visible width in top-view indicates that this region is receiving more current than the other.

This behavior is attributed to the finite length of the opening and of the back-side metal grid. The ends of the pocket can receive a different current density because they are the least resistive current path for a bigger part of the grid, as shown in Figure 4.15. This leads to a locally faster porosification. The same result is observed in Figure 4.14, a top-view of wafer pn++ number 2 with $W_p = 3 \mu\text{m}$, $W_n = 4 \mu\text{m}$ square pattern.

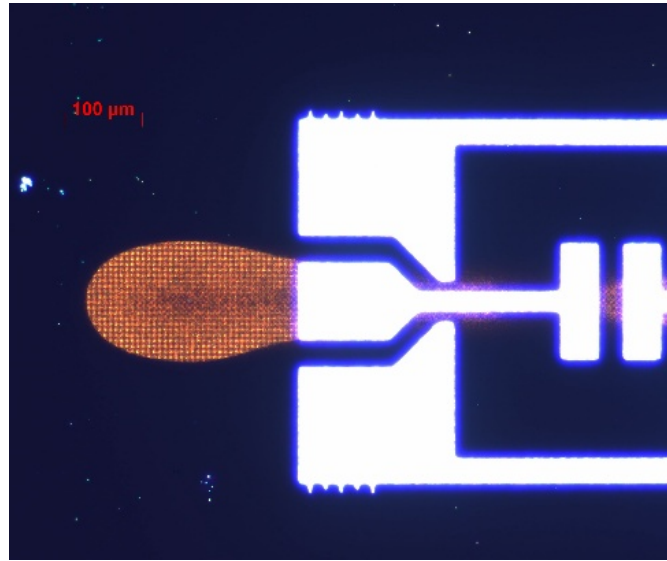


Fig 4.13. Top-view in the x-y plane of the porous pocket at the edge of the CPW, wafer pn++ number 2, $W_p = 5 \mu\text{m}$, $W_n = 2 \mu\text{m}$ Square pattern. The PSi is in orange and the CPW in white. The PSi pocket is wider at the extremity.

These observations support two conclusions. First, the PN pattern is able to affect the local porosification behavior, since changing the PN dimensions modifies the penetration of PSi near the front-side. Second, the stopping-layer behavior cannot be interpreted independently of the macroscopic porous-pocket geometry. The finite length of the opening, the shape of the metallic grid, and the access resistance through the remaining silicon all contribute to the final front shape.

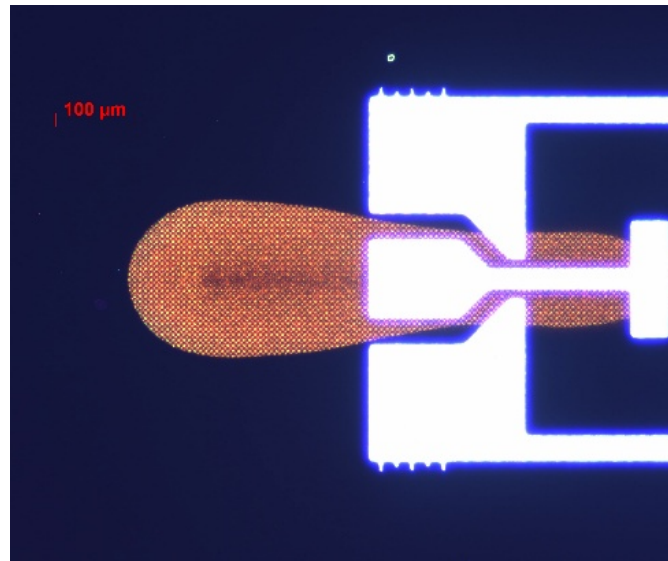


Fig 4.14. Top-view in the x - y plane of the porous pocket at the edge of the CPW, wafer pn^{++} number 2, $W_p = 3 \mu\text{m}$, $W_n = 4 \mu\text{m}$ Square pattern. The PSi is in orange and the CPW in white. The PSi pocket is wider at the extremity.

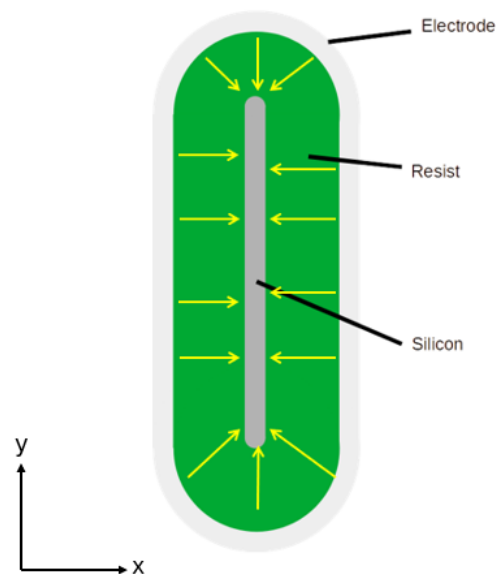


Fig 4.15. Schematic top-view of the back-side opening with highlighted current paths in yellow

4.5.3 RF measurements

The RF measurements provide complementary information to the cross-sectional observations. The objective is to evaluate whether the PSi region actually improves the electrical behavior of the substrate below the CPW structures. In principle, better RF performance is expected when the PSi extends sufficiently close to the CPW field region and when the remaining conductive silicon volume is minimized. The PN stopping layer must therefore allow enough PSi penetration while still protecting the front-side structures.

The experimental RF results shown in Figure 4.16 suggest that some samples, in particular the pn+ and pn++ candidates, can provide improved performance. This would fit with the fact that, with those dopings, the p-type regions are porosified more easily and so the unporosified silicon remaining is smaller. However, these results must be interpreted carefully. During the experimental campaign, changes in the porosification process were introduced, like the porosification time for example. As a result, the RF differences between samples cannot be attributed only to the PN geometry. The RF measurements should therefore be used together with the physical cross-sections rather than as a standalone ranking of the candidates. No

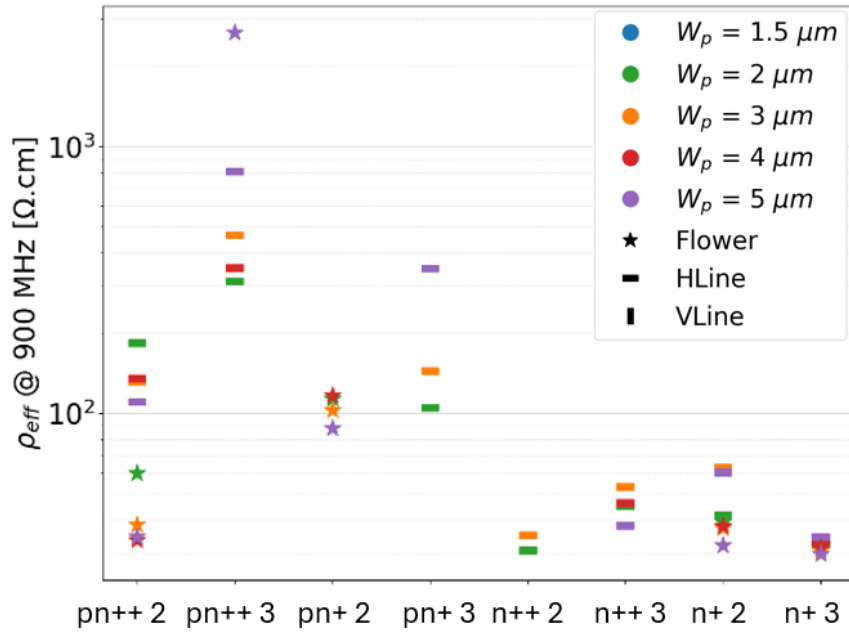


Fig 4.16. Effective resistivity of the substrate at 900 MHz extracted from the CPW measurements. Results of samples are displayed by columns. The color shows the width of the P-type region and the shape of the symbol, the 3D pattern used. Porosification times (not shown) vary between samples and geometries.

single monotonic trend with W_p can be extracted from all samples. In some cases, larger W_p values lead to higher effective resistivity, which is consistent with deeper PSi penetration between the PN regions and a smaller remaining conductive silicon volume. In other cases, smaller widths provide better results, possibly because when the porous front is stopped

slightly earlier, the PN depletion barriers are the effective factor. The ratio of depletion width compared to the total length is higher for smaller PN regions. This confirms that the RF response is controlled by a combination of porous penetration depth, residual silicon thickness, PN depletion effects, and process variations.

Finally, it is hard to get a comparison between the different patterns as there is only three samples for which two configurations are available but it seems, based on them, that the results for the horizontal lines are better but not always by a lot. This may induce that the non-idealities created at the lithography reduce the efficiency of the PN junctions. This still has to be investigated.

The experimental results are therefore consistent with the qualitative design rule developed in Chapter 3: the optimal stopping layer is not necessarily the most protective one. A structure that leaves too much bulk silicon below the CPW can remain safe from a process point of view but provide limited RF benefit. Conversely, a structure that allows deeper penetration of PSi can improve RF behavior but must be controlled to avoid complete breakthrough. The best candidate must balance these two constraints.

Looking at the quantitative values of the ρ_{eff} obtained, we can see that the best results obtained are around 1 k Ω cm. This result is close the 3 k Ω cm obtained by Tuyaerts *et al.* (2026) with the SOI post-process PSi. Therefore, it seems reasonable to think that, with improvements of the uniformity of the non-porosified layer, same range of effective resistivity could be achieved with bulk post-process PSi.

4.6 Conclusion

This chapter presented the experimental implementation of PN-based stopping structures for post-process PSi integration in bulk-compatible substrates. The two-dimensional PN candidates introduced previously are converted into periodic three-dimensional layouts, including line patterns, square patterns, and modified square patterns. These layouts are combined with front-side CPW structures and processed through a back-side porosification flow involving wafer bonding, thinning, back-side metallization, resist patterning, electropolishing, and HF-based porosification.

The cross-sectional observations show that the PN geometry can affect the penetration of the porous front near the front-side region. Narrow or strongly blocking patterns can prevent significant penetration between the doped regions, providing a strong stopping behavior but leaving a larger residual silicon thickness. Other geometries allow deeper penetration between PN structures, which is more favorable for RF performance but less conservative from an etch-stop perspective.

The experimental images also reveal important non-uniformity effects. In particular, the resid-

ual silicon thickness in the x-z plane cross-section can be larger in the center of the pocket than near the edges, consistent with the geometric effect previously reported by Scheen, Tuyaerts, Van Overmeere, *et al.* (2025). This effect originates from the increasing access resistance encountered by the current as the porous pocket approaches the front-side stopping layer. In addition, some samples show longitudinal non-uniformity effects along the y axis that cannot be described by a two-dimensional model as they are linked to the 3D geometry of the opening and the electrode.

Finally, the RF performance of the sample seems to be influenced by the porosification, as expected. The 2D candidates that allow more penetration tends to increase ρ_{eff} . The best result obtained of 1 k Ω cm confirms that resistivity similar to the one obtained with SOI post-process PSi can be achieved in bulk technologies with a good control of the porosification.

These observations motivate the numerical work presented in the following chapters. The 2D simulations will first be used to establish a controlled moving-boundary model and to study the influence of local resistivity profiles. The 3D simulations will then be required to capture the macroscopic geometry effects observed experimentally, especially the non-uniform current distribution and the resulting non-uniform porous-front evolution.

Chapter 5

2D Simulations of porosification

This chapter presents the two-dimensional COMSOL model developed to study the post-process porosification of silicon substrates. This model has two purposes. First, it provides a simplified numerical environment in which the main features of the porosification process can be tested at a reduced computational cost. Second, it allows the influence of non-uniform substrate resistivity to be evaluated before moving to full three-dimensional simulations. In this Section, we will test the PN stopping-layer candidates introduced in Chapter 3 by introducing the resistivity maps extracted.

The model is a macroscopic current-distribution model. It is not intended to describe the formation of individual pores at the nanometer scale, nor to reproduce the absolute experimental porosification time. Instead, it describes the evolution of an electrolyte-filled porous region whose interface moves according to the local electrochemical current density. The simulated time is therefore used mainly as an evolution parameter, while the shape of the porous pocket, the current distribution and the sensitivity to local resistivity variations are the quantities of interest.

The chapter is organized as follows. Section 5.1 describes the geometry, physical assumptions, boundary conditions, mesh, and solver strategy. Section 5.2 presents the results obtained on a uniformly resistive silicon substrate, which are used as a first consistency check of the model. Finally, Section 5.3 discusses the introduction of resistivity profiles extracted from Silvaco Atlas simulations. The results between the different candidates will be compared and the numerical limitations encountered when applying the moving-boundary model to sharp variations of resistivity due to the PN profiles will be provided.

5.1 Introduction of the simulation model

5.1.1 Geometry and simulated domains

The simulated geometry represents a two-dimensional cross-section in the x-z plane of the back-side porosification setup. It contains three main domains, displayed in Figure 5.1: the silicon substrate in dark gray, the electrolyte above the back-side opening in light blue, and the initial pre-etched cavity in light gray. The silicon substrate is $100\text{ }\mu\text{m}$ thick. The electrolyte domain is $550\text{ }\mu\text{m}$ wide and $600\text{ }\mu\text{m}$ high, while the silicon domain is slightly wider, with a total width of $600\text{ }\mu\text{m}$. The back-side opening has a width of $50\text{ }\mu\text{m}$. The initial cavity, produced experimentally by electropolishing, is modeled as a $25\text{ }\mu\text{m}$ deep electrolyte-filled region with a lateral underetch of $10\text{ }\mu\text{m}$ on each side of the opening. Its initial width is therefore $70\text{ }\mu\text{m}$. As the electropolishing is isotropic, the lateral underetch should have been set to $25\text{ }\mu\text{m}$. It should then be changed in further works but it is likely to not change the results presented here.

The resist that is located between the electrolyte and the silicon is an insulator between the two media in the real experiments. In the simulations, the resist is thus omitted and the space between the two is out of domain. Furthermore, the corners of the resist above the opening are rounded. This choice was made to avoid current crowding that would have been caused by corners.

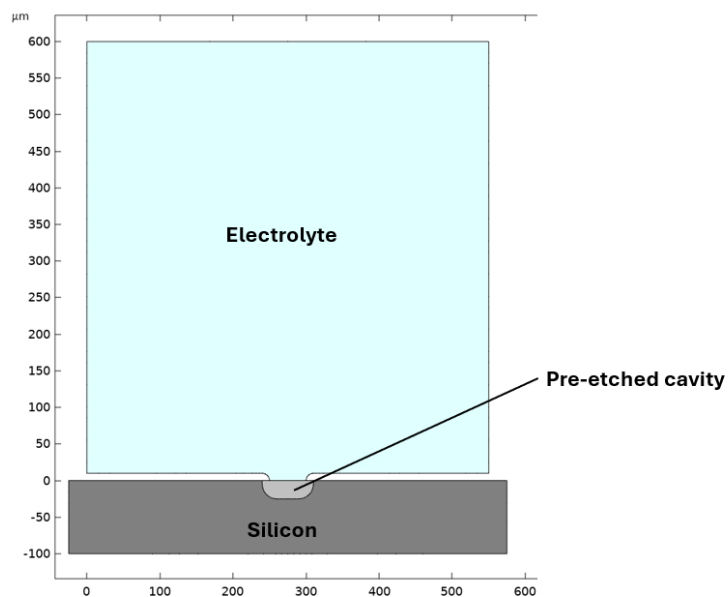


Fig 5.1. Two-dimensional COMSOL geometry used for the porosification simulations. The model includes the silicon substrate, the electrolyte domain and the initial electropolished cavity that acts as the starting porous region.

In the real sample, the pre-etched cavity corresponds to silicon removed during the electropolishing step and subsequently filled with electrolyte. In the numerical model, it is just considered as the electrolyte. However, as the simulation progresses, it is the boundary between the silicon wafer and the cavity that moves into the substrate. This electrolyte region is

therefore treated as the initial PSi region. The newly formed PSi is in fact represented as an extension of the electrolyte-filled initial cavity. This approximation avoids explicitly resolving the nanometric pore network creation while preserving the macroscopic role of PSi as an electrolyte-filled path connecting the external solution to the active reaction front.

As mentioned at the beginning of the chapter, the use of a two-dimensional model implies an invariance in the out-of-plane direction. The results therefore represent the behavior of an extruded opening rather than the full three-dimensional growth of a finite porous pocket. This simplification is acceptable for the first stage of model development because it greatly reduces the computational cost and allows the impact of parameters to be studied more easily. However, it also means that effects related to finite pocket length, lateral current spreading in the third direction and true three-dimensional PN layouts must be addressed separately in later simulations.

5.1.2 Physical model and assumptions

The electrochemical problem is modeled using the Primary Current Distribution interface of the COMSOL Electrochemistry Module. This formulation solves the current distribution in the electrolyte and in the conducting silicon domain, while neglecting concentration gradients and activation overpotentials. The model therefore assumes that the local interface motion is only controlled by the electrical current distribution. This is consistent with the objective of the present simulations, which is to study how the geometry and the substrate resistivity profile redistribute the current reaching the porosification front.

This assumption is also reinforced by the experimental process. In practice, the porosification current is interrupted periodically to allow the electrolyte to replenish the reactive species at the porous front. In the present model, such pauses are not explicitly simulated. As a result, the model should not be used to predict the absolute porosification time, but rather to compare the relative evolution of different geometries and resistivity distributions.

The Primary Current Distribution interface solves the current-conservation problem in both the electrolyte and the silicon domain. In the electrolyte, the current density $\mathbf{i}_l$ and the electrolyte potential ϕ_l are related by

$$\nabla \cdot \mathbf{i}_l = Q_l, \quad \mathbf{i}_l = -\sigma_l \nabla \phi_l, \quad (5.1)$$

with σ_l the electrolyte conductivity. In the silicon domain, the current density $\mathbf{i}_s$ and the electric potential ϕ_s are governed by

$$\nabla \cdot \mathbf{i}_s = Q_s, \quad \mathbf{i}_s = -\sigma_s \nabla \phi_s. \quad (5.2)$$

No volumetric current source is included, so $Q_l = Q_s = 0$. The current is therefore conserved inside each domain and is exchanged only through the electrochemical interface.

For the uniform-substrate simulations, the silicon resistivity is set to $10 \Omega\text{cm}$, corresponding to a standard wafer resistivity. The electrolyte conductivity is set to 3.7 Sm^{-1} ¹. When PN stopping-layer candidates are studied, the silicon conductivity is no longer uniform. Instead, it is obtained by interpolation in a spatially dependent resistivity map extracted from TCAD simulations:

$$\sigma_s(x, y) = \frac{1}{\rho_{\text{Atlas}}(x, y)}. \quad (5.3)$$

In that case, the PN junctions are not solved as active semiconductor junctions during the porosification simulation. Their effect is introduced through the fixed resistivity map. As mentioned before, an important modeling limitation is that the possible changes of the depletion regions due to the potential at the porous interface getting closer are not recomputed dynamically. Another problem of the resistivity maps is that the N-doped regions are just seen as a low-resistivity region. The porosification could then be really fast in the region compared to the rest of the wafer whereas, in theory, the porosification should be significantly slowed down.

5.1.3 Electrode reaction and interface motion

The porosification equation happens at the interface of the silicon and the electrolyte and is driven by the presence of holes. The porosification reaction is therefore represented by an internal electrode surface reaction located at the boundary between the silicon and the electrolyte-filled cavity. This is the only boundary where silicon dissolution is allowed. The reaction uses silicon as the dissolving species, with a density of 2329 kg/m^3 and a molar mass of 28.09 g/mol . The number of participating electrons is set to $n = 2$ as the Si porosification process is a two-electron electrochemical dissolution reaction. The equilibrium potential is set to

$$E_{\text{eq}} = -0.5 \text{ V}, \quad (5.4)$$

following previous implementations of similar porosification models.²

The local reaction rate is written as

$$R_d = -\nu_d \frac{i_{\text{loc}}}{nF}, \quad (5.5)$$

where ν_d is the stoichiometric coefficient, i_{loc} is the local electrode current density, n is the number of electrons involved in the reaction and F is Faraday's constant. The interface condition between the silicon and electrolyte potentials is

$$\phi_s - \phi_l = E_{\text{eq}}. \quad (5.6)$$

¹Based on discussions with Thibault Fiasse

²Also based on discussions with Thibault Fiasse

The motion of the porosification front is handled by the Deformed Geometry interface coupled to the electrochemical reaction. The normal velocity of the moving interface is proportional to the local dissolution rate:

$$v_n = \frac{R_d M_{Si}}{\rho_{Si}}, \quad (5.7)$$

where M_{Si} and ρ_{Si} are the molar mass and density of silicon. These two relations make the link between the electrical and geometrical domains: regions receiving a larger normal current density advance faster. The result is that regions protected by the high-resistivity barriers advance more slowly.

The model therefore captures the feedback between geometry and current distribution. As the porous pocket grows, the shape of the Si/electrolyte interface changes, which modifies the current paths and consequently the local growth velocity at the next time step.

5.1.4 Boundary conditions

The main boundary conditions are summarized in 5.2. The upper boundary of the electrolyte is used as the counter-electrode and is fixed at $\phi_l = 0$ V (highlighted in green). A current density is imposed on the back-side grid contact region of the silicon (highlighted in orange). In the simulations presented here, the imposed current density is of the order of 10^3 A/m^2 . This value is not intended to reproduce the experimental current density quantitatively. It is chosen to obtain a numerically convenient interface displacement while preserving the qualitative current-redistribution mechanisms of interest. Furthermore, the values was changed several times through this work to accommodate with the convergence problems sometimes encountered.

Since the imposed current density is applied on a fixed electrode boundary, the total current remains constant during the simulation. As the porous interface grows, its surface increases. As a result, the average current density at the moving front decreases. In real experiments, the current density at the interface is aimed to remain constant in order to get a uniform porosification. For the simulations, the pores are not represented. The current density at the interface can then change without changing the electrical properties of the medium. Nevertheless, this decrease of current density leads to the progressive slow down of the simulated interface motion.

Periodic boundary conditions with equipotentiality are applied to the paired lateral boundaries, both for the electrolyte and the electrode (highlighted in purple). This choice represents the fact that the simulated geometry is only one die of the larger periodically repeated back-side geometry rather than an isolated finite wafer. All the external boundaries except the imposed electrode contact and the counter-electrode are treated as electrically insulating. This will impose that the current flows from one electrode to the other, passing by the Si/electrolyte interface. The counter-electrode itself is not explicitly modeled as a reacting surface, because

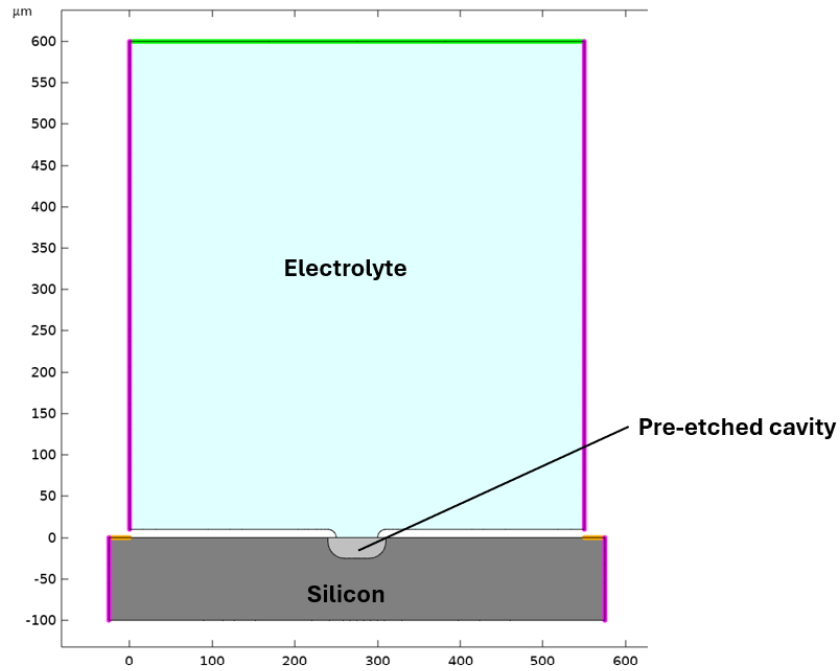


Fig 5.2. Boundary conditions used in the 2D COMSOL model. The top electrolyte boundary is in green, the back-side grid contact imposes the etching current density in orange, the lateral boundaries are paired using periodic conditions in purple, and the remaining boundaries are electrically insulating.

the present work focuses on the silicon dissolution front.

5.1.5 Mesh strategy

The geometry is meshed with triangular elements. Different mesh sizes are used in the different domains because the relevant spatial scales are not the same everywhere. A relatively coarse mesh is sufficient in most of the electrolyte, with mesh elements going to $50\ \mu\text{m}$, because only the large-scale potential distribution is needed. The mesh is refined near the Si/electrolyte interface and around the initial cavity, where the strongest current-density gradients and the moving boundary are located. The elements are there around $3\text{--}5\ \mu\text{m}$. This is displayed in Figure 5.3

In addition to the element size, the element quality is also important. Highly elongated elements can degrade the accuracy of the current-density calculation and slow down convergence. The mesh generation therefore aims to limit the element aspect ratio. Moreover, as the boundary displacement progressively deforms the mesh, automatic remeshing is enabled during the simulation to restore mesh quality when the deformation becomes too large. Figure 5.4 shows a remeshing performed as the elements in the initial cavity were too elongated and the mesh in the silicon wafer too constricted as a consequence of the moving boundary.

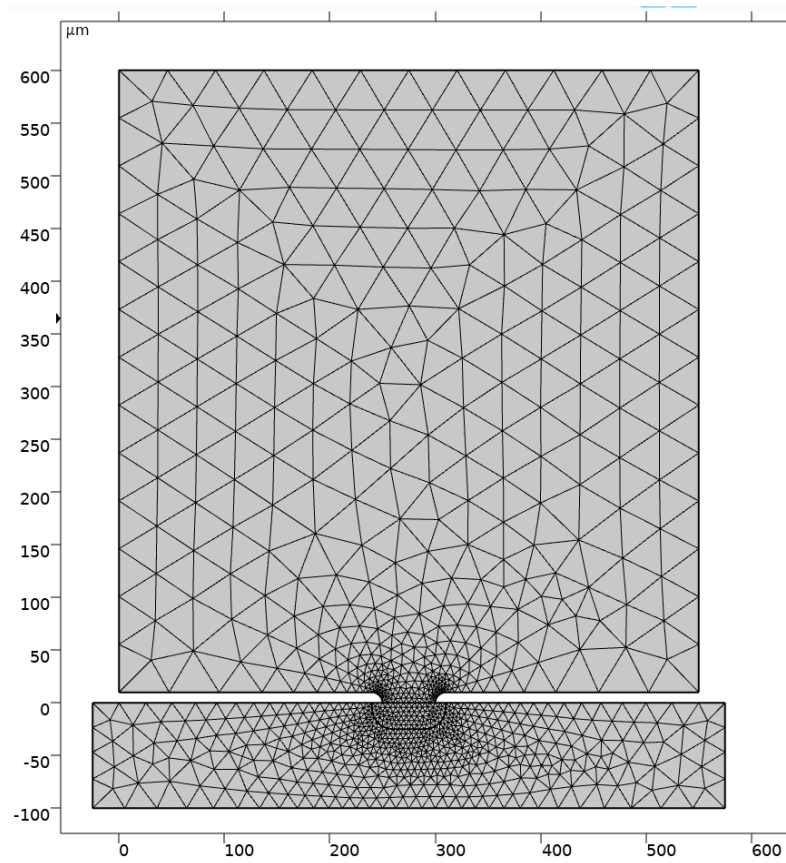


Fig 5.3. *Triangular mesh used for the 2D porosification model.*

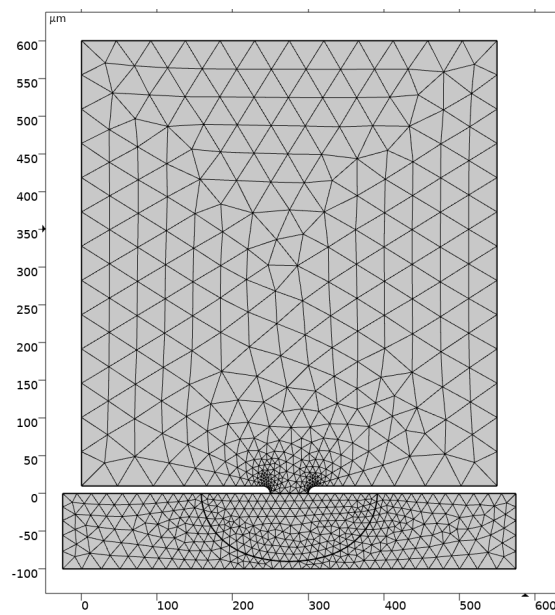


Fig 5.4. *Remeshing performed because of the interface displacement during a simulation*

5.1.6 Solver strategy

The simulation is solved in two stages. First, a current-distribution initialization step is performed on the initial geometry. This step computes the initial potential and current-density fields without moving the interface. The resulting solution is then used as the initial condition for the time-dependent study.

The time-dependent step solves the coupled current-distribution and deformed-geometry problems. At each step, the electrical problem determines the local current density at the Si/electrolyte interface. The electrode reaction then converts this current density into a normal velocity of the interface following the Equation 5.5 and Equation 5.7 and the deformed-geometry interface finally updates the shape of the porous pocket. As said before, the automatic remeshing is enabled so that the mesh can be rebuilt when the deformation caused by the moving boundary becomes too large.

The position of the interface, the current density, and the potential values are extracted from the simulations at every time step and will be useful to validate the performance model and then compare the different resistivity patterns introduced in the simulations.

As already mentioned, the time variable used in the simulations is not interpretable as it is not calibrated physically. The simulation time is then normalized as a variable τ , ranging from 0 for the initial geometry to 1 for the final available time step.

5.2 Results on uniform resistivity wafer

The first simulations are performed on a uniform silicon substrate with a resistivity of $10 \Omega\text{cm}$. This reference case is used to verify that the model behaves consistently before introducing non-uniform PN resistivity profiles. In the absence of local resistivity variations, the current distribution and the interface motion should be governed by the imposed boundary conditions and the porous region growth should be isotropic.

Figure 5.5 shows the solution obtained at $\tau = 0$. The color scale represents the electrolyte potential, while the black curves correspond to current-density streamlines. The current lines converge toward the initial electropolished cavity, where the silicon/electrolyte interface is electrochemically active. The largest potential gradients are located close to this interface and the opening, indicating the strongest current densities. This is expected as the cross-section of the opening is tighter. Away from the opening, the potential field becomes smoother as current lines distribute themselves in the wider electrolyte and so the current density decreases.

The evolution of the interface is shown in Figure 5.6. The porous pocket remains symmetric with respect to the center of the back-side opening. This is the expected behavior for a uniform-resistivity substrate, since no lateral component is introduced in the silicon. The front shape is

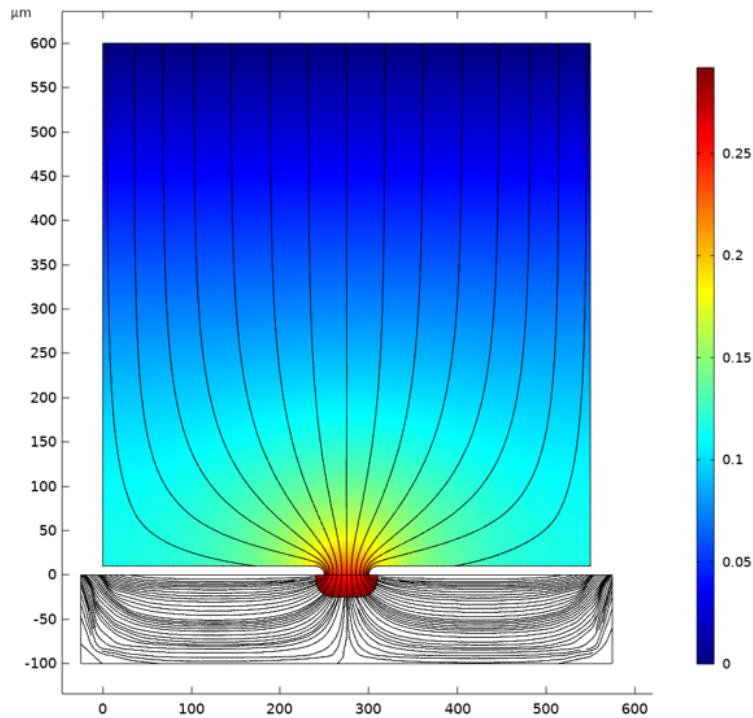


Fig 5.5. Initial solution for the uniform-resistivity substrate at $\tau = 0$.

also nearly isotropic: the porous region grows both vertically and laterally from the initial cavity, giving a rounded interface. This observation provides a first consistency check of the moving-boundary model. It confirms that the model does not introduce an artificial preferential direction in the absence of PN patterns.

It is interesting to see that, in Fig 5.6 (b), the region close to the lower boundary exhibits a smaller potential gradient and fewer current streamlines. This indicates that only a limited fraction of the imposed current reaches this part of the interface as the potential gradient and the current are proportional. Therefore, the local interface velocity is lower, which is consistent with the slowing down of the front as it approaches the boundary. This behavior aligns with the imposed insulating boundary condition.

Another useful consistency check is the potential distribution in the silicon domain. Figure 5.7 shows the silicon potential at $\tau = 0.31$. Unlike an ideal metallic electrode, the silicon substrate is not equipotential as it has a finite resistivity. The current injected from the electrode must spread laterally through the remaining silicon before reaching the active interface. This produces an ohmic drop in the solid phase, visible as a spatial variation of ϕ_s . The arrows indicate that the current converges from the grid region toward the porous pocket. The map shows a continuous potential drop from the current-injection region toward the active interface, which is coherent with those arrows.

Overall, the uniform-resistivity case validates the qualitative behavior of the 2D model. The front remains symmetric, the porous pocket grows in a nearly isotropic way, and the potential

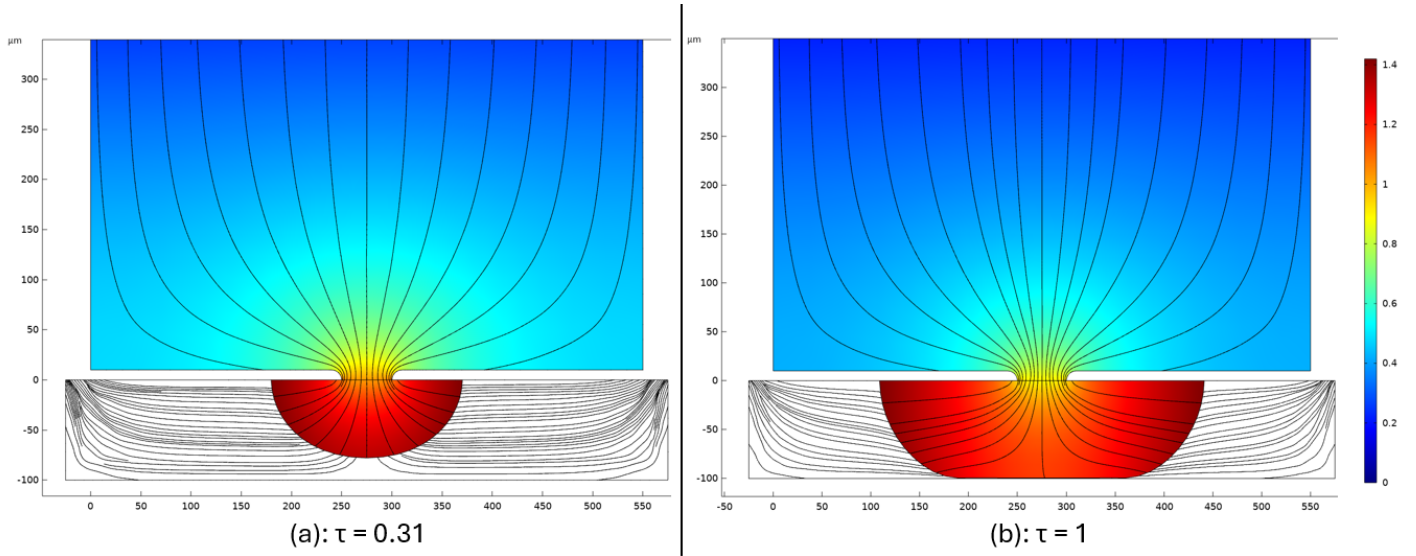


Fig 5.6. Evolution of the Si/electrolyte interface for the uniform-resistivity substrate at two normalized times at $\tau = \{0.31, 1\}$.

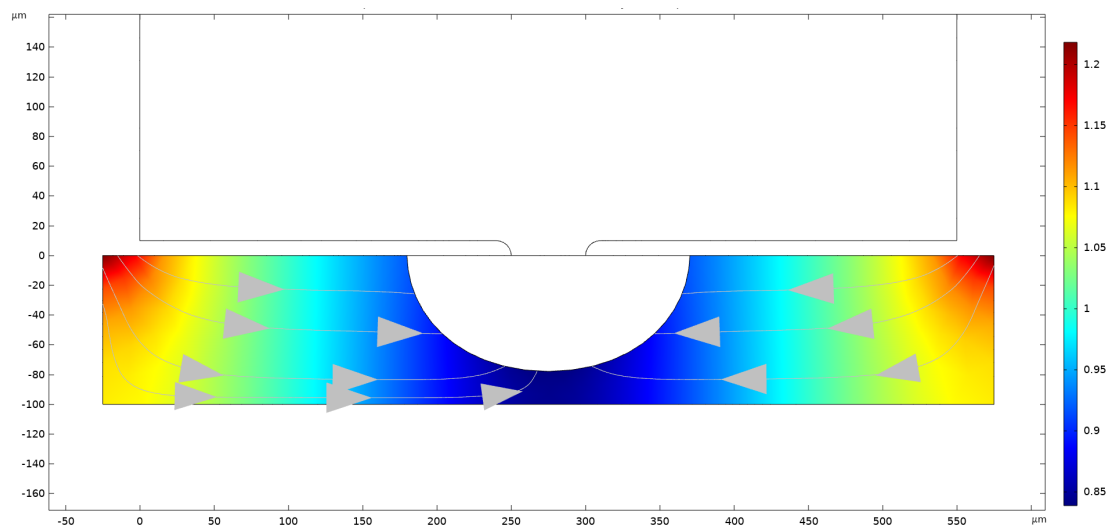


Fig 5.7. Silicon potential at $\tau = 0.31$ for the uniform-resistivity substrate. The arrows indicate the current direction in the silicon.

and current fields are consistent with the imposed current path. This case is therefore used as a reference for interpreting the simulations with PN resistivity profiles and the behavior of the etch-stopping layers.

5.3 Results with resistivity profiles from Silvaco

After validating the model on a uniform substrate, the next step is to introduce the PN stopping-layer candidates. The resistivity profiles obtained from Silvaco Atlas are imported into COMSOL as spatially dependent tables of $\rho(x, y)$. COMSOL then interpolates these values over the silicon domain and uses them to define the local conductivity through Equation 5.3. The objective is to evaluate whether the high-resistivity regions associated with the PN patterns can slow down or stop the moving porous front.

5.3.1 Numerical difficulty of directly importing sharp resistivity profiles

The first simulations using the raw Silvaco resistivity maps revealed an important numerical limitation. The resistivity profiles contain very sharp variations, especially near the depleted regions around the PN junctions. Since COMSOL solves the problem on a finite-element mesh, the resistivity field is only sampled at the mesh nodes and interpolated inside each element. If the mesh is too coarse compared with the characteristic width of the high-resistivity regions, those narrow barriers are likely to be missed. For this reason, a refined mesh was created with element sizes below $0.5 \mu\text{m}$ around both the PN layer and the moving interface, as shown in Figure 5.8.

This refinement improved the spatial resolution but did not fully solve the problem. Figure 5.9 and Figure 5.10 show the final available step of a simulation on the doping candidate pn++ with $W_p = 4 \mu\text{m}$ and $W_n = 2 \mu\text{m}$ before numerical failure. The interface remains mostly rounded and is only weakly affected by the PN pattern. In addition, the current streamlines still extend close to the lower boundary of the silicon domain, whereas a stronger blocking effect would be expected if the high-resistivity barriers were fully resolved.

The remaining difficulty is believed to be linked to the combination of sharp resistivity variations and remeshing. During the simulation, the interface moves and the mesh is periodically rebuilt to guarantee that the elements respect the size conditions. When new mesh nodes are created, they can be placed on different parts of the resistivity map compared with the previous mesh. A node that was previously located in a low-resistivity region can therefore be moved into a high-resistivity region, or conversely. Because the imported maps contain resistivity contrasts over several orders of magnitude (from $0.1 \Omega\text{cm}$ to $1 \text{ M } \Omega\text{cm}$), these remeshing events can introduce abrupt changes in the local conductivity matrix and lead to solver convergence failure. The issue is therefore not only the spatial resolution of the initial mesh, but also the

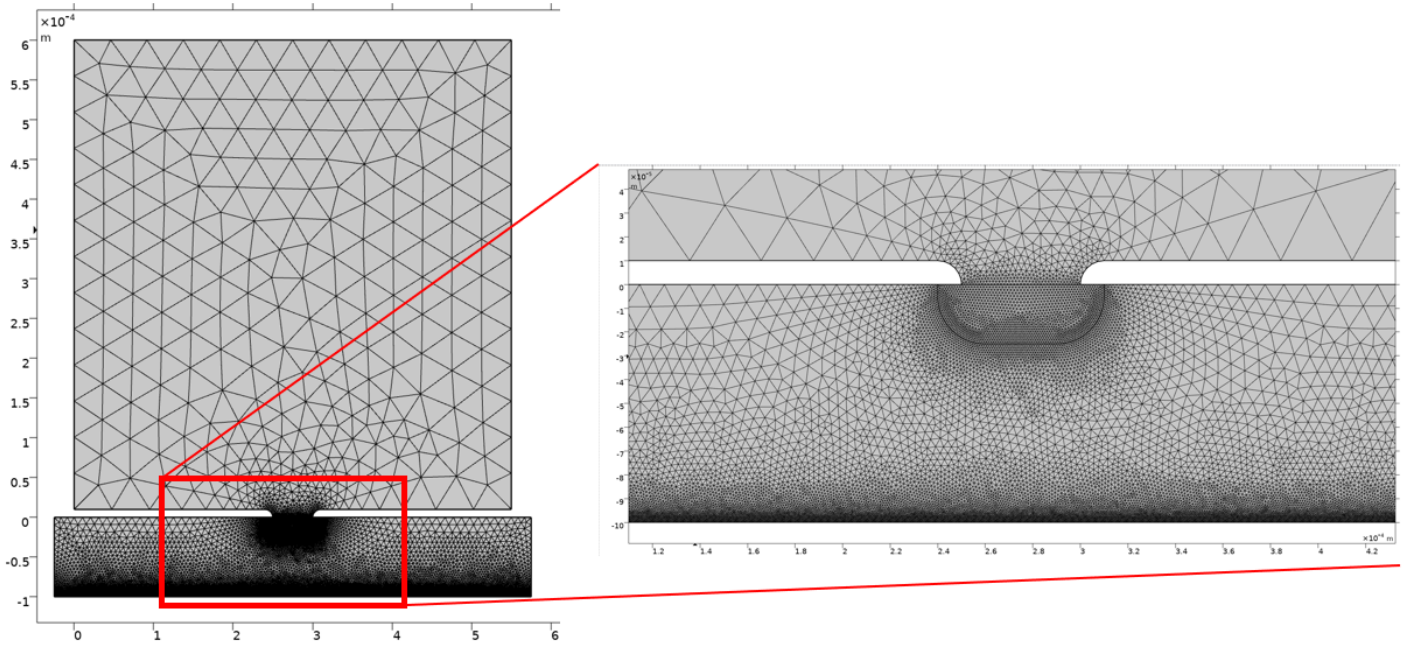


Fig 5.8. Refined mesh used to resolve the imported PN resistivity profiles. The mesh is refined both around the moving interface and the front-side PN regions.

compatibility between a highly discontinuous material map and a moving-mesh simulation.

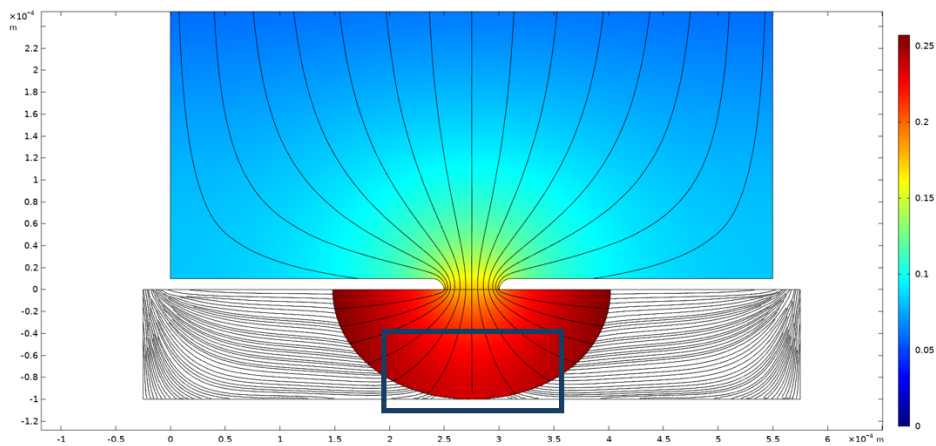


Fig 5.9. Solution obtained with the raw imported resistivity map shortly before solver failure. The blue rectangle indicates the region shown in Figure 5.10.

5.3.2 Simplified high-resistivity representation of N-type regions

To obtain stable simulations while preserving the main physical role of the PN patterns, the resistivity values inside the N-type regions were replaced by 1 k Ω cm. This choice is a modeling approximation. It is motivated by the fact that N-type silicon is not expected to porosify as easily as P-type silicon under the same anodization conditions, because holes are minority carriers in N-type regions. Assigning a high resistivity to the N regions therefore provides an

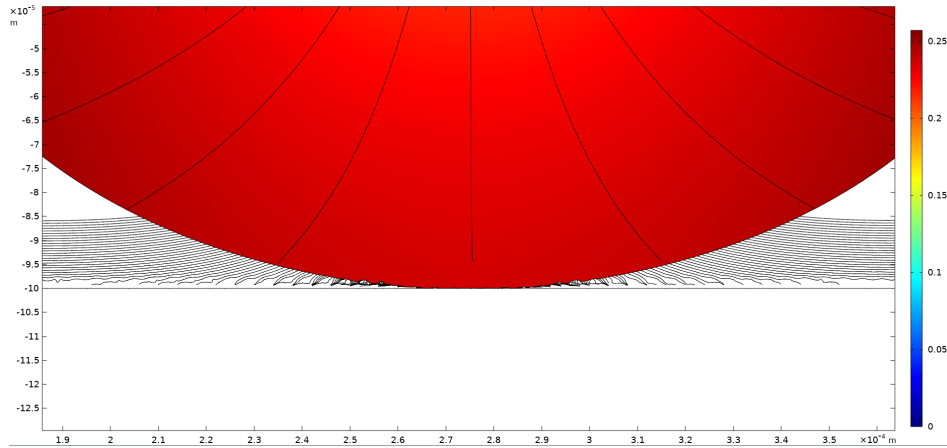


Fig 5.10. Zoom of the moving interface for the simulation shown in Figure 5.9.

effective way to represent their reduced ability to feed the porosification reaction. It must then absolutely not be interpreted as the physical resistivity of the implanted N-type silicon. Furthermore, it will simplify the computations. Instead of resolving very narrow and abrupt depleted barriers from the raw map, the simulation uses a more robust effective contrast between P-type paths and N-type blocking regions. The obtained resistivity map is shown in Figure 5.11.

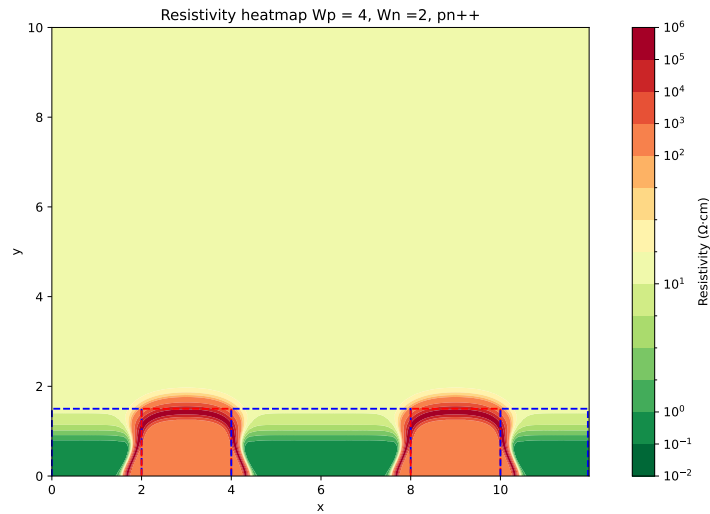


Fig 5.11. Modified resistivity map used for the pn++ candidate with $W_p = 4 \mu\text{m}$ and $W_n = 2 \mu\text{m}$, after replacing the N-type regions by $1 \text{ k}\Omega\text{cm}$.

With this modified resistivity map, all the candidates introduced in Chapter 3 were used as inputs for the porosification simulations. The comparison is based on the shape of the porous region and on the residual non-porosified silicon thickness at the final simulated time, $\tau = 1$. This second quantity corresponds to the vertical distance between the porous front and the front-side of the substrate. A smaller residual thickness indicates a deeper porosification. It is also interesting to look at the oscillations of this thickness to see whether the zones between the N-type regions were deeply porosified.

Some simulations stopped before reaching $\tau = 1$, typically between $\tau = 0.87$ and $\tau = 1$, because of convergence limitations. These cases are still included in the comparison when the final available interface is sufficiently close to the end of the simulation, but the corresponding conclusions are to be interpreted cautiously.

5.3.3 Effect of the PN patterns on the Si/electrolyte interface

Figure 5.12 and Figure 5.13 show the final solution obtained for the pn++ candidate with $W_p = 4 \mu\text{m}$ and $W_n = 2 \mu\text{m}$. The porous front is no longer perfectly smooth. Instead, it exhibits local oscillations following the PN pattern. These oscillations are expected: the current cannot easily penetrate the high-resistivity N-type regions. Since the interface velocity is proportional to the local current density, the front advances faster below the more conductive paths and more slowly below the blocking regions. The zoom in Fig 5.13 also shows that the current avoids the high-resistivity regions as the streamlines seems to hop above those. This confirms the insight we could get from the modified resistivity map in Fig 5.11: the PN pattern is now visible in the current distribution and in the final shape of the porous front.

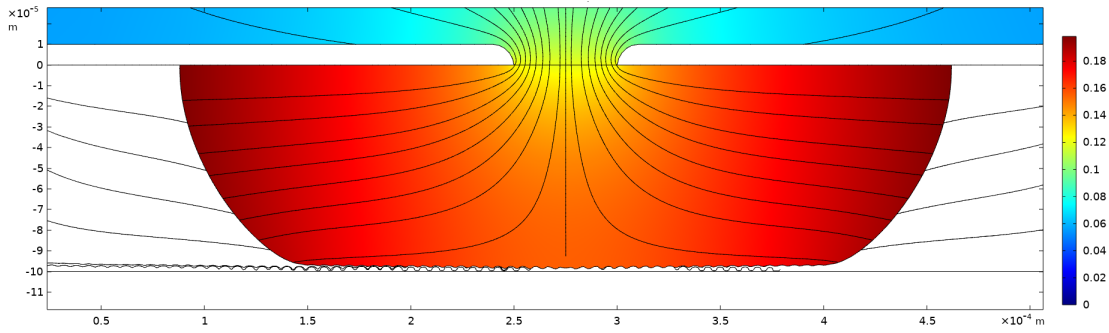


Fig 5.12. Final solution for the pn++ candidate with $W_p = 4 \mu\text{m}$ and $W_n = 2 \mu\text{m}$ at $\tau = 1$. The PN pattern modifies the current distribution and produces oscillations of the porous front.

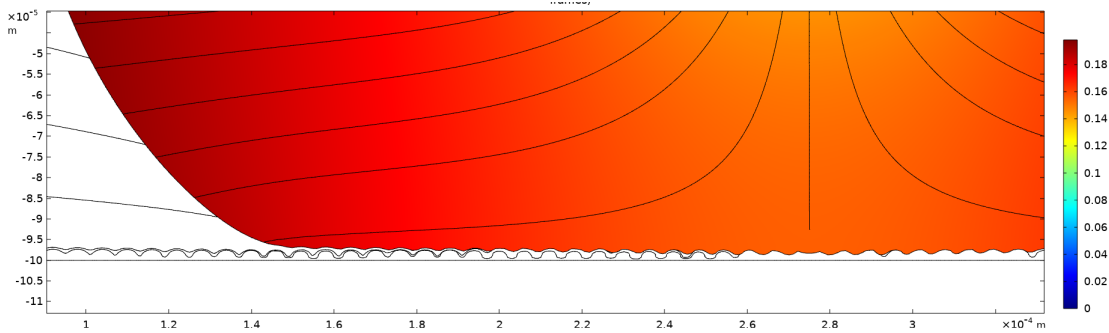


Fig 5.13. Zoom of the final interface for the pn++ candidate with $W_p = 4 \mu\text{m}$ and $W_n = 2 \mu\text{m}$.

The n++ candidate with $W_p = W_n = 2 \mu\text{m}$ behaves differently, as shown in Figure 5.14 and Figure 5.15. In this case, the interface oscillations are not visible. This can be understood from the resistivity map that was shown previously in Figure 3.2: the N-type regions are closely spaced, and the associated high-resistivity barriers almost form a continuous blocking layer.

Instead of creating small openings where the current can strongly penetrate, the pattern behaves almost as a uniform high-resistivity front-side barrier at the resolution of the simulation. The resulting interface is therefore smoother, but the porous front is also stopped earlier. This illustrates confirms the trade-off stated along this work that a strong barrier may protect the front-side efficiently but it will probably also leave a larger residual silicon thickness below the RF structures.

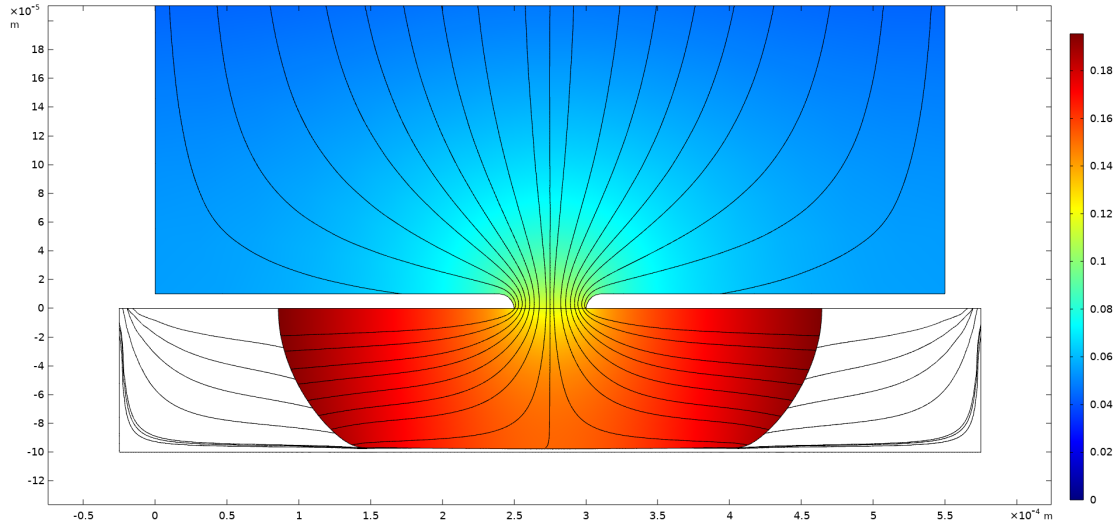


Fig 5.14. Final solution for the n^{++} candidate with $W_p = W_n = 2 \mu\text{m}$ at $\tau = 1$. The closely spaced high-resistivity N-type regions produce a much smoother front than in the wider PN cases.

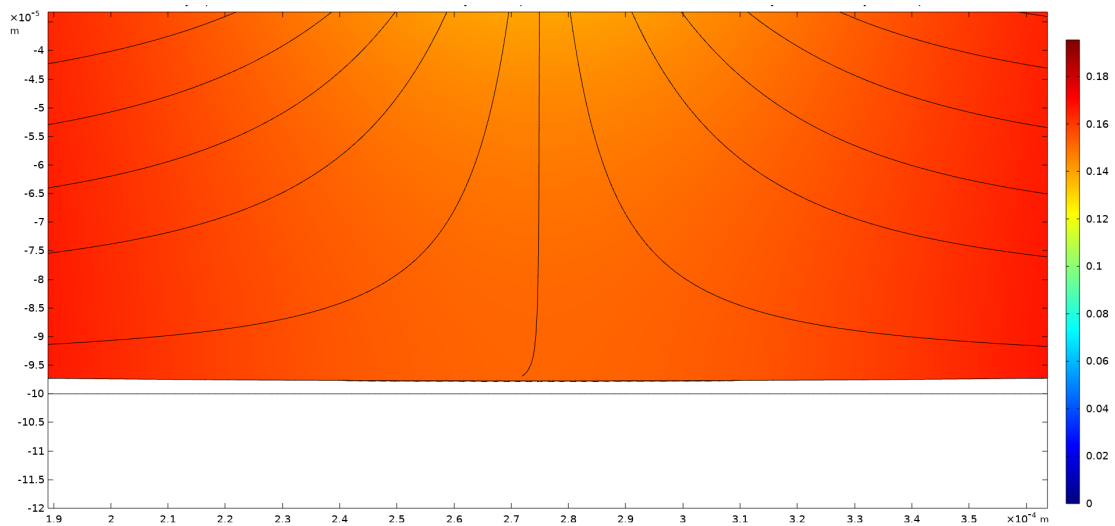


Fig 5.15. Zoom of the final interface for the n^{++} candidate with $W_p = W_n = 2 \mu\text{m}$.

5.3.4 Comparison of residual non-porosified thickness

After analyzing individual simulations, the different candidates are compared through the residual non-porosified silicon thickness extracted along the final Si/electrolyte interface. The

x-axis is called 'x' as it is the x-coordinate in the COMSOL simulation. The raw profiles contain sharp oscillations induced by the periodic PN patterns. For readability, the profiles shown in Figure 5.16 to Figure 5.19 are smoothed using a moving average. The smoothed profiles are used to compare the global penetration depth, while the oscillation amplitude is quantified separately in Table 5.1. The roles of the two metrics are complementary. The smoothed profile indicates the global penetration of the porous front, while the RMS oscillation indicates the local non-uniformity induced by the PN pattern.

The uniform-resistivity case is included as a reference in each comparison. It systematically leads to the smallest residual thickness, because no high-resistivity stopping structure blocks the current paths coming to the interface. This confirms that the PN patterns effectively slow down the porosification front in the model. The small residual thickness observed in the uniform case should however not be interpreted as a physical stopping effect. It is mainly related to the numerical difficulty of continuing the simulation when the remaining silicon layer becomes comparable to the local mesh size.

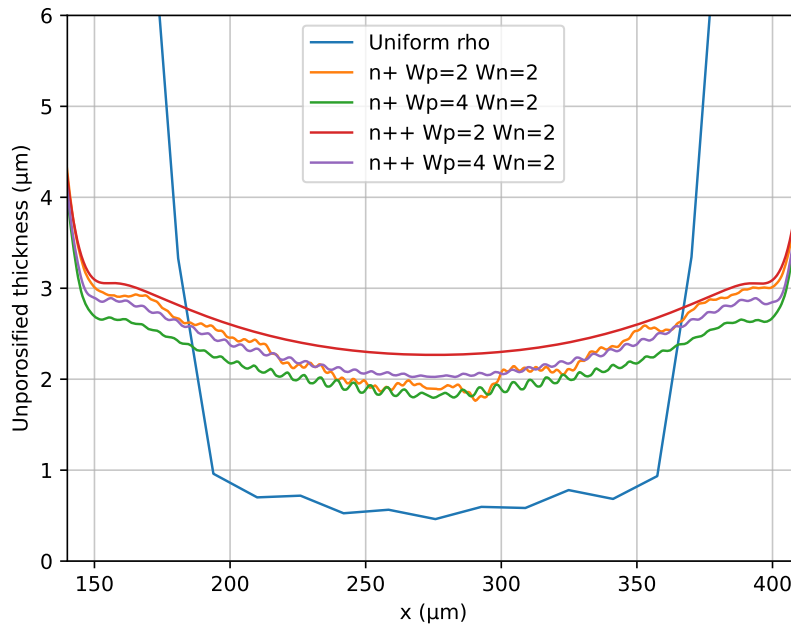


Fig 5.16. Smoothed residual non-porosified thickness at $\tau = 1$ for the $n+$ and $n++$ candidates, compared with the uniform-resistivity reference.

Figure 5.16 compares the $n+$ and $n++$ candidates. As a reminder, these structures do not include additional implanted P-type regions between the N-type barriers. The remaining thickness is around 2 μm . The high-resistivity regions are located below 1.6 μm . These candidates are thus, as expected, stopping the porosification too early and leaving an extra layer of silicon. The $W_p = 2 \mu\text{m}$ cases are stopping the porosification earlier than the 4 μm at equivalent doping levels, because the high-resistivity regions between the N-doped regions are closer to each other. This leads to a stronger bottleneck effect that will prevent the current from

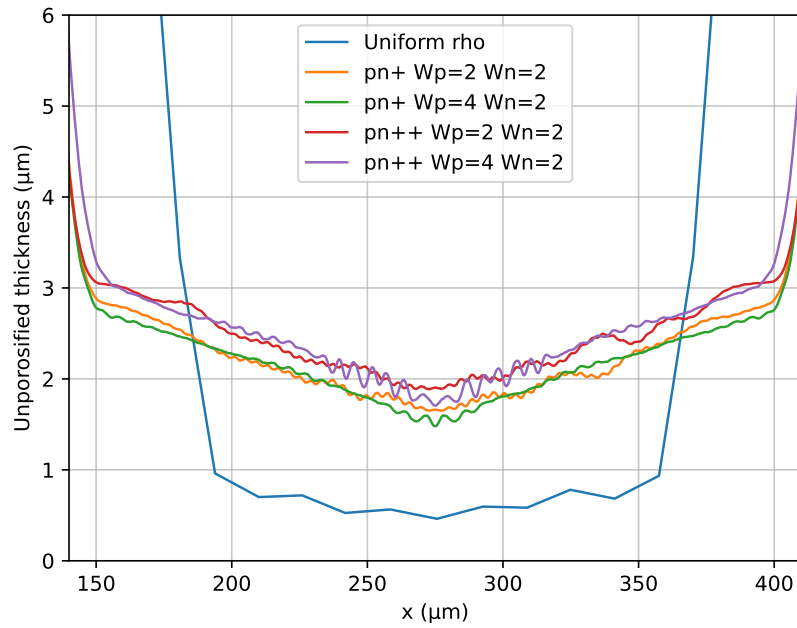


Fig 5.17. Smoothed residual non-porosity thickness at $\tau = 1$ for the pn+ and pn++ candidates, compared with the uniform-resistivity reference.

flowing between the N-doped zones. This leads to a larger residual thickness and, in the n++ $W_p = 2 \mu\text{m}$ case, to an almost perfectly smooth front.

Because of the larger space between the barriers in the $W_p = 4 \mu\text{m}$ cases, penetration between the N-type regions is possible. This also decreases the remaining layer above the N regions. This can be seen in Table 5.1, where the rms oscillation of the $W_p = 4 \mu\text{m}$ cases are always bigger than the one of their analog $W_p = 2 \mu\text{m}$ cases. The oscillations are however still limited as they are below $0.257 \mu\text{m}$, which is a sixth of the N region thickness.

Finally, as the increase of N dopants dose was linked to an increase of the depletion region width in the simulated resistivity maps in 3, it seems logical that the residual thickness is slightly bigger for the n++ cases compared to the n+ cases for the same dimensions.

Figure 5.17 shows remain crystalline silicon thickness for the pn+ and pn++ candidates. Adding implanted P-type regions modifies the behavior compared to the N-only structures. The P-type regions provide conductive regions that will reduce the bottleneck effect. As a result, the front can penetrate more deeply between the N-type barriers than in the most blocking N-only cases, especially for the $W_p = 4 \mu\text{m}$ geometries for which the minimal thickness is approximately $1.5 \mu\text{m}$. This value means that the minimum is probably located in a P-doped region between two N-doped regions. This stronger local penetration is also reflected in Table 5.1, where the ($W_p = 4 \mu\text{m}$) case is reaching the more significant value of $0.37 \mu\text{m}$ of rms oscillation which is a bit less than a quarter of the region.

The same geometrical trend as for the N-only candidates is observed: increasing (W_p) allows

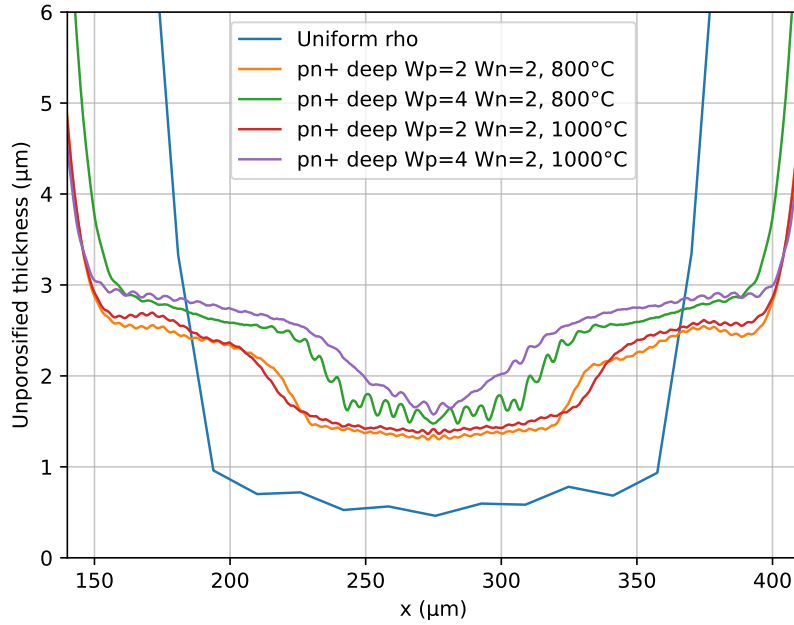


Fig 5.18. Smoothed residual non-porosified thickness at $\tau = 1$ for the pn+ deep candidates, compared with the uniform-resistivity reference.

stronger local penetration between the N-type barriers, but also increases the oscillation amplitude of the front. The effect of the doping level is also visible. The more heavily doped candidates tend to leave a larger residual thickness, which is consistent with a stronger effective blocking effect in the simulated resistivity maps due to the larger depletion regions.

Then, Figure 5.18 presents the pn+ deep candidates, for which the P-type region is shifted deeper into the substrate. The Figure confirms that the candidates allow a deeper penetration than the corresponding strongly blocking structures. Indeed, the presence of the shifted P-doped region facilitates the conductivity above the etch-stop layer as the current can flow through this low-resistivity. The $W_p = 2 \mu\text{m}$ cases lead to the smallest residual thickness among the pn+ deep curves, with only around $1.4 \mu\text{m}$. This is because the P-doped regions facilitate the conduction in the upper part of the layer while the closely-spaced N-regions create a strong bottleneck effect between them in the lower part of the layer. As a result, the porosification is favored in an homogeneous way in the upper part of the layer but is strongly blocked in the lower part.

In contrast, the $W_p = 4 \mu\text{m}$ cases preserve a stronger spatial modulation: the front penetrates more locally below the P-type regions because the N regions are more spaced. The porosification is then less favored above the N regions and the remaining thickness is around $1.7 \mu\text{m}$. This increases the RMS oscillation and leads to a larger smoothed residual thickness.

The effect of the annealing is nevertheless not very significant compared to the geometry or the doping levels, it is difficult to extract any conclusion of this. It seems that for $W_p = 4 \mu\text{m}$, the

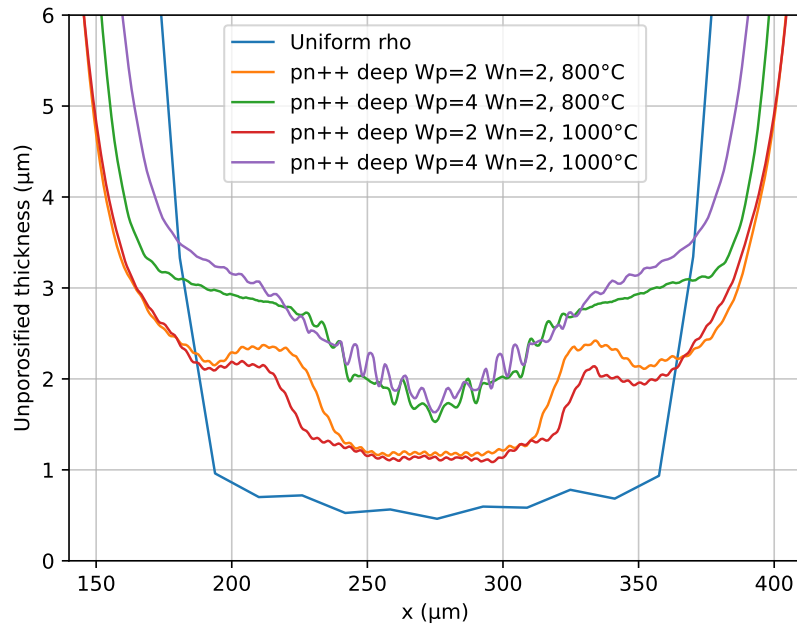


Fig 5.19. Smoothed residual non-porosity thickness at $\tau = 1$ for the pn++ deep candidates, compared with the uniform-resistivity reference.

increase of the annealing temperature increases the remaining porous thickness. This could be consistent with the fact that the depletion regions are wider with a higher temperature as the diffusion of the implants is bigger.

Finally, Figure 5.19 shows the pn++ deep candidates curve of non-porosity thickness. These cases provide the strongest penetration among the PN patterns simulated, especially for $W_p = 2 \mu\text{m}$ at both annealing temperatures, for which the remaining layer is roughly $1.2 \mu\text{m}$ thick. This result is consistent with the role of the deeper and more conductive P-type region. The resistivity of the upper part of the etch-stop layer is even more reduced thanks to the bigger dose of P-type regions compared to the pn+ deep candidates.

The difference induced by the geometry is similar to previous Figure. The wider zones between the N-doped regions are easily penetrated with $W_p = 4 \mu\text{m}$ but, because of that, the front progression above the high-resistivity N-type regions remains strongly limited, with a thickness around $1.5 \mu\text{m}$ left. The oscillations exhibited in this case are really big, above $0.5 \mu\text{m}$. This is nearly a third of the zone. The bottleneck effect is therefore not so efficient in that case.

To conclude this section, a clear trend can be observed in the RMS oscillation values in Table 5.1: for most families, the $W_p = 4 \mu\text{m}$ cases exhibit larger oscillations than the $W_p = 2 \mu\text{m}$ cases. This is consistent with the larger separation between neighboring high-resistivity barriers reducing the bottleneck effect. Conversely, when the barriers are closely spaced, the front undergoes a stronger bottleneck effect and the local oscillations are reduced.

Doping profile	RMS interface oscillation [μm]
pn+ deep $W_p = 2 \mu\text{m}$, $W_n = 2 \mu\text{m}$, 800°C	0.179
pn+ deep $W_p = 4 \mu\text{m}$, $W_n = 2 \mu\text{m}$, 800°C	0.357
pn+ deep $W_p = 2 \mu\text{m}$, $W_n = 2 \mu\text{m}$, 1000°C	0.177
pn+ deep $W_p = 4 \mu\text{m}$, $W_n = 2 \mu\text{m}$, 1000°C	0.297
pn++ deep $W_p = 2 \mu\text{m}$, $W_n = 2 \mu\text{m}$, 800°C	0.188
pn++ deep $W_p = 4 \mu\text{m}$, $W_n = 2 \mu\text{m}$, 800°C	0.396
pn++ deep $W_p = 2 \mu\text{m}$, $W_n = 2 \mu\text{m}$, 1000°C	0.190
pn++ deep $W_p = 4 \mu\text{m}$, $W_n = 2 \mu\text{m}$, 1000°C	0.505
pn+ $W_p = 2 \mu\text{m}$, $W_n = 2 \mu\text{m}$	0.137
pn+ $W_p = 4 \mu\text{m}$, $W_n = 2 \mu\text{m}$	0.314
pn++ $W_p = 2 \mu\text{m}$, $W_n = 2 \mu\text{m}$	0.140
pn++ $W_p = 4 \mu\text{m}$, $W_n = 2 \mu\text{m}$	0.373
n+ $W_p = 2 \mu\text{m}$, $W_n = 2 \mu\text{m}$	0.143
n+ $W_p = 4 \mu\text{m}$, $W_n = 2 \mu\text{m}$	0.257
n++ $W_p = 2 \mu\text{m}$, $W_n = 2 \mu\text{m}$	0.001
n++ $W_p = 4 \mu\text{m}$, $W_n = 2 \mu\text{m}$	0.125

Table 5.1: RMS oscillation amplitude of the residual non-porosified thickness for the different doping profiles.

5.3.5 Conclusion

Overall, the 2D simulations show that the PN resistivity patterns can significantly modify the porosification front. Compared with the uniform substrate, all PN candidates increase the remaining silicon thickness, confirming their stopping effect. Among the tested patterned cases, the pn++ deep candidates with $W_p = 2 \mu\text{m}$ and $W_n = 2 \mu\text{m}$ provide the smallest residual thickness at both annealing temperatures, with a value of approximately $1.2 \mu\text{m}$. This suggests that they offer a favorable compromise in the 2D model: the porous front can penetrate deeply in a homogeneous way while undergoing a strong bottleneck effect between the N-type regions.

This conclusion must remain specific to the present modeling assumptions. The N-type regions are represented by an effective high resistivity and the junction depletion regions are not recomputed dynamically. The results should therefore be interpreted as a comparison of current-redistribution tendencies rather than as a definitive prediction of experimental stopping performance. Furthermore, the crashes of the simulation for longer simulation times does not allow to compare the trends for later time steps that could have had interesting features.

Chapter 6

3D simulations

The previous chapter introduced the two-dimensional COMSOL model used to describe the growth of a porous silicon pocket during back-side porosification. In that model, the simulated cross-section was assumed to be invariant in the third direction. This assumption is useful to reduce the computational cost and to isolate the effect of local resistivity profiles, but it cannot describe the finite geometry of the real back-side openings. In practice, the openings have a finite length and rounded ends. These geometrical features are expected to redistribute the current in three dimensions and therefore create non-uniformity effects along the length of the porous pocket, as observed in Chapter 4.

The objective of this chapter is to extend the previous model to three dimensions in order to reproduce and interpret this geometry-induced non-uniformity. Based on the simulated current redistribution, modified electrode geometries are then proposed to reduce the non-uniformity of the porous pocket.

6.1 From the 2D model to the 3D geometry

The physical assumptions used in the 3D model are the same as those introduced for the 2D simulations. The governing equations, the electrochemical interface condition, and the moving-boundary strategy are therefore not repeated in detail here. Mathematically, the 3D model mainly adds a third spatial coordinate to the current-distribution and deformed-geometry problems. Geometrically, however, the change is significant. The 2D model represents an infinitely extruded opening, whereas the 3D model includes the finite length and rounded end of the experimental back-side opening.

If the 2D cross-section were simply extruded along the third direction, the result would remain essentially equivalent to the 2D model because the geometry would still be invariant along the extrusion direction. In the present model, the rounded end breaks this invariance and allows the current lines to spread laterally in both the silicon and the electrolyte-filled porous region.

To reduce the computational cost, only a symmetric fraction of the full structure is simulated. The simulated domain corresponds to one quarter of the physical die, using the geometrical symmetry of the opening and of the current grid, as shown in Figure 6.1. This choice preserves the current-spreading effects near the rounded end while limiting the number of mesh elements. The main geometrical parameters of the model are listed in Table 6.1. The corresponding COMSOL geometry is shown in Figure 6.2, with the silicon substrate in gray, the electrolyte in blue and the initial electropolished cavity in brown.

Parameter	Value	Description
W_{die}	600 μm	Die width
L_{die}	1300 μm	Die depth in the longitudinal direction
t_{Si}	100 μm	Silicon wafer thickness
t_{el}	600 μm	Electrolyte height
L_{el}	1275 μm	Electrolyte depth
W_{open}	50 μm	Back-side opening width
u_{etch}	25 μm	Lateral underetch of the pre-etched cavity
t_{cav}	25 μm	Initial cavity thickness in the silicon
L_{cav}	1000 μm	Longitudinal depth of the pre-etched cavity
R_{end}	300 μm	Radius defining the rounded end of the opening

Table 6.1: Main geometrical parameters of the 3D COMSOL reference model.

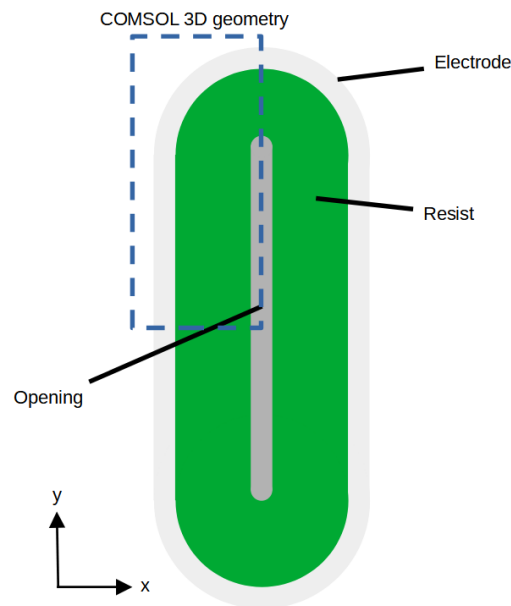


Fig 6.1. Schematic representation of the three-dimensional back-side opening geometry. Only a symmetric fraction of the full pocket is simulated in order to reduce the computational cost while keeping the rounded-end current-spreading effect.

The boundary conditions follow the same logic as in the 2D model. The upper boundary of the electrolyte is set to a fixed electrolyte potential and represents the counter-electrode. A current density is imposed on the back-side current-injection boundary representing the grid. This surface is represented in blue in Figure 6.2. The other non-electrode boundaries

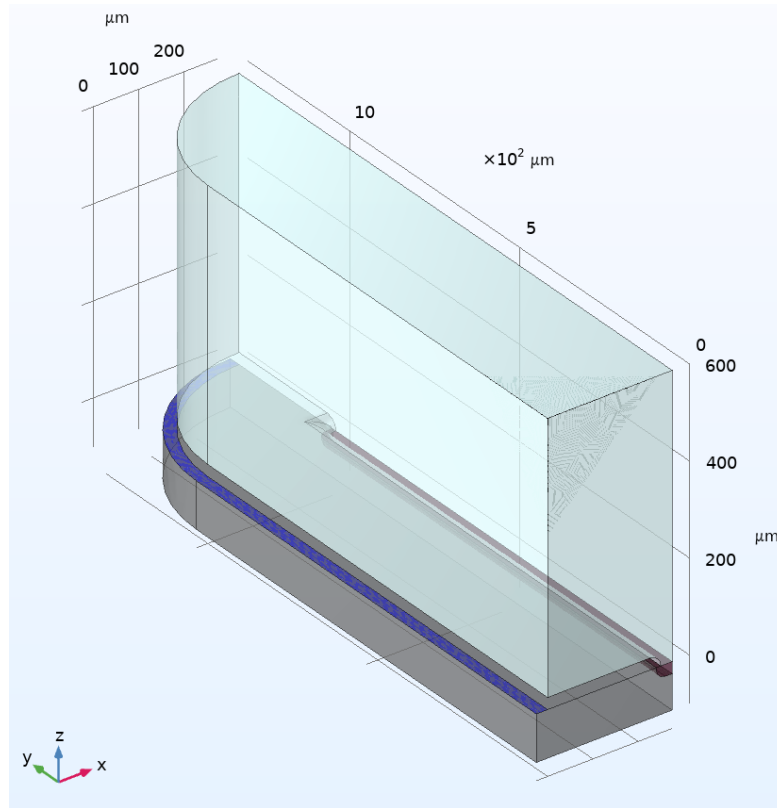


Fig 6.2. Three-dimensional COMSOL geometry representing only a quarter of the full die.

are electrically insulating boundaries. The porosification reaction is again defined only on the internal Si/electrolyte interface, so between the pre-etched cavity and the Si wafer.

6.2 Mesh and computational cost

The 3D model uses free tetrahedral elements. As in the 2D model, the mesh is refined near the moving Si/electrolyte interface and around the initial cavity, where the strongest curvature and current-density gradients are expected. A coarser mesh is used in the upper part of the electrolyte, since the detailed field distribution far from the reaction front is not the main quantity of interest. Due to the computational cost of the 3D moving-boundary problem, the smallest element size around the interface is kept close to $5\ \mu\text{m}$. This mesh size reduces the spatial resolution compared with the refined 2D simulations, but it provides an acceptable compromise between numerical resolution and computation time.

The 3D extension strongly increases the computational cost compared with the 2D model. Even the uniform-resistivity reference case requires a much longer computation time than the corresponding 2D simulation. This limitation is important for the interpretation of the following results. The 3D model is used to study macroscopic geometrical effects and current redistribution along the finite pocket, while the 2D model remains more suitable for resolving sharp local resistivity variations associated with the PN stopping patterns.

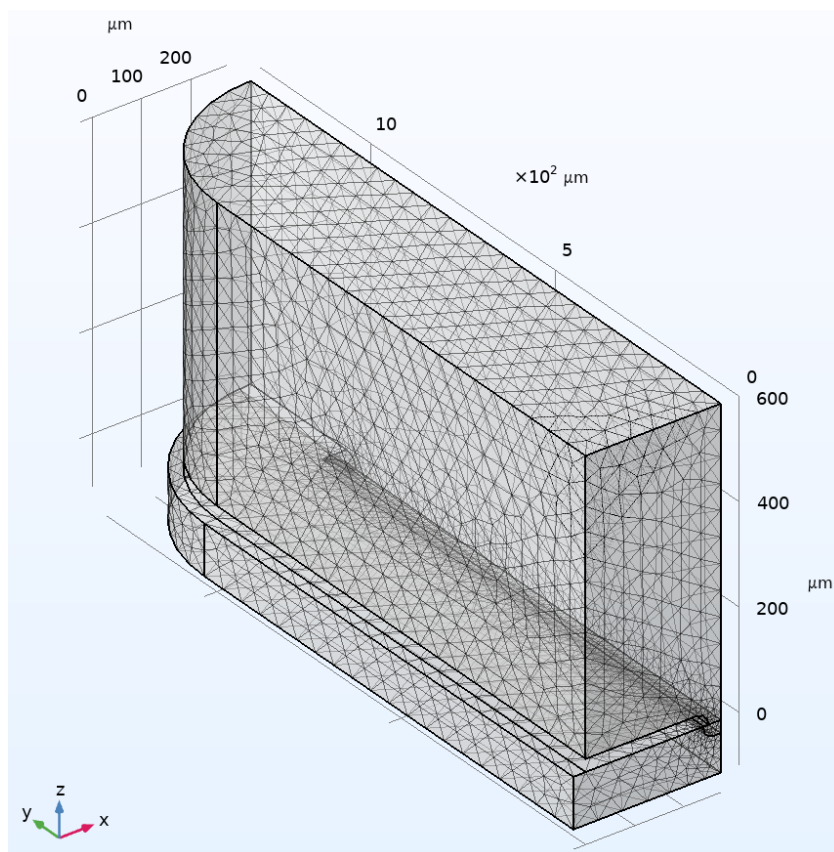


Fig 6.3. Tetrahedral mesh used in the 3D model. The mesh is refined near the initial cavity and the moving Si/electrolyte interface, while the electrolyte volume is meshed more coarsely away from the reaction zone.

The simulation procedure remains the same as in 2D. A current-distribution initialization step is first performed to compute a consistent initial electric field. The time-dependent study then solves the coupled primary current distribution and moving-boundary problem. Automatic remeshing is enabled to preserve mesh quality as the interface moves.

As in the previous chapter, the simulated time is normalized as a variable τ , ranging from 0 for the initial geometry to 1 for the final available time step. The time is, indeed, not a representative quantity as the total injected current is kept constant during the simulation. As a result, as the active Si/electrolyte interface grows, the total active surface increases while the imposed current supply does not follow this increase. The average current density at the moving front will consequently decrease during the simulation. The results are therefore interpreted in terms of relative shape evolution and current redistribution, rather than absolute porosification time.

6.3 Results on uniform ρ substrates

The first 3D simulations are performed on a uniform silicon substrate with a resistivity of $10 \text{ } \Omega\text{cm}$. This reference case is used to check that the 3D model behaves consistently before introducing additional resistivity patterns. In the x - z plane, corresponding to the 2D geometry, the porosification is expected to be uniform. In the $x - y$ and $y - z$ plans, on the contrary, the finite 3D geometry is expected to create a longitudinal non-uniformity because the current can spread differently near the rounded end of the opening. Indeed, the current supply is expected to increase from the symmetry central point to the end of the pocket following the y -axis.

Figure 6.4 and Figure 6.5 show the initial solution at $\tau = 0$ in two cross-sections. The current streamlines are not confined to planes equivalent to the 2D cross-section. Instead, they bend toward the end of the pocket, showing that the current distribution is already three-dimensional at the beginning of the simulation. This confirms that the 3D model captures an effect that cannot be represented by a simple 2D extrusion.

The solution at the final time step is shown in Figure 6.6 and Figure 6.7. The porous pocket has grown deeper near its rounded end than near the symmetry plane. This behavior is consistent with the streamline distribution observed at $\tau = 0$ and $\tau = 1$: the end of the pocket receives a larger local current density and therefore the porosification happens faster. The pocket is not only deeper near the rounded end, but also laterally wider, which is consistent with the approximately isotropic motion of the local porous front.

The uniform-resistivity simulation therefore validates the expected qualitative behavior of the 3D model. The model does not simply reproduce the 2D result: it reveals an additional non-uniformity along the pocket length linked to the finite back-side geometry and motivates the geometry modifications studied later in this chapter.

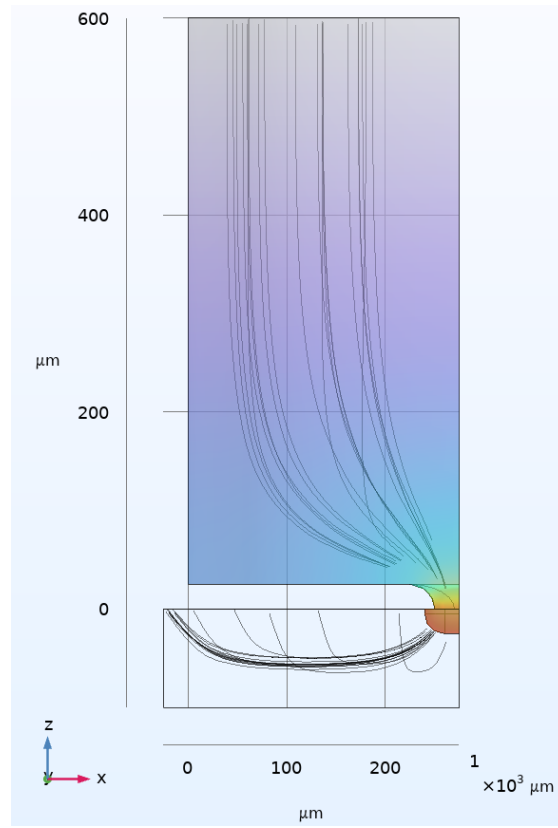


Fig 6.4. Cross-section in the $x - z$ plane of the uniform-resistivity 3D solution at $\tau = 0$.

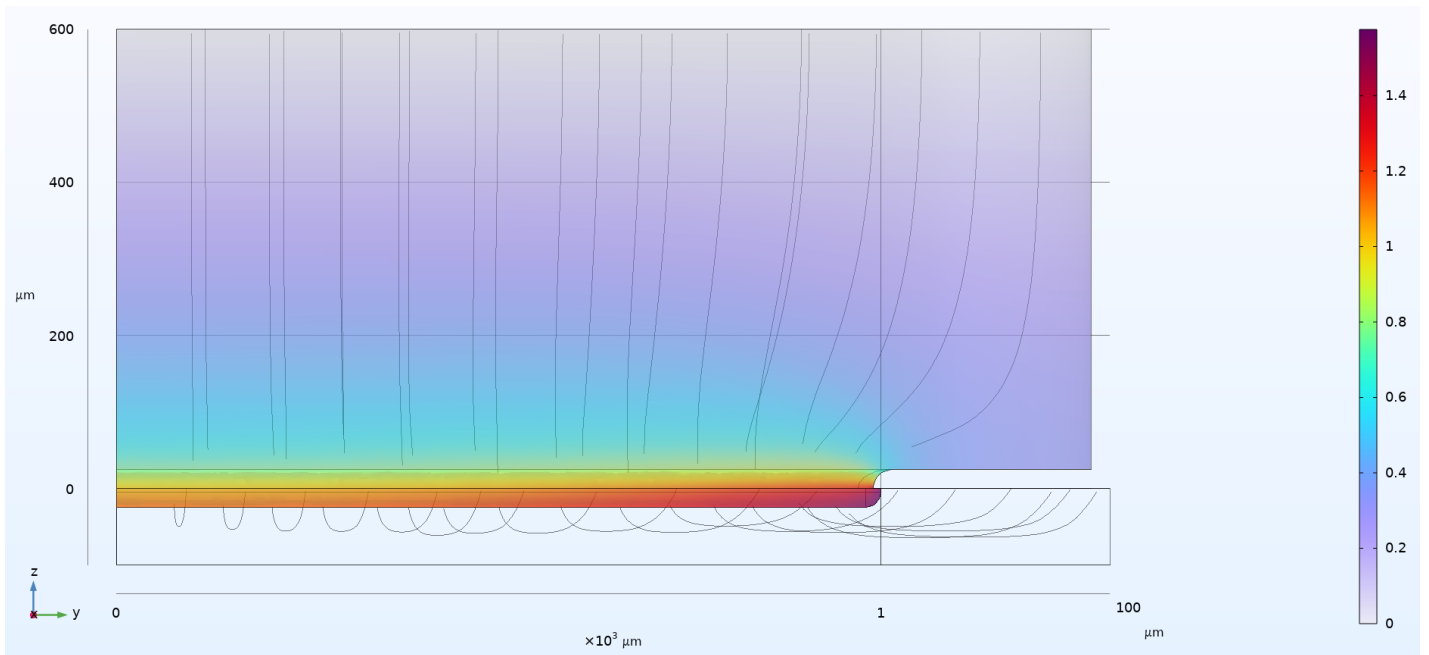


Fig 6.5. Cross-section in the $y - z$ plane of the uniform-resistivity 3D solution at $\tau = 0$.

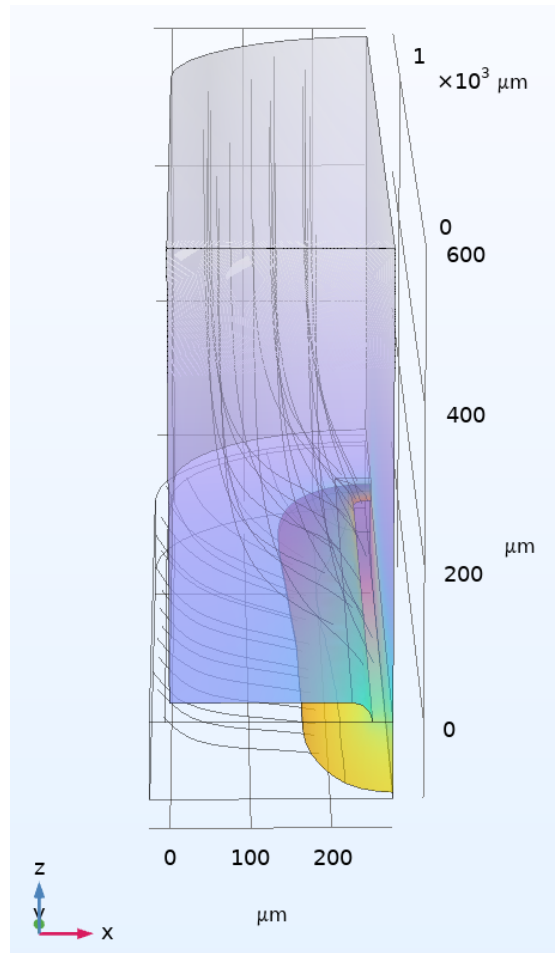


Fig 6.6. Cross-section in the $x - z$ plane of the uniform-resistivity 3D solution at $\tau = 1$ shown with a slight perspective to visualize the lateral extension of the porous region.

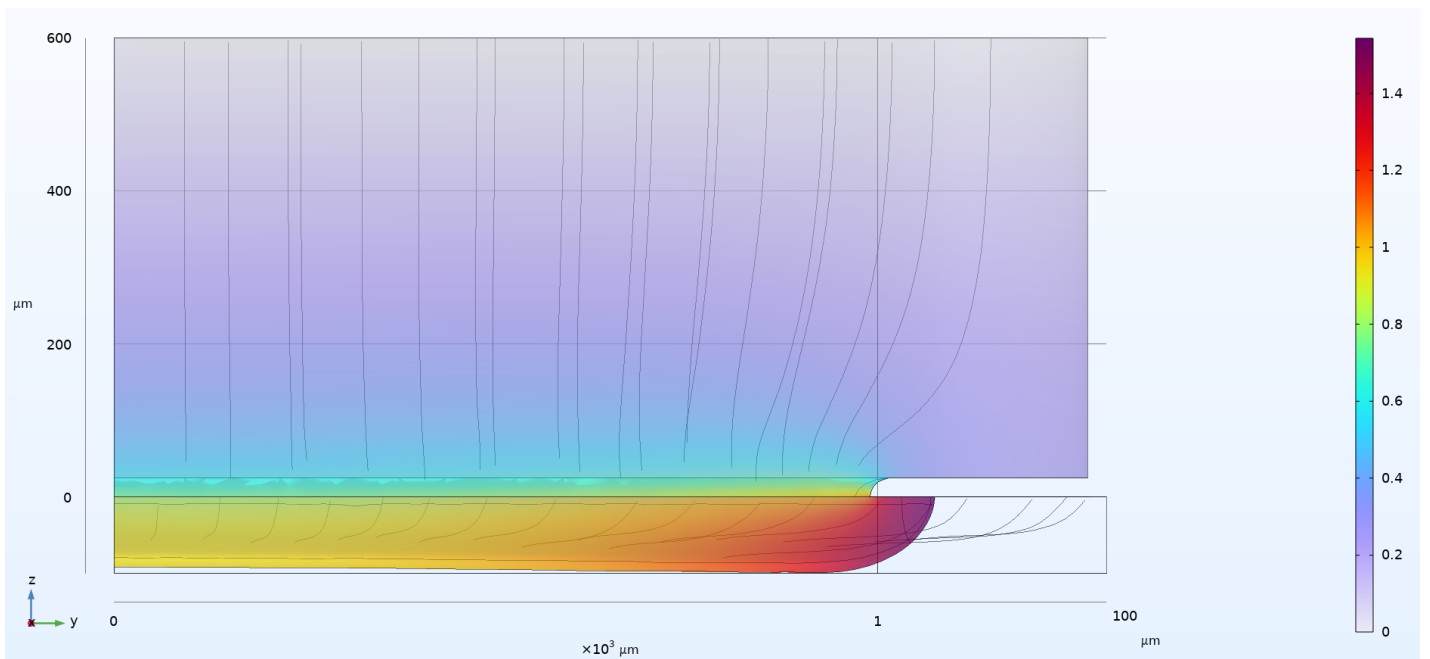


Fig 6.7. Cross-section in the $y - z$ plane of the uniform-resistivity 3D solution at $\tau = 1$.

6.4 Results with different resistivity patterns

After validating the behavior of the model, the next step was to introduce resistivity variations into the 3D model. The first approach was to import the same Silvaco Atlas resistivity maps as in the 2D simulations. These maps were defined in the $x - z$ plane and then assumed to be invariant along the y -direction. This approximation was used because full three-dimensional TCAD implantation profiles corresponding to the experimental square or line patterns were not available.

However, this direct approach is not numerically practical in 3D. As discussed in the previous chapter, the PN resistivity profiles contain sharp transitions and high contrasts over submicrometer distances. In 2D, resolving these profiles already required a strongly refined mesh. In 3D, applying the same refinement would increase the number of elements and the computation time by a prohibitive amount. Using a mesh fine enough to resolve the full PN profiles was not considered realistic for the present study.

A simplified idealized PN pattern was therefore tested. It consisted of alternating rectangular regions with resistivities of $1 \text{ M}\Omega\text{cm}$ and $1 \text{ m}\Omega\text{cm}$, each $4 \text{ }\mu\text{m}$ wide and $4 \text{ }\mu\text{m}$ thick in the $x - z$ plane and invariant along the y -direction. This pattern was intended to mimic an ideal alternation between highly conductive P-type paths and strongly blocking N-type regions. However, even this simplified rectangular pattern remained difficult to combine with the moving boundary in 3D. The sharp resistivity discontinuities still produced convergence issues when the moving mesh crossed from one resistivity region to another.

For this reason, a final simplified resistivity pattern was introduced: a continuous high-resistivity layer at the lower end of the silicon substrate. In this model, the last $3 \text{ }\mu\text{m}$ of silicon are assigned a resistivity of $1 \text{ M}\Omega\text{cm}$, while the rest of the wafer keeps the standard resistivity of $10 \text{ }\Omega\text{cm}$. This layer is not meant to reproduce the detailed PN layout. Instead, it acts as an effective stopping region that reduces the current supply when the porous front approaches the front-side. It also avoids the numerical instabilities associated with sharp laterally alternating resistivity profiles.

This HR layer provides a useful reference for the comparison of electrode geometries. In the real structure, the PN stopping layer is expected to slow down the porous front when it approaches the front-side, because the current path becomes increasingly resistive. A fully uniform substrate would not include this stopping effect and would therefore not represent the situation targeted in the experiments. The HR layer case is thus used as a simplified and numerically stable reference to study how the 3D electrode geometry affects the residual non-porosified silicon thickness.

The profiles compared in Figure 6.8 are extracted at the first time step for which the minimum residual thickness becomes lower than $6 \text{ }\mu\text{m}$. This threshold is chosen as a compromise. It is low enough for the porous front to start interacting with the high-resistivity layer, so that the

effective stopping behavior is already visible. At the same time, it remains sufficiently far from the $3\text{ }\mu\text{m}$ -thick idealized HR layer to avoid a regime where the front shape would be dominated by this simplified layer rather than by the 3D current redistribution. It is then chosen as the reference to compare the effects of the HR layer and, later, of the geometry changes.

Figure 6.8 shows that the high-resistivity layer reduces the final non-uniformity of the remaining non-porositified layer compared to the fully uniform substrate. For the same minimal thickness, the remaining layer at the symmetry point is approximately $2\text{ }\mu\text{m}$ higher. Nevertheless, the longitudinal variation remains visible, meaning that the 3D geometry still creates a significant non-uniformity, even with the HR layer. For the rest of the chapter, the HR layer case is therefore used as the reference pattern. It provides a conservative and numerically stable way to evaluate whether electrode geometry modifications can reduce the 3D non-uniformity.

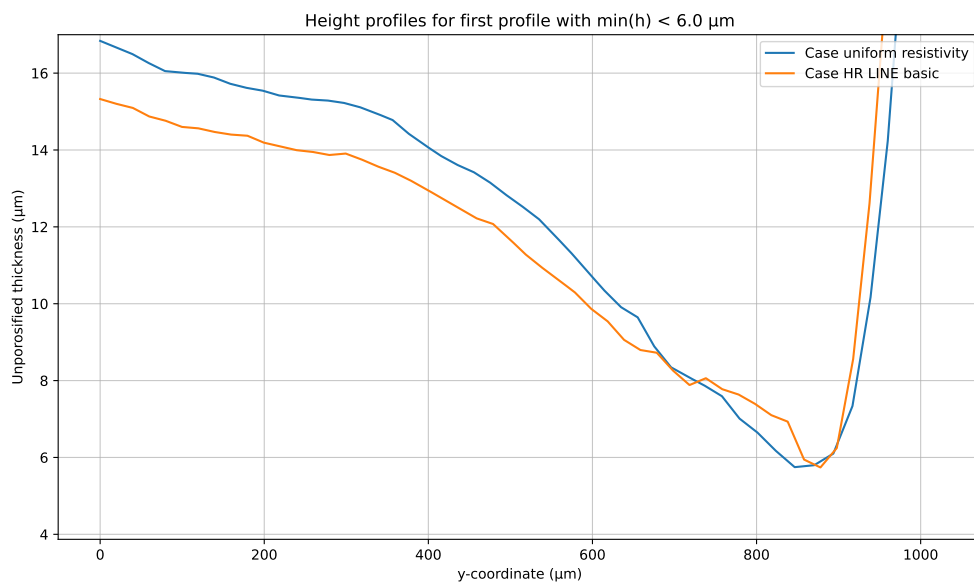


Fig 6.8. Comparison of the residual non-porositified silicon thickness along the pocket for the uniform-resistivity case and for the simplified HR layer case. The profiles are extracted at the first time step for which the minimum residual thickness is below $6\text{ }\mu\text{m}$.

6.5 Modification of the electrode geometry

The previous sections showed that the finite 3D geometry accelerates porosification near the rounded end of the pocket. The objective of this section is to evaluate whether the back-side metallic grid can be reshaped in order to reduce this non-uniformity. The guiding idea is to increase the access resistance between the grid and the regions that porosify too quickly. Moving the grid further away from the rounded end increases the current path length through the substrate and therefore reduces the fraction of current supplied to this region. The porosification rate near the end of the pocket is then expected to decrease. All the proposed geometry changes will be tested with idealized corners (without rounding) in order to simplify the geom-

etry definitions

The different candidates are compared using the residual silicon thickness along the pocket. A figure of merit, called the uniform length, is introduced to quantify the useful part of the pocket. It is defined as the distance over which the residual thickness remains within a tolerance Δh of the value at the symmetry plane:

$$L_{\text{uni}}(\Delta h) = \max \{ y : |h(y') - h(0)| < \Delta h \quad \forall 0 \leq y' \leq y \}, \quad (6.1)$$

where $h(y)$ is the residual non-porosified thickness along the pocket. In this work, $\Delta h = 2 \mu\text{m}$ is chosen. This value is not a universal process specification, but it provides a practical criterion for comparing the different geometries. It is of the same order as the dimensions of the PN stopping patterns. It is therefore expected to represent the length along which the porous front will be close enough of the stopping layer without piercing it. It is also chosen to be robust against the local fluctuations of the height cause by the lower resolution.

This metric is directly linked to the RF structures above the porous pocket. It aims to represent the length of the region with improved effective parameters because the simulation is uniform enough. Since the model represents only half of the pocket along the y -direction, the uniform length obtained in the simulation corresponds to half of the uniform region in the full structure. For example, a simulated uniform length of $800 \mu\text{m}$ would correspond to approximately 1.6 mm of uniform porosification in the complete pocket, and could therefore be suitable for a CPW of comparable length.

6.5.1 The notch case

The first modification consists in adding a notch to the electrode near the rounded end of the opening. Figure 6.9 shows this design. The notch locally increases the distance between the grid and the end of the porous pocket, where the reference simulation shows the fastest porosification. The expected effect is therefore a reduction of the local current supply near the porous region end.

The resulting residual-thickness profile is compared with the reference HR layer case (called HR LINE) in Figure 6.10. The notch increases the uniform length from $364.1 \mu\text{m}$ to $490.7 \mu\text{m}$. This confirms that locally moving the current-injection boundary away from the rounded end can reduce the longitudinal non-uniformity. However, the improvement remains limited and the front is still significantly deeper near the end of the pocket.

This result must be interpreted with caution though. In the real process, the current is imposed globally and the metallic grid redistributes this current according to the local access resistances. In the present COMSOL implementation, a current density is imposed on the electrode surface. Therefore, when the notch reduces the electrode area, the total injected current is also slightly modified. This numerical implementation can amplify the apparent effect of the notch. A

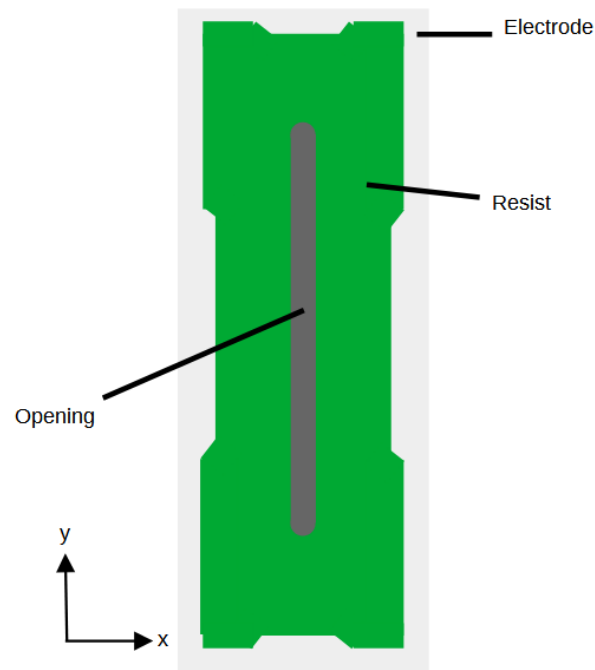


Fig 6.9. Schematic top-view of the notch electrode geometry. The metallic grid is locally recessed near the rounded end of the opening in order to increase the access resistance in the region where porosification is fastest.

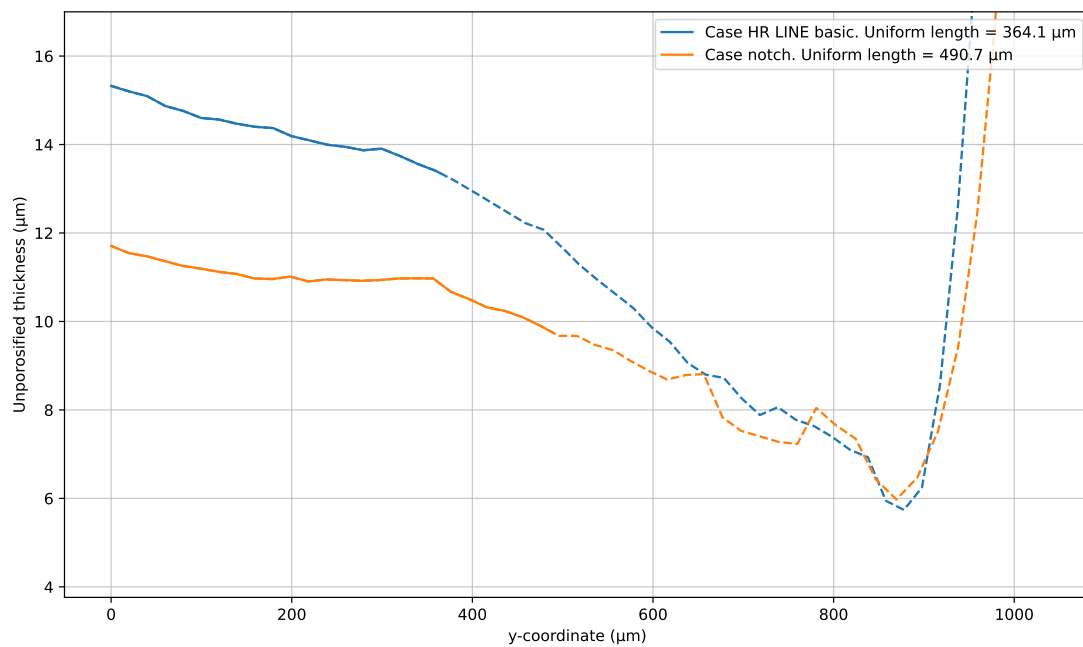


Fig 6.10. Residual non-porosified silicon thickness for the reference HR layer (HR LINE) case and for the notch electrode geometry.

better way to implement the notch with the current density condition in COMSOL would then be to add an offset instead of the notch to have the grid near the corner further away without decreasing the width. Nonetheless, the trend remains useful: increasing the local distance between the grid and the pocket end is a relevant direction for improving uniformity. This makes the notch a useful preliminary design, but not a fully optimized geometry.

6.5.2 The cut case

The second geometry is a stronger version of the notch. Instead of only recessing the electrode near the rounded end, this part is removed. The electrode is therefore separated into two lateral parts, as shown in Figure 6.11. The remaining electrode length is defined as αL_{cav} , where L_{cav} is the cavity length and α is varying between 0.85 and 1. Smaller values of α remove a larger fraction of the electrode close to the rounded end and should therefore produce a stronger reduction of the current supplied to that region.

This case could seem incompatible with the grid geometry of the electrode but this case is in fact asymptotic. In real experiments, the two parts of the electrode would be linked by a metal trace that would be very far so that its influence would be negligible. The downside of this solution is therefore that the real implementation would take a lot of space to be set up, resulting in a low density of integration.

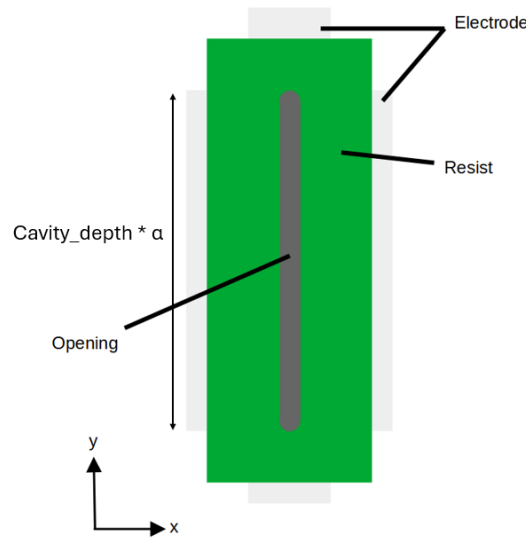


Fig 6.11. Schematic top-view of the cut electrode geometry. The electrode is removed near the rounded end of the opening. The remaining electrode length is controlled by the parameter α .

The results are shown in Figure 6.12. All cut geometries improve the uniform length compared with the reference case, HRLINE. For $\alpha = 1$, the uniform length increases to $663.0 \mu\text{m}$. Reducing the electrode further improves the result, with $L_{\text{uni}} = 945.9 \mu\text{m}$ for $\alpha = 0.9$. The case $\alpha = 0.85$ gives a slightly lower uniform length of $893.9 \mu\text{m}$, suggesting that an excessive removal of the electrode does not necessarily improve the profile further. This can be seen in the Figure as

the problem is now that the porosification rate at the edge is lower than at the center. There is thus a trade-off in the reduction of current supply to keep it in the same range over the whole range of the opening.

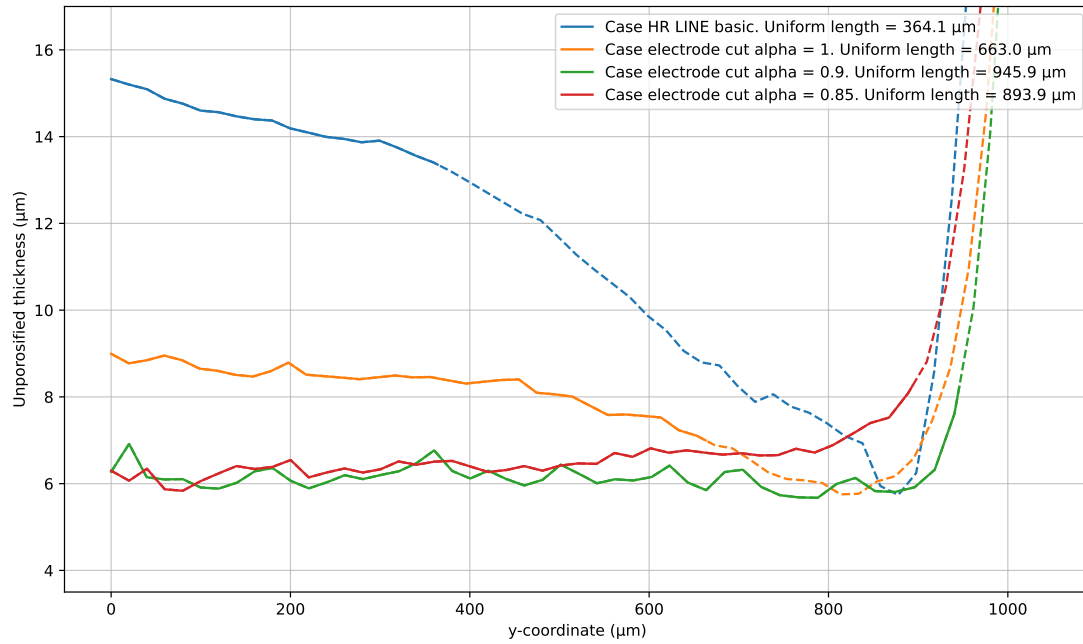


Fig 6.12. *Residual non-porosified silicon thickness for the reference HR layer and for the cut electrode geometries, with $\alpha = \{0.85, 0.9, 1\}$.*

6.5.3 The side case

The third geometry further simplifies the cut case. The electrode is reduced to a lateral line parallel to the opening, without a metallic segment near the rounded end. This idealized "side" electrode geometry is shown in Figure 6.13. It represents an asymptotic case in which the current supply near the end is minimized. In a real layout, however, the different electrode lines must remain connected to the global grid. It would be possible to remove the transversal part of the grid but the pockets inside of the same vertical column would have to be linked together to connect the pockets at the center of the wafer with the electrical contact. If the connection is placed too close to the pocket end, it can reintroduce an influence that the side geometry is meant to avoid. The same problem is thus stated as for the "cut" case electrode. There will be a trade-off between the density of integration and the efficiency of the uniformity for this geometry.

For this reason, a more realistic continuous version is also considered, as shown in Figure 6.14. In this layout, the side electrodes are connected to the die in the vertical direction, but the connecting part is shifted away from the end of the pocket by an offset distance. Two distances between the side electrode and the opening are studied, $d = 250 \mu\text{m}$ and $d = 500 \mu\text{m}$, together with several values of the offset.

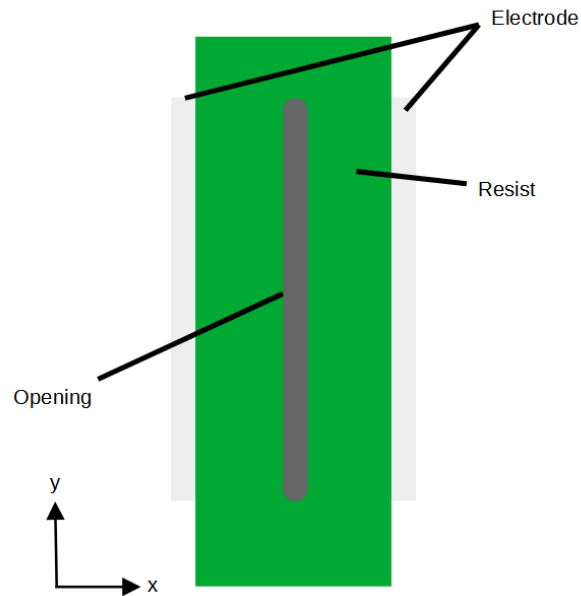


Fig 6.13. Schematic top-view of the idealized "side" electrode geometry. The electrode is kept only along the side of the opening, removing the current supply close to the rounded end.

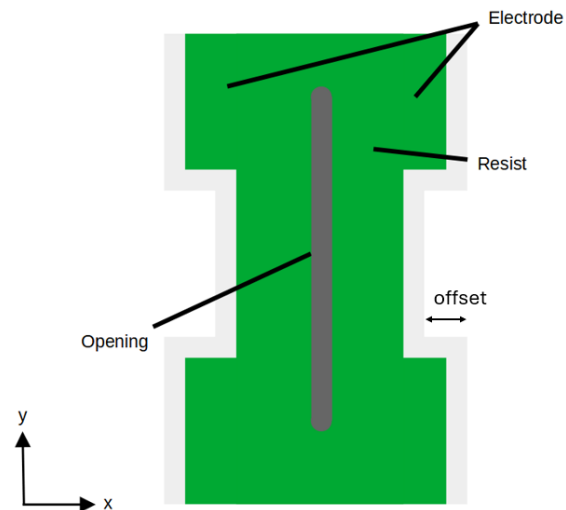


Fig 6.14. Schematic top-view of the continuous "side" electrode geometry. The side electrodes remain connected, but the connecting part is shifted away from the rounded end by an offset distance.

Figure 6.15 presents the results for $d = 250 \mu\text{m}$. The idealized side case gives a nearly uniform profile according to the chosen criterion, with $L_{\text{uni}} = 944.6 \mu\text{m}$. However, when the electrodes are connected with no offset, the uniform length decreases to $424.8 \mu\text{m}$, only slightly above the reference case. Adding the offset improves the situation: the uniform length reaches $471.7 \mu\text{m}$ for an offset of $100 \mu\text{m}$ and $535.4 \mu\text{m}$ for an offset of $175 \mu\text{m}$. This confirms that the connection region must be kept far enough from the pocket end to avoid reintroducing a local current supply.

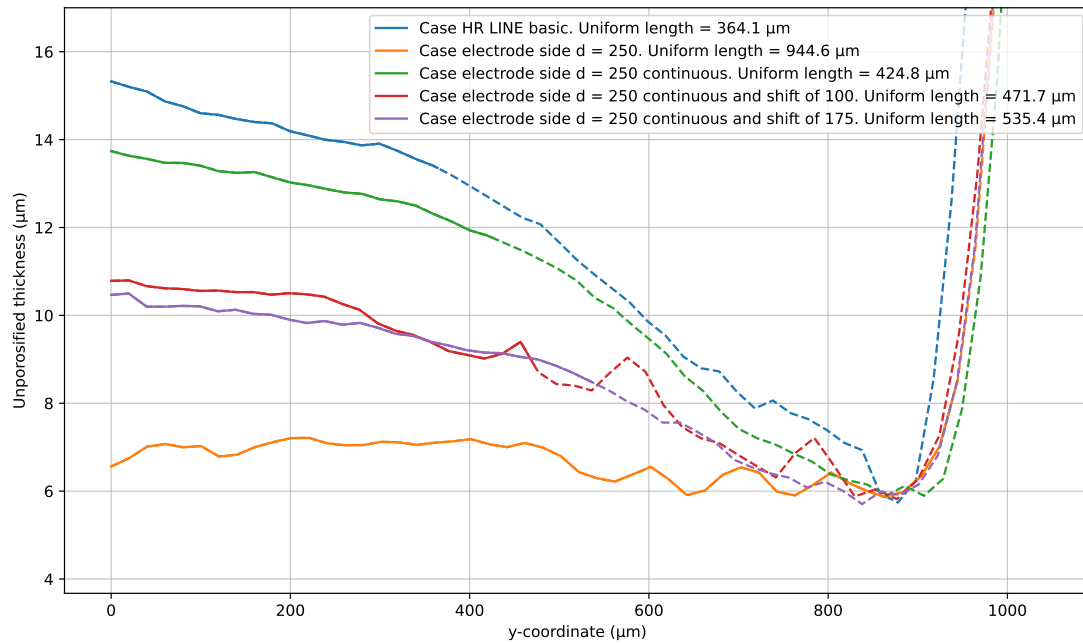


Fig 6.15. Residual non-porosity silicon thickness for the "side" electrode geometries with $d = 250 \mu\text{m}$.

The same analysis is performed for $d = 500 \mu\text{m}$ in Figure 6.16. Increasing the distance between the side electrode and the opening improves the continuous geometry. The side case gives $L_{\text{uni}} = 953.1 \mu\text{m}$, while the continuous geometry without offset added reaches $541.2 \mu\text{m}$. A small offset of $150 \mu\text{m}$ does not significantly improve the profile, with $L_{\text{uni}} = 549.2 \mu\text{m}$. In contrast, an offset of $350 \mu\text{m}$ gives a much better result, with $L_{\text{uni}} = 822.0 \mu\text{m}$. This shows that both the side distance d and the offset of the connection can be optimized together.

Overall, the side-electrode results show that the best uniformity is obtained when the current supply is removed from the rounded end and when the electrode connection is placed sufficiently far away from the pocket. The idealized side geometry provides an upper bound on the improvement that can be obtained, while the continuous geometries indicate the process constraints that would have to be respected in a real grid layout.

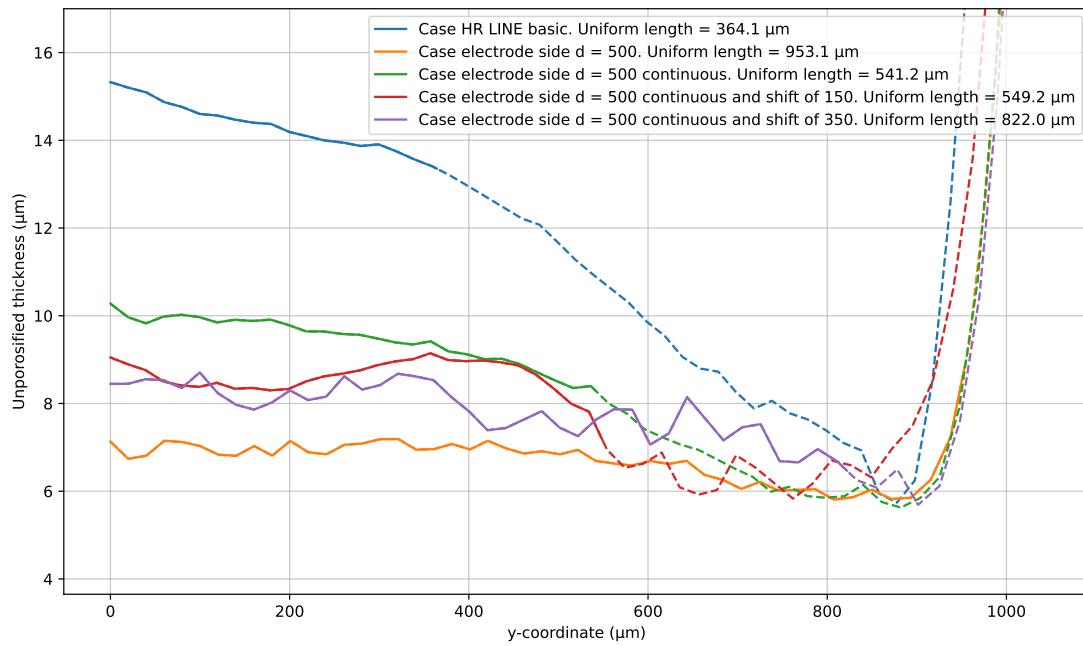


Fig 6.16. *Residual non-porosity silicon thickness for the "side" electrode geometries with $d = 500 \mu\text{m}$.*

6.6 Conclusion

The 3D simulations confirm that the finite geometry of the back-side opening can introduce a significant longitudinal non-uniformity in the porosification front. Even for a uniform-resistivity substrate, the current distribution is not equivalent to an extruded 2D case due to the finite length of the openings in the resist. The current is redistributed because of the rounded end of the pocket and the front receives a larger current density and therefore advances faster.

The direct introduction of detailed PN resistivity profiles in 3D remains numerically impractical because of the combination of sharp resistivity variations and high computational cost. Simplified rectangular PN patterns were also found to be unstable. A continuous high-resistivity layer was therefore introduced as an effective stopping pattern. This layer does not reproduce the local PN layout, but it provides a stable way to study how the macroscopic 3D geometry interacts with a stopping region close to the front-side.

The electrode geometry study shows that the non-uniformity can be reduced by limiting the current supply near the rounded end of the pocket. The notch geometry gives a moderate improvement, increasing the uniform length from $364.1 \mu\text{m}$ to $490.7 \mu\text{m}$. The cut geometries provide a stronger improvement, with the best case reaching $945.9 \mu\text{m}$, but they come with a loss of integration density. The side-electrode geometries confirm that removing the current supply near the rounded end is effective, but also show that the connection of the grid must be placed sufficiently far away to avoid reintroducing a local current path. For a grid distance of $250 \mu\text{m}$, the ideal side-electrode case reaches $944.6 \mu\text{m}$, while the best continuous

implementation reaches only 535.4 μm when the connection is shifted by 175 μm . Increasing the grid distance to 500 μm improves the continuous design: the ideal side-electrode case reaches 953.1 μm , and the best continuous implementation reaches 822.0 μm for a 350 μm connection shift.

These results suggest that the back-side grid should not only be designed to distribute the current uniformly across the wafer, but also to control the local current access around each porous opening. In particular, the region near the rounded end of the pocket should be supplied through a larger access resistance than the central part of the pocket. This conclusion provides a design guideline for future experimental layouts and motivates further simulations combining optimized grid geometries with more realistic PN stopping-layer profiles.

Chapter 7

Conclusion

7.1 Summary

This thesis investigated the possibility of integrating porous silicon in bulk CMOS substrates using a back-side post-process approach. It explored the use of P- and N-doped regions as an etch-stop layer to prevent the porous front from reaching the front-side devices while allowing sufficient penetration in the silicon substrate.

A first analysis of representative PN etch-stop layer candidates was performed using simulated resistivity maps. This analysis highlighted the central trade-off of the proposed approach. Closely spaced N-type regions and strong depletion barriers provide better front-side protection, but they may stop the porous front too early and leave a significant residual crystalline silicon thickness below the RF structures. Conversely, larger and more conductive P-type regions allow deeper PSi penetration and may therefore improve the effective RF properties of the substrate, but they also reduce the stopping margin. Within the assumptions of the resistivity-map analysis, the candidates with deeper P-type implantation appeared promising, because they could allow the porous front to approach the RF-active region before being strongly confined by the neighboring N-type regions.

The experimental results of Thibault Fiasse showed that the PN etch-stop layer influences the porosification front. Cross-sectional views confirmed that the porous front, depending on the candidate, can either stop too early or penetrate more deeply between the PN regions. Top-view observations also revealed a non-uniformity along the length of the porous pocket, with a larger lateral extension near the extremities caused by finite three-dimensional geometry of the back-side opening and of the metallic grid. RF measurements on CPW structures provided a first qualitative confirmation that the remaining silicon thickness and the penetration of PSi below the CPW are critical for the final substrate performance. They also suggested an improvement of the effective substrate parameters, with an effective resistivity above $1 \text{ k}\Omega \cdot \text{cm}$ obtained in the best measured configuration.

A 2D COMSOL model was developed to reproduce the porosification trends numerically. Simulations of porosification on uniform standard-resistivity wafer were performed to confirm the validity of the model. The PN resistivity maps were then introduced in the model to study the impact of the etch-stop layer. The residual non-porosified thickness was reduced from approximately $1.8\text{--}2\text{ }\mu\text{m}$ for the initial candidates to about $1.5\text{ }\mu\text{m}$ for the deep pn+ candidate with $W_p = 2\text{ }\mu\text{m}$, and to about $1.2\text{ }\mu\text{m}$ for the deep pn++ candidate with $W_p = 2\text{ }\mu\text{m}$. Within the assumptions of the model, these results suggest that the deeper P-type implantation candidates are promising for improving the compromise between front-side protection and PSi penetration.

Finally, the model was extended to three dimensions. This model allowed to characterize the influence of the finite-length of the opening over the uniformity of the porosification. To model the etch-stop layer in a computationally efficient way, a high-resistivity layer of $3\text{ }\mu\text{m}$ was implemented. The influence of the electrode geometry was then investigated with this HR layer. The uniform length L_{uni} was introduced as FoM, representing the distance over which the residual thickness remains within a tolerance Δh of the distance at the center of the pocket. The proposed changes in the electrode grid improved L_{uni} from $364.1\text{ }\mu\text{m}$ to $490.7\text{ }\mu\text{m}$ with the notch geometry. The cut geometries improved this value to $945.9\text{ }\mu\text{m}$, but because of their asymptotic character, these cases would reduce the integration density significantly. Finally, the best result for the non-asymptotic side electrode was obtained for a distance of $500\text{ }\mu\text{m}$ between the grid and the opening and with an added offset of $350\text{ }\mu\text{m}$, improving L_{uni} to $822.0\text{ }\mu\text{m}$. The realistic continuous side-electrode geometry therefore increases the uniform length by more than a factor of two compared with the reference geometry.

7.2 Limitations

Several limitations must be kept in mind when interpreting the results of this work. First, the porosification model is based on a primary current distribution formulation. This choice makes it possible to isolate the influence of geometry and resistivity on the current distribution, but it neglects interfacial kinetics, mass transport in the electrolyte, HF renewal inside the porous network, and gas production. As a result, the simulated time cannot be interpreted quantitatively, and the model should mainly be used to compare relative front shapes and current redistribution effects.

Second, the PN stopping layer is represented through fixed resistivity maps. This approach captures the expected blocking effect of high-resistivity regions, but it does not solve the semiconductor physics of the junctions during porosification. In particular, the depletion regions, carrier concentrations, and local potential distribution are not updated as the porous front approaches the doped regions.

Third, the numerical implementation remains limited by the moving mesh. Sharp resistivity

profiles imported from TCAD simulations are difficult to combine with large interface displacements, especially in 3D. For this reason, simplified resistivity patterns were used in several parts of the work, including the $1\text{ k}\Omega\text{cm}$ replacement of N-type regions in 2D and the continuous high-resistivity layer in 3D. These approximations are useful to identify trends, but they should not be interpreted as exact representations of the real PN structures.

Finally, the experimental interpretation is limited by the available samples and measurements. The RF results provide useful indications on the impact of PSi penetration and residual silicon thickness, but several parameters vary simultaneously between samples, including the porosification time. A fully quantitative correlation between a given PN candidate, the residual silicon thickness, and the extracted RF figures of merit would require a larger and more controlled experimental dataset.

7.3 Perspectives

This work could then be improved in many ways. A first perspective is to improve the electrochemical model. The primary current distribution model could be extended toward a secondary current distribution formulation including interfacial kinetics, or even toward a tertiary formulation including species transport in the electrolyte. Such developments would make it possible to investigate the influence of diffusion of reactants in HF, electrolyte renewal, and pulsed-current conditions. They would also make the simulated time and local porosification rate more physically meaningful.

A second important perspective is to couple the porosification model with a semiconductor model of the PN stopping layer. Instead of using fixed resistivity maps, the depletion regions and carrier distributions could be updated during the progression of the porous front. This would allow the bottleneck effect to be evaluated more rigorously and would help determine how the applied potential, doping profiles, and junction geometry influence the stopping behavior.

Finally, a numerical point of view, the robustness and efficiency of the simulations should also be improved. A more advanced meshing strategy, such as local adaptive refinement near the moving interface and the PN regions, could help resolve sharp resistivity variations without making the full 3D model prohibitively expensive. Improving the solver strategy would also reduce convergence failures and make it possible to perform broader parametric studies. This would be particularly useful for optimizing the PN geometry, the depth of the implanted regions, and the back-side grid layout as this would allow to test bigger parameter sets.

The electrode geometries proposed in the 3D simulations also deserve further investigation. The results suggest that the back-side grid should not only distribute the current uniformly across the wafer, but also control the local current access around each porous opening. In particular, reducing the current supply near the rounded end of the pocket appears to improve

the uniformity of the residual silicon thickness. Future layouts could therefore combine a globally conductive grid with local design rules that increase the access resistance near regions where porosification is naturally accelerated.

Finally, the most important perspective is experimental validation. Future samples should combine the most promising PN stopping-layer candidates, especially the deeper P-type implantation profiles, with optimized back-side grid geometries. This experimental validation is necessary to determine whether post-process PSi integration can become a realistic bulk CMOS-compatible strategy for RF performance enhancement.

Appendix A

Use of generative artificial intelligence

This thesis was written in accordance with the EPL guidelines for the responsible use of generative artificial intelligence. Generative AI tools were used as support tools only. The scientific content, simulations, interpretation of the results, and final wording remain my responsibility.

Generative AI was used for the following purposes:

- **Linguistic assistance:** AI tools were used to improve the clarity, grammar, syntax, and style of English text initially written by the author. They were only used to improve the readability and the starting text was always written without AI tools. No content was added by the AI. Structure and argumentation remain original work.
- **Initial explanations and brainstorming:** AI tools were used to obtain preliminary explanations of some physical or numerical concepts, and to help structure possible interpretations. These explanations were not used as primary sources; the scientific content was checked against the relevant literature, simulation results, and discussions with supervisors.
- **Code assistance for data visualization:** AI tools were used to help write and improve Python scripts used for plotting simulation results and extracting numerical metrics from the data. The generated code was reviewed, adapted, and tested before use.

No AI-generated text, code, or interpretation was used without verification and modification when necessary. Bibliographic references were not generated by AI without being checked manually against the original sources.

Bibliography

- Alicandro, S. (2023). “Experimental study of different shaped nanopores in a porous silicon cathodic exchange membrane for reverse electrodialysis”. Master Thesis. UCLouvain.
- Aroutiounian, V. M. and M. Zh. Ghulinyan (May 2003). “Electrical conductivity mechanisms in porous silicon”. In: *physica status solidi (a)* 197.2, pp. 462–466. ISSN: 00318965, 1521396X.
- Capelle, M., J. Billoué, P. Poveda, and G. Gautier (Dec. 2012). “RF performances of inductors integrated on localized p+-type porous silicon regions”. In: *Nanoscale Research Letters* 7.1, p. 523. ISSN: 1556-276X.
- Cathelin, A. (2017). “Fully Depleted Silicon on Insulator Devices CMOS: The 28-nm Node Is the Perfect Technology for Analog, RF, mmW, and Mixed-Signal System-on-Chip Integration”. In: *IEEE Solid-State Circuits Magazine* 9, pp. 18–26.
- Eminente, S., M. Alessandrini, and C. Fiegna (Apr. 2004). “Comparative analysis of the RF and noise performance of bulk and single-gate ultra-thin SOI MOSFETs by numerical simulation”. In: *Solid-State Electronics* 48.4, pp. 543–549. ISSN: 00381101.
- Fadel, C. (2025). “Wideband Characterization of Vanadium Dioxide for Millimeter-Wave Switch Applications”. Master Thesis. UCLouvain.
- Gautier, G. and P. Leduc (Mar. 2014). “Porous silicon for electrical isolation in radio frequency devices: A review”. In: *Applied Physics Reviews* 1.1, p. 011101. ISSN: 1931-9401.
- Ivanov, A. (2018). *Silicon Anodization as a Structuring Technique*. Wiesbaden: Springer Fachmedien Wiesbaden. ISBN: 978-3-658-19237-2 978-3-658-19238-9.
- Laurent, S. and E. Desbonnets (2011). *RF Substrate Technologies for Mobile Communications*. White paper. Accessed 2026-05-31.
- Lederer, D. and J.-P. Raskin (Mar. 2005). “Effective resistivity of fully-processed SOI substrates”. In: *Solid-State Electronics* 49.3, pp. 491–496. ISSN: 00381101.
- Matsusada Precision (Apr. 28, 2026). *Fundamentals of Ion Implantation: Processes and Equipment*. Published: 2025-07-28; updated: 2026-04-28. URL: <https://www.matsusada.com/column/ion-implantation.html> (visited on 05/28/2026).
- Nabet, M. (Feb. 2025). “Enhanced High-Resistivity Silicon-Based Substrates for RF and mmWave FD-SOI Circuits”. PhD thesis. Louvain-la-Neuve: UCLouvain.
- Rack, M. (Mar. 2021). “Modelling of Advanced Silicon-Based Substrates for RF and mm-Wave Applications”. PhD thesis. Louvain-la-Neuve: UCLouvain.

- Raskin, J.-P. (Apr. 2009). "SOI technology: An opportunity for RF designers ?" In: *Journal of Telecommunications and Information Technology*.
- Sailor, M. J. (2012). *Porous Silicon in Practice*. Weinheim: Wiley-VCH.
- Sarafis, P., E. Hourdakakis, and A. G. Nassiopoulou (Sept. 2013). "Porous Si dielectric parameter extraction for use in RF passive device integration: Measurements and simulations". In: *2013 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*. ESSDERC 2013 - 43rd European Solid State Device Research Conference. Bucharest, Romania: IEEE, pp. 99–102. ISBN: 978-1-4799-0649-9.
- Scheen, G. (July 2015). "Metal electrode integration and Palladium nanoparticle functionalization on a miniaturized macroporous silicon chemiresistor". PhD thesis. Louvain-la-Neuve: UCLouvain.
- Scheen, G., R. Tuyaerts, M. Rack, L. Nyssens, J. Rasson, M. Nabet, and J.-P. Raskin (June 2020). "Post-process porous silicon for 5G applications". In: *Solid-State Electronics* 168, p. 107719. ISSN: 00381101.
- Scheen, G., R. Tuyaerts, Q. Van Overmeere, and J.-P. Raskin (July 1, 2025). "Homogeneous Backside Porosification of Standard Silicon Wafers for Post-Fab Process Integration of Porous Silicon". In: *Journal of The Electrochemical Society* 172.8, p. 083503. ISSN: 0013-4651, 1945-7111.
- Tuyaerts, R., G. Scheen, K. Aouadi, M. Rack, and J.-P. Raskin (Jan. 2026). "Post-fab porous silicon in silicon-on-insulator substrates for improved radio frequencies performances". In: *Materials Science in Semiconductor Processing* 201, p. 110098. ISSN: 13698001.
- Vercauteren, R., G. Scheen, J.-P. Raskin, and L. Francis (Feb. 2021). "Porous silicon membranes and their applications: Recent advances". In: *Sensors and Actuators A: Physical* 318, p. 112486. ISSN: 09244247.
- Welty, R.J., S.H. Park, P.M. Asbeck, K.-P.S. Dancil, and M.J. Sailor (1998). "Porous silicon technology for RF integrated circuit applications". In: *1998 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems. Digest of Papers (Cat. No.98EX271)*. First Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems. Ann Arbor, MI, USA: IEEE, pp. 160–163. ISBN: 978-0-7803-5288-9.

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