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Design of an ultra-low-power always-on analog front-end for audio events detection in forests

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Abstract

The constant advances in integrated artificial intelligence (AI), low power electronics and increased network agility enable the deployment of connected smart sensor nodes exchanging data over the internet, also known as the Internet of Things (IoT). This extensive deployment raises ethical and environmental concerns. Sensor materials are rare and sometimes difficult to harvest. Besides, the e-waste generated by the replacement of each sensor is harmful to the environment. Each sensor needs to be autonomous, non-invasive and exhibit a long lifespan to prevent such issues. If design efforts are made to meet these constraints, the IoT could be profitable in ecosystem monitoring. Among these ecosystems, forests provide essential services and represent resources to protect in the context of climate change. This thesis is part of a larger project aimed at developing an automated acoustic sensor node monitoring several parameters of forest conditions. Because relevant sounds can happen at any time, an always-listening sensor is required. Nevertheless, keeping the entire sensor always awake is not a possibility due to the restricted power budget. For that reason, the purpose of this master thesis is to achieve the design of an ultra-low-power (ULP) analog-front-end (AFE), enabling the second stage of the sensing system when any relevant sound is detected.

First, a low-power MEMS microphone converts the acoustic wave into an electrical signal. It features -37 dBV sensitivity and a bandwidth spanning from 90 Hz to 16 kHz. Second, from the microphone specifications, constraints are set for the low-noise amplifier (LNA), which consumes 530 nW and provides a constant 30 dB gain across the microphone bandwidth. Afterward, the energy of the amplified signal is extracted by a 420 nW half-wave rectifier followed by a passive low-pass filter. Finally, the second stage of the sensing system is enabled whether the comparator at the end of the chain evaluates the signal energy as sufficient with respect to its comparison voltage. This last circuit consumes 66 nW and presents 4 mV hysteresis to prevent its binary output voltage from instability. The comparator is also provided with adjustable comparison voltages to avoid always toggle when the background noise increases. In this way, the AFE can adapt to distinct background noise levels. The aforementioned analog circuits use a single supply voltage of 600 mV. All their transistors operate in weak inversion for low power considerations.

The always-listening AFE (or always-on chain) senses sounds as low as 37 dB_{SPL} (minimum level of detection). It can enable the rest of the sensor for sound levels greater than 57 dB_{SPL} (minimum toggle level) and adjust this level depending on the background noise. The total power consumption of the proposed design is 1.02 μW, which is 437 times less than the previous AFE design proposed in the project on acoustic monitoring in forests. As a result, the always-on chain aligns with state-of-the-art voice activity detection (VAD) systems for the considered bandwidth. The main limitations of the proposed design are associated with the variation of performance with PVT corners and statistical variability. This will be thoroughly discussed in this work.

The design presented in this thesis exhibits promising results in the acoustic monitoring of forests thanks to its low power consumption and high bandwidth. If subsequent research follows the footsteps of this thesis, forests could be effectively monitored by ULP sensors in the near future, hence protecting their resources and limiting the impact of their degradation on the environment.

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Contents

Chapter 1

Introduction

Context

In recent years, there has been a growing interest in applications relying on the Internet of Things (IoT) to achieve ubiquitous sensing and processing. This terminology refers to a network of smart sensor nodes provided with the ability to exchange data over a wireless link. Nowadays, the IoT enables applications such as smart homes, intelligent transport, pollution control and ecosystem monitoring [1]. Still, many challenges remain to be addressed in the development of IoT networks, notably regarding the deployment method and materials employed for the sensor. Undeniably, the fast expansion of IoT nodes should be as non-invasive as possible and limit its environmental impact. Moreover, we expect each sensor to be energy-autonomous, exhibit a decade-long lifetime, have a low cost and require close to no external intervention [2]. As the energy source restriction limits the power budget in the microwatt range, the sensor node needs to sense data, process it locally, and transmit the preconditioned data afterward.

With the significant impact of human activities on natural ecosystems over the past few years, one emerging field of IoT is currently dedicated to acoustic monitoring in forests. Deforestation, soil pollution, and poaching indeed have an immediate impact on nutrient cycling mechanisms, soil fertility, plant physiology, and the natural habitat of endangered species [3]. In addition to providing data about poaching activities and the local environment, forest monitoring should prevent forest fires. As such, IoT could prove key to preserve millions of acres of forests from wildfires yearly [4].

Motivation

Two essential requirements are associated with acoustic monitoring in forests. First, detecting every acoustic event of interest. Second, relying on a very restricted power budget suiting the energy harvesting system and preserving battery lifetime. To avoid intensive power consumption, we could think of sensors that periodically sample their surrounding acoustic environments. However, the main challenge in sparse acoustic environments such as forests is to prevent missing relevant sounds, emphasizing the necessity for always-listening sensors as is the case in speech recognition systems [5].

The concept of always-on proportional sensing bridges the gap between low power consumption and an always-listening sensor [6]. As such, the sensor exhibits wake-on-sound properties and scales the power consumption of the sensing system with the complexity of the sensing operation. As a result, depending on the relevance of the sound, different blocks in the processing chain are enabled. Therefore, we have to consider what criterion to choose to assess the relevance and whether this criterion remains relevant across time. The ability to adapt to various acoustic environments evolving with time while maintaining the relevance of information is called context-awareness [7]. Context-awareness is essential in this application as the background noise level in forests may vary depending on the weather conditions. Voice activity detection (VAD) systems consider these key concepts, establishing a reliable basis for a study in state-of-the-art papers. All VAD systems are not based on these concepts but are still relevant to analyze for their low-power designs.

The selected relevance criterion in this work is the energy of the acoustic signal. The motivation of this work is to study an AFE that wakes on sound and enables the rest of the sensing system if the signal energy is sufficient. In addition, the AFE should try to minimize its power consumption through a custom design and an ultra-low-power (ULP) architecture.

Contribution

In the present work, we propose an ULP always-on (AO) chain for detecting acoustic events specific to forest environments. Viewed as a black box, the chain outputs a single bit when the sound energy is sufficient. It exhibits the features stated in the preceding paragraph: always listening to the surrounding acoustic environment while presenting context-awareness. To achieve these goals, we rely on current VAD systems architectures to propose the top-level design of the AO chain. Furthermore, we cautiously study state-of-the-art papers in the fields of audio sensing and biomedical applications to find appropriate low-power topologies for the distinct circuits in the chain.

The main figures of merit (FoMs) for all circuits are identified to provide appropriate sizings. When possible, sizings are based on an analytical model. Otherwise, an iterative sizing is adopted to obtain the most suitable circuit implementation. If the results do not meet the circuit specifications, we pave the way for further improvements and discuss the challenging trade-offs. We achieve the AO chain starting by converting the acoustic wave into an electrical signal using a microphone. The microphone is then interfaced with a low-noise amplifier (LNA) to amplify this signal. Afterward, the energy detection is achieved by a rectifier followed by a low-pass filter. Finally, a comparator evaluates the signal at the low-pass filter output and toggles whether it exceeds a given threshold. Statistical variability and PVT corner simulations have been performed to assess the robustness of each circuit.

As part of a more extensive project, the AO chain affords as much flexibility as possible in its implementation through a comprehensive discussion of the main circuit trade-offs. This feature is particularly desirable if additional constraints are changed later on for acoustic monitoring in forests. This work does not propose a validation via tape-out-based measurements. We implemented the main circuits of the AO chain with layout simulations.

Structure

Chapter 2 studies papers in the field of acoustic monitoring in forests and state-of-the-art VAD systems papers. The top-level design of the AO chain is established as a result of this research. In addition, general design considerations for the analog circuits through the chain are provided.

Chapter 3 details the characteristics of the acoustic environment in forests to set the specifications for the microphone. This chapter closes with selecting the best-suited microphone for this application and measurements of its power consumption.

Chapter 4 provides the analytical model of the LNA in both ideal and non-ideal cases, concluding with the expected requirements for this circuit.

Chapter 5 deals with the design and implementation of the operational transconductance amplifier (OTA) in the LNA. The first sizing is obtained thanks to g_m/I_D methodology and is further optimized employing a genetic algorithm to meet the IRN and bandwidth requirements of the LNA.

Chapter 6 presents the design of a pseudo-resistor employed as the feedback resistor in the LNA. A low high-pass corner is expected for this circuit, pointing out the need for a large feedback resistance value.

Chapter 7 deals with the design and implementation of a low-power half-wave rectifier suited for audio applications. This circuit is essential for energy detection when followed by a low-pass filter.

Chapter 8 closes the design process by providing the design and implementation of an hysteresis comparator. The comparator is responsible for the decision based on the signal energy. The concept of hysteresis will be thoroughly discussed.

Chapter 9 performs a transient noise analysis of the AO chain to assess its performance for the minimum acoustic toggle level. Afterward, a comparison between the proposed design performance, state-of-the-art VAD systems and the previous AFE design for this project is realized. This chapter also discusses the strengths and weaknesses of the AO chain to bring a discussion on further improvements.

Chapter 10 closes this thesis by summarizing the key steps in the design process and the main performance of the AO chain.

Chapter 2

Top-level design

In this first chapter, we study acoustic monitoring systems in forests and state-of-the-art VAD systems to establish the top-level design (TLD) of the AO chain. The state-of-the-art search in Section 2.1 yields the TLD architecture presented in Section 2.2. General considerations for the design of analog circuits in the AO chain are then presented in Section 2.3.

2.1 State-of-the-art papers

Acoustic monitoring in forests

Current works on acoustic monitoring systems in forests mainly aim to collect acoustic samples but are not yet deployed employing low-power IoT nodes that process data locally and feature sound classification. In [8] for instance, sensors are programmed to analyze the entire soundscapes in forests continuously over predefined periods. This work aims to bridge the gap between on-the-ground surveys and the bird-eye view of satellites, hence monitoring animal biodiversity. In [9], the authors present a methodology to prevent illegal poaching activities. The proposed system samples the acoustic environment periodically with intervals of 15 seconds thanks to a Raspberry Pi-connected microphone and sends an alarm if the recorded sound matches the features of poaching activities. However, this system has not been tested in real conditions and shows limited performance due to its poor database. Finally, in [10], the SAFE (Stability of altered ecosystems) organization presents a fully automated, real-time, eco-acoustic monitoring network that continuously transmits compressed audio files to a remote FTP server using a 3G mobile internet connection [10]. This latter work focuses on establishing a comprehensive set of acoustic samples but is limited to a precise area in Borneo's tropical rain forests.

These papers provide little information about the employed design for the sensor but instead focus on the harvesting of acoustic data, networking and machine learning aspects. For instance, none detail the AFE design or microphone choice for their systems. Besides, the concepts of proportional sensing and context-awareness developed in the introduction are not mentioned. Therefore, it is more appropriate to investigate another field for reference papers presenting detailed topologies suited for implementing a low-power, always-listening AFE. This is the case of the VAD systems developed next.

Voice activity detection systems

VAD systems always listen to their surrounding acoustic environments and aim to detect a relevant sound, in that case, human voice. If the sound turns to be relevant, the VAD system enables power gating of higher-level speech tasks such as speaker identification and speech recognition [11] granting the establishment of voice-user interfaces. As VAD systems are inherently batteries-powered systems, the search for ultra-low-power architectures has driven extensive researches in this field during the past decade.

In 2015, a 90nm CMOS VAD based on the concept of proportional sensing was proposed in [6]. The system dynamically adapts sensing resources to signal information content and context, hence only dedicating energy to relevant information extraction. It features 6 μW power consumption. Later, in 2017, the first paper demonstrating a fully functional 4.7 μW audio sensor node in millimeter-scale size, including recording, storage, and transmission of the recording over a 20m wireless link[1] was introduced in [12]. The year after, the architecture proposed in [13] achieved a 1 μW speech/non-speech recognition employing analog signal processing for acoustic feature extraction, event-driven analog-to-digital conversion, and a digital deep neural network for the speech/non-speech classification task. More recently, in 2019, power consumption was further reduced in [14]. This paper proposes a 142 nW programmable, neural network-based acoustic sensing system for VAD and non-voice event detection. Finally, the most stringent power consumption in VAD systems was obtained in [15] with a 12 nW power consumption. The key element for such meager power consumption is the low target bandwidth constraint below 0.5 kHz, enabling a 1 kHz clock signal for all active components. Even if the power consumption is attractive in this paper, the proposed architecture is not necessarily suited for processing voice signals.

Except for the last mentioned paper, all VAD systems aim at 4-5 kHz bandwidth as the human voice cannot go above this frequency range. It is also important to stress that the specified power consumption values do not correspond to the AFE of the design but to the total power consumption of the VAD system. Only the power consumption of the AFEs of these designs will be kept to produce a meaningful comparison with the results of this work. Also, we need to bear in mind that the sounds produced by the human voice are distinct from the acoustic environment in forests. Chapter 3 will be devoted to the formulation of new constraints suited for acoustic content in forests.

[1]This paper does not strictly present a VAD system but rather an audio sensor more generally. It has nevertheless been included in the state-of-the-art search for the sake of comparison because it is mentioned in several VAD systems papers.

2.2 Top-level design

The search in VAD systems state-of-the-art papers provides significant guidelines for the TLD architecture and the expected power consumption. The design presented in Fig. 2.1 gets mostly inspired by [6] in order to provide the sensor with proportional sensing feature and adaptability to the background noise. Consequently, only the power of the microphone, the AO chain and deep sleep mode of the microprocessor unit will be consumed when the acoustic environment surrounding the sensor is irrelevant. The AO chain should aim at sub-microwatt power consumption to align with state-of-the-art VAD systems. Hence, the maximum power budget has been set to 1 μW. The TLD architecture was expressly chosen to be uncomplicated to re-implement if the final constraints for the sensor need to be reviewed. As stated in the introduction, the notion of flexibility in implementing the AO chain has been at the heart of this work to ease further research on the final sensor design.

The working principle of the AO chain is straightforward. The purpose of the microphone is to convert an acoustic wave into an electrical signal. However, to cope with the weak signal amplitude at the microphone output, a gain stage is typically required. Thus, an LNA interfaces the microphone to ensure enough signal amplitude. Once amplified, the energy detection is achieved through a rectifier ensued by a low-pass filter (LPF). It results in a DC signal representing the average of the rectified signal. Finally, the decision stage, a comparator, toggles whether this signal is above a given comparison voltage. As the acoustic environment in forests is prone to background noise variation, context-awareness can be achieved by setting variable comparison voltages at the comparator input.

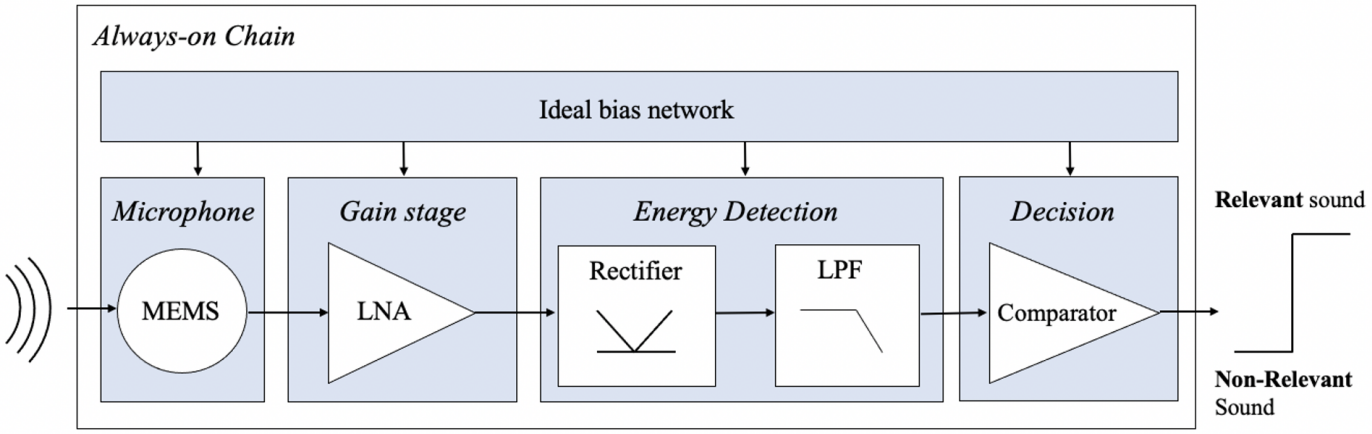


Figure 2.1: Proposed architecture for the top-level design of the always-on chain

2.3 General design considerations

This section contains general considerations for the analog block designs in the AO chain. The goal is to avoid repeating these considerations in each new chapter.

Employed technology

All the designs presented in this work are realized using the 65nm low-power (LP) CMOS process from Taiwan Semiconductor Manufacturing Company (TSMC).

In addition, low-V_{th} MOS transistors have been employed in the Eldo Spice simulator for the following blocks: the main OTA, rectifier, and comparator. To support this choice, simulations showed that standard-V_{th} MOS transistors leave their zone of operability more quickly when operating in very low inversion for this technology.

Single supply voltage

A single ideal supply voltage was considered for all the AO chain analog blocks. As a result, these can be efficiently powered from a single cell. The low supply voltage is $V_{DD} = 0.6\,V$. It is critical to emphasize that this does not concern the microphone, whose supply voltage is set by the manufacturer.

The main issue associated with the implementation of low-supply voltage analog circuits is the threshold voltage. With technology scaling, the threshold voltage decrease is not as fast as the voltage supply reduction [16]. Operating in a sub-threshold regime allows coping with the threshold voltage issue. This operation regime is discussed in the following subsection.

Weak inversion

Low-power designs often translate in transistors that operate in a sub-threshold regime where the channel is weakly inverted. When $V_{GS} < V_{th}$, channel charge drops exponentially with decreasing gate-to-source voltage, which is not predicted by the strong inversion model that concludes zero inversion charge. In this operating regime, the current flows by diffusion rather than drift as there is not enough charge in the channel to generate a significant electric field to pull electrons from source to drain [17]. Even though electrons concentration is small, it increases exponentially with gate bias [18]. The known expression for the drain current in weak inversion is the following [19, 20]

$$I_{DS} = I_S \cdot \left(\frac{W}{L}\right) \cdot e^{\left(\frac{V_{GS}-V_{TH}}{n \cdot U_T}\right)} \cdot \left[1 - e^{\frac{-V_{DS}}{U_T}}\right], \tag{2.1}$$

with I_S the characteristic current, n the sub-threshold slope factor and U_T the thermal voltage. This expression is used in all important models (EKV [21] or BSIM [22]) because of its

precision. While this can be seen as an undesirable side effect in the form of leakage in digital designs, weak inversion appears as an adequate transistor mode for targeting micropower analog circuits supplied by low voltage. Moreover, weak inversion is an efficient operating region benefiting from high transconductance-to-current ratio inducing high gain designs at the expense of speed due to low currents.

Equation 2.1 indicates that the transistor will be in saturation at 25°C, given that

$$V_{dsat} > 4 \cdot \frac{kT}{q} \approx 100\,mV\,, \tag{2.2}$$

where k is the Boltzmann constant, q the elementary electric charge of an electron and T the temperature in Kelvin.

Layout considerations

The principal circuits of the AO chain have been realized in layout to have more precise insight into their performance. Therefore this work provides the layout of the main OTA in the LNA, the rectifier and the comparator. This section aims to summarize the layout considerations that have been taken into account.

As far as possible, the transistors that need to be matched are organized in a common centroid structure. This matching technique split the transistors into several fingers and arrange these according to a pattern [23]. The purpose is that the centroid of each device matches to form a common one. The array of devices should be as compact as possible with ideally the same orientation for the devices. Hence, the common centroid technique is typically used for differential pairs and current mirrors for which matching is essential. The use of the Module generator tools from the Cadence Virtuoso design platform allowed a quicker implementation of common centroid structures.

It is also convenient to consider one metal layer for the vertical connections and another one for horizontal connections as a rule of thumb. An important consideration to consider is the crossing of distinct metal layers as these form parasitic capacitances. Even if the crossing of two metal layers is sometimes inevitable, design efforts have been made to reduce it. A compact layout is also beneficial for area-saving purposes and limiting the lengths of metal lines yielding large parasitic resistances.

The proposed layouts through this work have not been realized by taking into account the potential thermal gradient issues, common centroid implementations for the capacitors, interdigit connections for the resistors and the integration of dummy transistors (that allows for each transistor to see the same environment in a common centroid organization). The performed parasitic extraction is *C+CC*. It considers the capacitances between each node and ground, and the coupling capacitances between the different nodes.

Chapter 3

Acoustic environment in forests and microphone choice

This chapter studies the characteristics of the acoustic environment in forests to establish the specifications for the microphone. These specifications and the low power consideration allow selecting the most suitable microphone for the AO chain.

Section 3.1 is dedicated to sound propagation and the primary sound sources in forests. This allows setting bandwidth constraints for the microphone and the minimum level of detection. The concept of A-weighting, a central metric in the audio field, is also detailed. In Section 3.2, the main figures of merit of a microphone are described. The selection methodology and the selected microphone are provided in Section 3.3. Finally, Section 3.4 ends this chapter with measurements in order to assess the impact of a sound with huge amplitude on the power consumption of the chosen microphone.

3.1 Sound characteristics and acoustic environment in forests

Sound characterization and propagation

A sound is a physical phenomenon caused by fast pressure variations propagating through the air and can be sensed by a sound level meter. As the sound wave travels, the air is locally compressed, and expanded [24]. The elementary acoustic event is a sinusoidal wave at a given unique frequency called simple harmonic vibration. It is characterized by three essential parameters: a frequency (associated with the tone), an amplitude (associated with the loudness), and a duration. A measure of these three key parameters allows describing a sinusoidal tone fully.

Among the different metrics that characterize the amplitude A of a sound, the most common is the logarithmic value of the root mean square (RMS) of the amplitude relative to a

reference value. This metric is referred to as the sound pressure level (SPL)

$$L_p = 20 \log \left(\frac{p}{p_0} \right) \qquad [\mathrm{dB_{SPL}}] \,, \tag{3.1}$$

where $p = \frac{A}{\sqrt{2}}$ and $p_0 = 20\,\mu Pa$, the reference RMS pressure. We present typical sound sources and their corresponding value in dB_{SPL} in Table 3.1 [25].

Sound source	**Sound pressure level**
Rustling leaves in the distance	10 dB_{SPL}
Quiet library	40 dB_{SPL}
Conversational speech (1 meter away)	65 dB_{SPL}
City road (5 meters away)	80 dB_{SPL}
Chainsaw (1 meters away)	110 dB_{SPL}

Table 3.1: Source sources and their corresponding sound pressure level (expressed in dB_{SPL})

Due to the permanent compression and expansion of air as the sound wave travels, amplitude loss occurs. A logarithmic decrease of loudness provides the simplest model for representing sound propagation according to

$$L_{p,2} = L_{p,1} + 20 \log \left(\frac{r_1}{r_2} \right) \qquad [\mathrm{dB_{SPL}}] \,, \tag{3.2}$$

with $L_{p,1}$ (resp. $L_{p,2}$) being the perceived loudness at distance r_1 (resp. r_2). It is worth noticing that the model proposed in Eq. 3.2 represents a simplified version of sound propagation. In forest environments, some obstacles can scatter, reverb, or even absorb some sound frequency. Numerous models have been proposed to enhance the simplified version of sound propagation in a forest, such as the ISO 9613-2, Nord2000, CNPE, and RT-forest, documented in [26]. For instance, the RT-forest model considers the attenuation due to atmospheric absorption, ground, scattering, and a combination of reverberation and divergence. Interesting results have shown that forests behave like rooms. These show reverberation features that turn to be beneficial for some frequencies propagating into the air. The specific structure of forests explains this: the sound energy is trapped under the canopy due to horizontal backscatter from the tree trunks and vertical scatter from the underside of the canopy.

A-weighting

Sound amplitude is often provided in dBA units in the audio sensor papers or datasheets provided by the manufacturers. The A-weighting curve is a standardized curve applied to instrument-measured sound levels to imitate human perception of the sound [27]. Indeed, the human ear does not perceive sound linearly with frequency. We are more sensitive to high frequencies and less to low frequencies.

Practically, A-weighting is achieved by adding a table of values listed by octave bands to the measured sound pressure levels. The A-weighting curve is shown in Fig. 3.1. As a result of the weighting process, a sound measured in dBA cannot be converted back in dB_{SPL} if the spectral content in each band is not presented. Nevertheless, if the sound is a simple harmonic vibration, the conversion is possible, given that we know its frequency. In addition, note that the weight value is zero at 1 kHz. At this particular frequency, dB_{SPL} and dBA are equivalent.

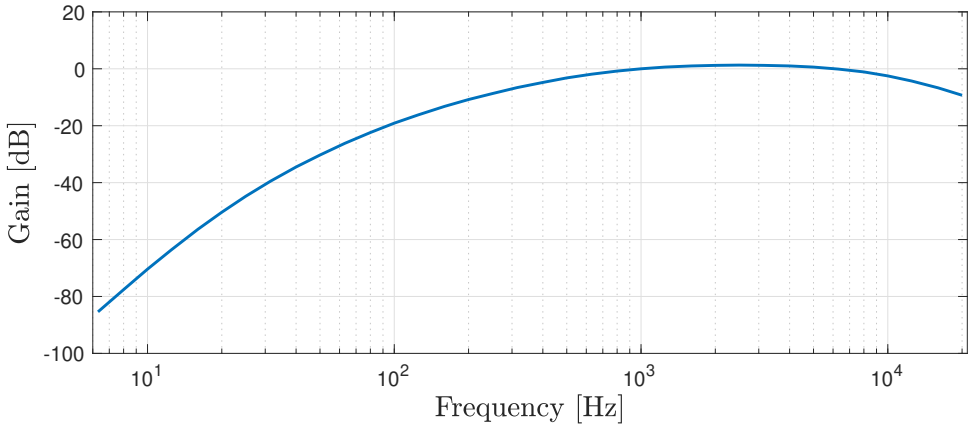


Figure 3.1: A-weighting curve. This curve covers a range from until 20 kHz corresponding to the maximum frequency that a human ear can perceive.

Acoustic environment in forests

To orientate the search for an adequate microphone, we first need to evaluate the primary sound sources in forests. As a wide diversity of sounds exist in such environments, it is helpful to use spectrograms because they offer a clear visualization of the spectral content of a sound over time.

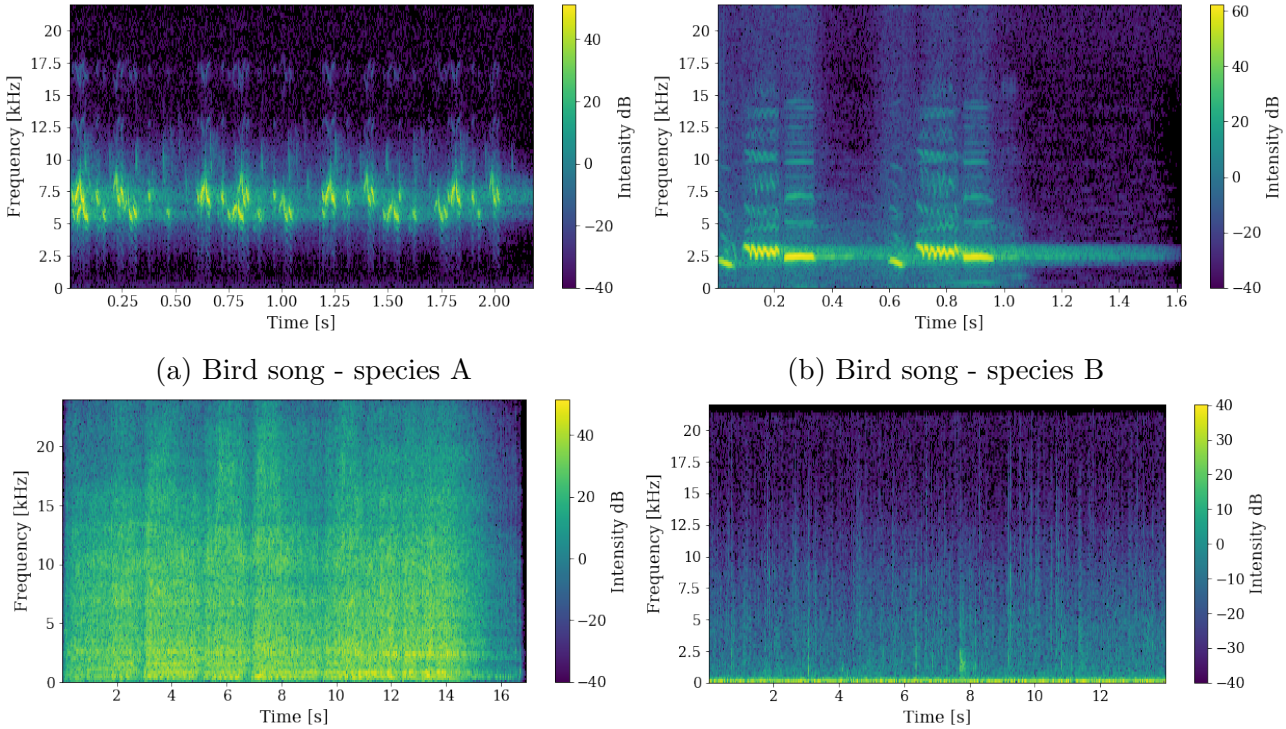
1. **Birds songs** often range from 1 kHz to 8 kHz [28]. However, as can be stated in Fig. 3.2a and 3.2b, spectral content is found at higher frequencies corresponding to the harmonics of the fundamental tones. These harmonics are the signature of the bird songs and help to characterize them. From this analysis, we firstly assert that the bandwidth performance of VAD systems ($f_{max} \approx 5\,kHz$) is not adequate for acoustic monitoring in forests. Secondly, we hypothesize that a bandwidth **higher than 15 kHz** is sufficient to identify a bird from other sound sources and feature species classification thanks to the higher harmonics spectral content.

2. **Poaching activities** involve the use of motorized equipment such as chainsaws which are characterized by a loud ($100 - 120\,dB_{SPL}$) [29] and rich harmonic sound. This is depicted in Fig. 3.2c which clearly shows that the entire spectral content is covered. Due to this typical characteristic, poaching activities are not challenging to discriminate from other sound sources.

3. **Wild forest fires** possess a spectral content characterized by a low-frequency tone interrupted by spikes crossing the whole spectrum. These correspond to cracking wood under the effect of combustion as illustrated in Fig. 3.2d. The low-frequency segment typically lies between 30 and 80 Hz suggesting that the high-pass corner of the microphone bandwidth should be as minimum as possible to capture those frequencies.

4. **Background noise level** in forests is difficult to characterize as it depends on the weather conditions, the season and the hour of the day. Studies have shown that the average background noise in forests is around 35 dBA to 40 dBA [30].

   Despite a direct mapping between dBA and dB_{SPL} is not achievable, we hypothesize that the background noise in forest environments is around 40 dB_{SPL}. This assumption is supported by the presented values in Table 3.1 and other papers comparing distinct sound amplitudes in dB_{SPL} [31]. As a result, the most appropriated minimum acoustic level of detection for the microphone is $\mathbf{L_{p,min} = 40\,dB_{SPL}}$.



(a) Bird song - species A

(b) Bird song - species B

(c) Chainsaw

(d) Forest fire

Figure 3.2: Spectrograms of the most common sound sources in forests. Bird songs typically cover a spectral content up to 15 kHz. A chainsaw sound covers the whole spectrum. Forest fires are characterized by a low-frequency component and spectral spikes. The intensity indicated along each spectrogram does not correspond to the initial sound intensity as the recording biases the actual sound pressure level.

3.2 Main figures of merit of a microphone

Sensitivity

The sensitivity defines the electrical response at the microphone output to a given standard acoustic input and can be seen as the microphone transfer function. A microphone with a high sensitivity allows detecting sounds with low amplitudes. Standard conditions refer to a 1kHz sine wave at 94 dB_{SPL}, corresponding to 1 Pa [32]. A microphone sensitivity is measured in $\frac{mV}{Pa}$. It can also be expressed in dBV, that is, decibels with reference to 1 V_{rms} as [1]

$$S = 20 \cdot \log_{10}\left(\frac{S_{mV/Pa}}{V_{out,REF}}\right) \qquad [\text{dBV}]\,, \tag{3.3}$$

with $V_{out,REF}$ being the 1 $\frac{V}{Pa}$ reference output ratio.

Power consumption

Datasheets provide the typical supply voltages and supply currents for a microphone. These values are given separately as their product is not considered as the microphone power consumption. The reason is that the product between the supply current and supply voltage only indicates a rough evaluation of the power consumption because several supply currents can be used for the same supply voltage, for instance.

Signal-to-Noise ratio

Conventionally, the SNR denotes the ratio between a reference signal (1kHz, 94 dB_{SPL}) and the noise level at the microphone output. The SNR value in datasheets is often provided in dBA as the output noise of the microphone is measured in a quiet anechoic chamber and the A-weighting curve presented earlier is applied to it [32]. In order to compare different microphones based on their SNR, it is imperative to check that these have been obtained with the same weighting and bandwidth range.

Equivalent input noise

This value represents the output noise level of the microphone brought back to the microphone input as a theoretical external noise source. It is expressed in expressed in dB_{SPL}. The equivalent input noise (EIN) value can be immediately found based on the SNR according to

$$EIN = 94\ dB_{SPL} - SNR \qquad [\text{dB}_{\text{SPL}}]\,. \tag{3.4}$$

An audio wave whose amplitude is below the EIN cannot be sensed as it lies below the microphone noise floor.

[1] One must be careful with this definition because it is only valid for analog microphones. The definition for a digital microphone changes as the sensitivity is given in $dBFS$, dB with a full-scale digital output.

Acoustic overload point

The acoustic overload point (AOP) is the value in dB_{SPL} at which the total harmonic distortion on the microphone output equals 10 %. A clipping point is reached beyond this acoustic value, and non-linear distortion effects impact the output signal quality. The difference between the AOP and EIN in dB_{SPL} is equivalent to the microphone dynamic range (DR)

$$DR = AOP - EIN \qquad [\mathrm{dB_{SPL}}]\,. \tag{3.5}$$

Frequency response

The frequency response is defined as the range between the -3 dB low-pass (LP) corner and the -3 dB high-pass (HP) corner of the microphone. The reference level is set at 1 kHz and normalized at 0 dB. The frequency response of a microphone essentially describes the behavior of output levels across the different frequencies. If the frequency response is not flat, distortion is introduced. For specific applications, this might have to be taken into account.

The frequency mask representing the maximum and minimum output level values across frequency is also typically provided in datasheets. The microphone output is therefore guaranteed to fall in this mask.

Directionality

The directionality of a microphone describes how the microphone sensitivity is changing when moving a sound source around the microphone. Directionality is often described as a pattern. Omnidirectional microphones are a particular case for which the sensitivity does not change according to sound provenance in space.

Power supply rejection

The ability of a microphone to reject noise present on the supply pin from the output signal is referred to as power supply rejection (PSR). Typical conditions to measure the PSR require adding 100 mV peak to peak square wave at 217 Hz onto the supply voltage and no acoustic input. The PSR is then measured, A-weighted and integrated over a 20 kHz bandwidth. An ideal microphone should have a PSR value equal to the A-weighted noise floor, meaning that the noise from the supply voltage is completely rejected. The 217 Hz value is chosen for historical reasons since, in GMS applications, the 217 Hz switching frequency is typically dominating noise on the supply voltage [32].

Another metric called power supply rejection ratio (PSRR) is also found in standard microphone datasheets. This metric also defines the ability to suppress noise from the supply voltage. However, measurement conditions are slightly different. PSRR values are not A-weighted and measured by adding a sine wave on the supply voltage rather than a square wave.

3.3 Microphone selection

With a clear idea of the different FoMs in mind, the main manufacturers have been identified: *Knowles*, *Sonion*, *Infineon*, *InvenSense*, *PUI audio* and *DB Unlimited*. The market for microphones is various, and the joined offer of the distinct manufacturers embodies thousands of microphones. Therefore, it is essential to proceed systematically in the choice of the final microphone. For that purpose, the main FoMs have been split between requirements and expected performance to guide the search.

Requirements

1. **Directionality:** We need an omnidirectional microphone as the surrounding acoustic environment of the microphone is of interest.

2. **Price:** A sufficient number of nodes is required to implement an efficient IoT network. Therefore it is of utmost importance that the individual cost of each sensor does not exceed a given threshold. The maximum price threshold for the microphone has been set to 5€.

3. **Bandwidth:** In Section 3.1, we assumed that the LP corner of the microphone needs to be higher than 15 kHz to sufficiently capture the harmonics of a bird song. Indeed, a shorter bandwidth would penalize the performance of an algorithm implementing species identification[2].

Expected performance

1. **Power consumption:** The battery-powered design considered in this application indicates low power consumption as a critical specification. The selected microphone should exhibit as low power consumption as possible.

2. **Sensitivity:** High sensitivity is desirable because the sound environment in forests is typically quiet. In a forest, the sound source may be far away from the microphone input resulting in a low sound amplitude according to Eq. 3.2.

3. **EIN:** This metric should be as small as possible since it determines the microphone minimum acoustic level of detection. An EIN similar to the background noise in the forest should be pursued. This value should be at least under 40 dB_{SPL} according to Section 3.1.

4. **Size:** The most compact design possible is desirable.

[2]This assumption was discussed with Thomas Delsart, who also does his thesis on acoustic monitoring in forests but rather focuses on the machine learning aspect. With a cut-off frequency of 8 kHz, promising results were obtained to distinguish sounds in forests (poaching activities, birds, gunshots). Nonetheless, we make the common assumption that a higher cut-off frequency is required to obtain an algorithm featuring bird species classification.

Selection methodology

The two first requirements are not particularly restrictive. Numerous microphones available on the market feature omnidirectional sound patterns while being affordable. However, the bandwidth requirement allows discarding the microphones usually chosen for VAD systems which rather target lower bandwidth (4-5 kHz). This requirement also eliminates the possibility for a passive microphone as these hardly exceed an LP corner around 7 kHz. A typical passive microphone is the BJ-21590-000 produced by Knowles used in a VAD system in [33]. The main interest of passive microphones relies on the fact that they have no active circuitry and theoretically do not require power to operate. However, considering the expected performance, this type of microphone exhibit low sensitivity and are often more expensive than active microphones.

Although power consumption is not included as a requirement, microphones whose current consumption exceeds 100 μA have not been discarded as the design effort to implement a low-power AFE would be completely insignificant compared to the power consumption of the microphone alone. This constraint typically rejects most electret microphones available on the market since their current consumption lies in the hundreds of μA order of magnitude. The AOM-5024L-HD-R produced by PUI-Audio was used in an early version of the sensor [34] but must be discarded for power saving purposes.

Having removed passive microphones and those whose current consumption exceeds 100 μA, the search for a microphone suitable for the acoustic environment in forests leads to the category of microelectromechanical systems (MEMS) microphones. Indeed, these microphones present low power consumption, high sensitivity and are rather compact and affordable. Making a point on sensitivity and power performance, we have found models like the O8AC03 by Sonion and the ICS-40310 by InvenSense. A choice in favor of MEMS microphones is supported by the state-of-the-art VAD papers mentioned in Section 2.1 [12, 13, 14, 15] and other papers dedicated to audio sensing [35].

Finally, the VM1010 is a particular model of microphone manufactured by Vespers, which was also studied. This MEMS microphone exhibits a sound wake-up feature thanks to the piezoelectric effect that make the acoustic transducer work like an acoustic switch. When a sound wave moves a piezoelectric cantilever, this motion creates a voltage via the piezoelectric effect [36]. Afterward, the voltage is sensed by an ultra-low-power comparator circuit, which sends a wake signal to the rest of the system [37]. Unfortunately, this technology does not offer enough bandwidth for the requirements. Moreover, the manufacturer fixes the acoustic thresholds that the microphone can detect and the lowest one is rated at 65 dB_{SPL}, which is higher than the 40 dB_{SPL} target in this work. However, this microphone based on the energy of the sound itself for its activation should be closely followed. It could give excellent performance in the future in the field of ultra-low-power always-on audio sensing.

A detailed comparison between the microphones discussed in this subsection is presented in Table 3.2. This table highlights the ICS-40310 by InvenSense as the best candidate for the microphone choice as it fits all requirements while offering the best compromise among the

expected performance. This model features a bandwidth higher than 15 kHz and an EIN of 30 dB_{SPL}, which meet our specifications. However, this microphone has an HP corner at 90 Hz, which prevents detecting the low-frequency component of wild forest fires.

Performance	AOM-5024L-HD-R	O8AC03	BJ-21590-000	VM1010	**ICS-40310**
Type	Electret	MEMS	Passive	MEMS	MEMS
Sensitivity [dBV]	-24±3	-38±1	-55±3	-38±3	-37±3
SNR [dBA]	80	65	/	60.5	64
Current supply [μA]	500	31	/	10	16
Rated voltage [V]	3	0.9	/	1.8	0.9
Frequency response	20-20kHz	90-20kHz	300-5kHz	100-10kHz	90-16kHz
Unit price	2.6€	NA	26.2 €	1.65 €	2.4 $
Volume [mm^3]	369	8.2	178	14.4	8.2
Omnidirectional	Yes	Yes	Yes	Yes	Yes

Table 3.2: Comparison of different microphones. The best model for this work is the ICS-40310 from InvenSense.

3.4 Power consumption measurements

This latest section investigates the influence of a high sound amplitude on microphone current consumption. Analyzing the dynamics of power consumption is interesting because it is usually not given in the datasheets. A typical supply voltage of 1 V has been provided to the microphone, and current consumption has been measured. The sound source is here a whistling near the microphone that can be fairly evaluated at 90 dB_{SPL} level, at a 10 cm distance. We observe in Fig 3.3 that the current consumption of the microphone does not surge when it is located close to an intensive sound source. The variation in the current represents 5.5% of the mean supply current at 18.25 μA. Given the supply voltage value, the power consumption is thus 18.25 μW on average. The supply voltage noise is typically due to the measuring instruments and could considerably decrease by considering a stable on-chip power supply with more reliable connections than those used for the setup.

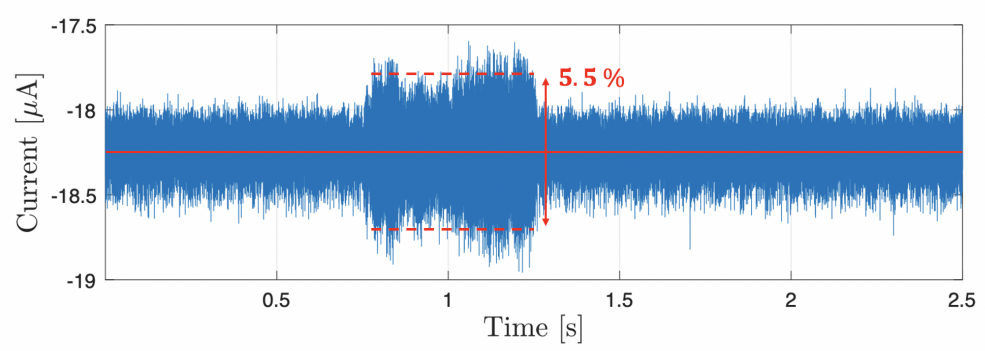


Figure 3.3: Current consumption for a 1 V supply voltage. We observe a deviation of 5.5% with respect to the mean supply current. Hence, the power consumption of the microphone does not surge when it is close to a high amplitude sound.

Chapter 4

Gain stage - Low-noise amplifier

In the previous chapter, we have chosen a suitable microphone for the AO chain. In this chapter, we detail the topology of the LNA interfacing the microphone. The transfer function of this circuit should exhibit a band-pass response to amplify the signal from the microphone with the same gain from 90 Hz to 16 kHz (the microphone frequency response).

Fist, Section 4.1 details the transfer function of the LNA for both ideal and first-order amplifiers. Second, Section 4.2 provides the expected performance for the LNA based on the microphone specifications and reasonable assumptions. Finally, Section 4.3 determines the expected resistor and capacitor values for this circuit.

4.1 LNA transfer function

We have chosen a topology for the LNA same as in state-of-the-art VAD systems papers presented in Section 2.1. This topology is illustrated in Fig. 4.1.

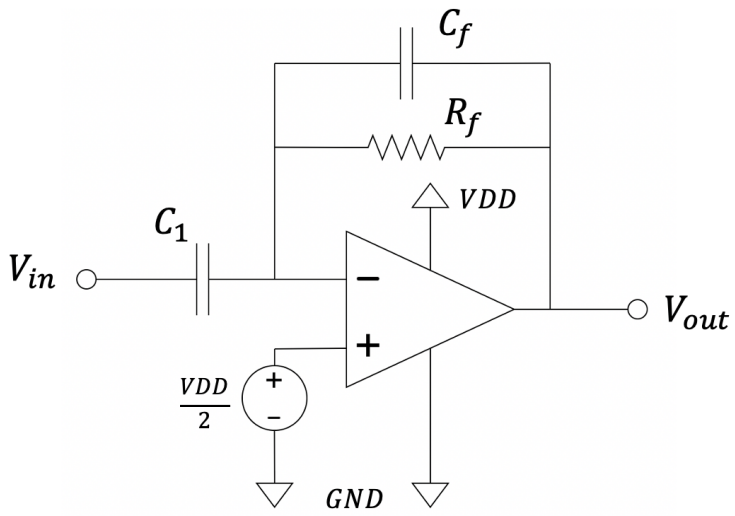


Figure 4.1: Topology of the low-noise amplifier

Transfer function with an ideal amplifier

Considering an ideal amplifier with infinite gain and infinite bandwidth, the transfer function between V_{out} and V_{in} is given by

$$G_{ideal}(j\omega) = \frac{-j\omega \cdot R_f C_1}{1 + j\omega \cdot R_f C_f} \,. \tag{4.1}$$

We identify a high-pass filter. Indeed, the gain value at $\omega = 0$ is zero. When the frequency exceeds the HP corner, the LNA gain is given by the ratio of the capacitances C_1/C_f. C_1 is a coupling capacitor that filters the DC component while the $R_f C_f$ couple determines the position of the HP corner. We have

$$A_{v,LNA} = 20\log\left(\frac{C_1}{C_f}\right) \qquad \text{and} \qquad \omega_{HP} = \frac{1}{R_f C_f}\,, \tag{4.2}$$

with $A_{v,LNA}$ expressed in dB and ω_{HP} expressed in rad/s.

Transfer function with a first-order amplifier

A more reasonable assumption is to consider a first-order amplifier for the LNA. Indeed, amplifiers have a finite gain and bandwidth in practice. A constant gain value cannot be maintained toward infinity due to the finite bandwidth of the amplifier. We understand that the topology proposed in Fig. 4.1 practically implements a band-pass filter. The transfer function of a first-order amplifier is given as

$$H(j\omega) = \frac{A_{v,0}}{1 + \frac{j\omega}{\omega_{p1}}}\,, \tag{4.3}$$

where $A_{v,0}$ represents the open-loop gain of the amplifier and ω_{p1} its dominant pole. Under the first-order response assumption, their product forms the gain-bandwidth (GBW) product which corresponds to the transition frequency ω_T where the gain is unitary (or 0 dB).

By taking into account the transfer function of the first-order amplifier, the transfer function of the LNA becomes

$$G_(j\omega) = \frac{-(j\omega)\cdot A_{v,0} R_f C_1}{(j\omega)^2\cdot(\frac{R_f C_1 + R_f C_f}{\omega_{p1}}) + (j\omega)\cdot(R_f C_1 + R_f C_f + \frac{1}{\omega_{p1}} + A_{v,0} R_f C_f) + (A_{v,0} + 1)}\,. \tag{4.4}$$

We can further simplify this equation considering that the closed-loop gain is sufficiently high, that is $C_1 \gg C_f$. We also note that the amplifier open-loop gain needs to be higher than the close-loop gain to ensure a proper working principle. This assumption implies $A_{v,0} \gg C_1/C_f \gg 1$. We can write Eq. 4.4 as follows

$$G(j\omega) \approx \frac{-(j\omega)\cdot R_f C_1}{(j\omega)^2\cdot(\frac{R_f C_1}{\omega_{p1} A_{v,0}}) + (j\omega)\cdot(R_f C_f) + 1}\,. \tag{4.5}$$

The Bode diagrams of $G_{ideal}(j\omega)$, $H(j\omega)$ and $G(j\omega)$ are illustrated in Fig. 4.2. These diagrams have been obtain with arbitrarily chosen value for the sake of working principle

illustration. From the Bode diagram of $G(j\omega)$, we state that the position of the LP corner is dictated by the intersection of the first-order amplifier response and the ideal high-pass filter response. The HP corner and LP corner for the band-pass LNA are

$$\omega_{HP} = \frac{1}{R_f C_f} \qquad \text{and} \qquad \omega_{LP} = \frac{A_{v,0} \cdot \omega_{p,1}}{C1/Cf} \,. \tag{4.6}$$

These frequencies should not overlap with the bandwidth of the microphone. For this reason, margins must be considered for the LNA frequency response, which means $f_{HP,LNA} < f_{HP,mic}$ and $f_{LP,LNA} > f_{LP,mic}$.

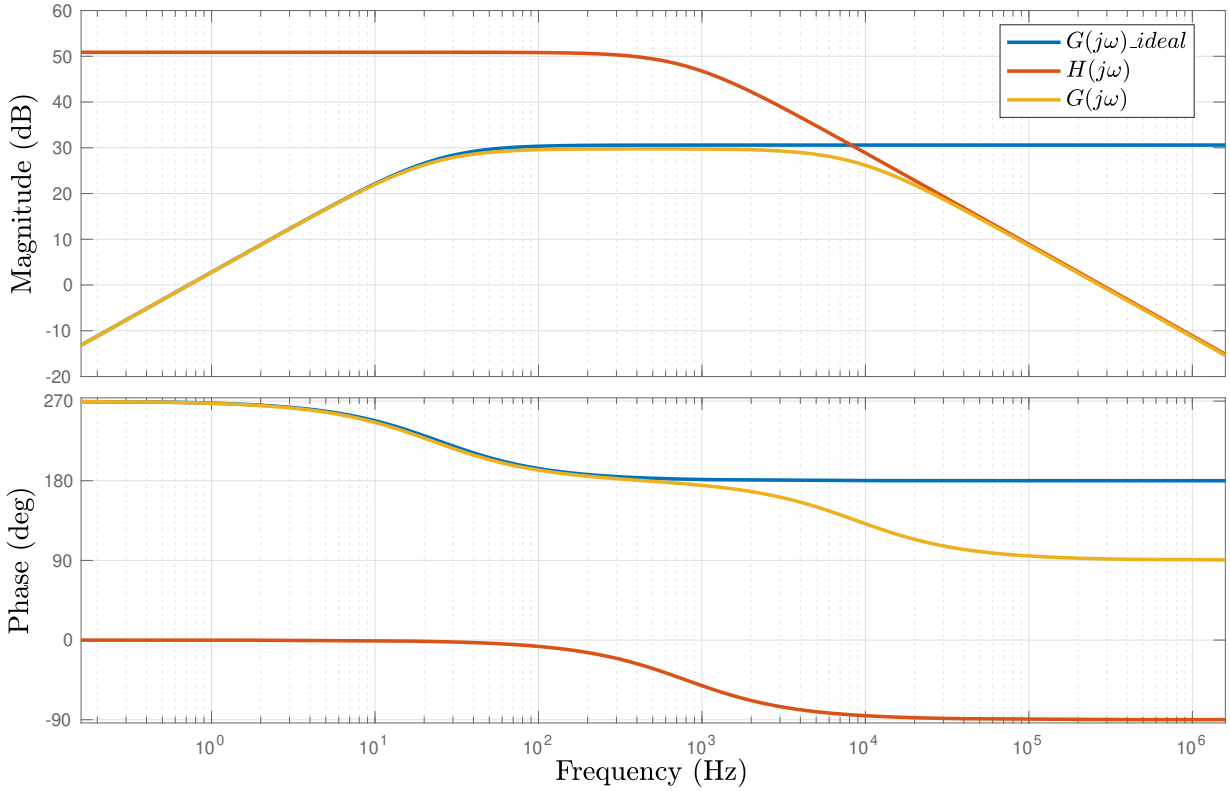


Figure 4.2: A Bode diagram illustrating the transfer function $G_{ideal}(j\omega)$, $H(j\omega)$ and $G(j\omega)$. We state that the position of the LP corner is given by the intersection of $H(j\omega)$ and $G_{ideal}(j\omega)$ given that $A_{v,0} > A_{v,LNA}$.

4.2 Expected performance for the LNA

The expected performance for the LNA are provided in this section and summarized in Table 4.1. We emphasize that these must be regarded as guidelines more than rigid requirements as the final performance of the amplifier (Chapter 5) and the resistive feedback (Chapter 6) cannot be foreseen.

Power consumption

The total power consumption of the AO chain should not exceed $1\mu W$. The power consumption of the LNA is typically dominated by the power consumption of the amplifier implemented as an operational transconductance amplifier (OTA). The allowable power consumption for the LNA should range in [400 nW, 600nW]. This assumption is supported by state-of-the-art papers presenting low-power OTAs for audio and biomedical applications [38, 39, 40, 41].

Input-referred noise

In Chapter 3, the minimum acoustic level of detection has been set to $L_{p,min} = 40\,dB_{SPL}$. This value determines the maximum input-referred noise (IRN) for the LNA, ensuring that electrical noise does not dominate at the input of this circuit. First, we need to convert $L_{p,min}$ in Pascal units. Thanks to Eq. 3.1, we have

$$p_{min} = p_0 \cdot 10^{(L_{p,min}/20)} = 2\,mPa\ . \tag{4.7}$$

Afterward, the sensitivity of the microphone has to be converted from dBV to V/Pa. Using Eq. 3.3 we can write

$$S_{V/Pa} = 10^{(S_{dBV}/20)} = 14,12\ mV/Pa\ . \tag{4.8}$$

By combining the results of Eq. 4.7 and Eq. 4.8, the maximum IRN is determined according to

$$IRN_{max} = 2 \cdot 10^{-3}\,[Pa]\ \cdot 14.12\,[mV/Pa]\ = 28.25\,\mu V_{rms}\ . \tag{4.9}$$

LNA gain

Given the power consumption constraint, the search in state-of-the-art VAD systems papers indicates a typical gain value of 30 dB for the LNA. On the one hand, lower values yield insufficient signal energy at the output of the LNA, making the decision task difficult for the comparator when a relevant sound is sensed. On the other hand, higher gain values mean a higher GBW product and thus higher power consumption. Indeed, the GBW product scales with power consumption, as it will be demonstrated in Section 5.7.

Bandwidth

As developed in the previous section, the HP corner and LP corner of the LNA should not overlap with the bandwidth of the microphone. As a result, margins must be considered to prevent HP and LP corner variation. Considering the expressions in Eq. 4.6 the variation of the HP corner could come from R_f variation as it is implemented using a pseudo-resistor. The variation of the LP corner mainly depends on GBW product variation. These potential issues will be addressed in the next two chapters. As the microphone bandwidth ranges from 90 Hz to 16 kHz, the LNA bandwidth must aim at a higher bandwidth.

Performance	Values
Power consumption	[400, 600] nW
IRN	$< 28.25\,\mu V_{rms}$
Gain	30 dB
Bandwidth	$f_{HP,LNA} < 90\,Hz$ and $f_{LP,LNA} > 16\,kHz$

Table 4.1: Expected performance for the LNA

4.3 Choice for the capacitor and resistor values

While the GBW product of the OTA set the LP corner of the LNA, the values for C_1, C_f and R_f can already be determined given the gain and HP corner specifications for this circuit listed in Table 4.1.

As the ratio between C_1 and C_f determines the LNA gain of 30 dB, we have $C_1 \approx 32 \cdot C_f$. Considering a typical on-chip capacitor value for C_f (hundreds of fF), the capacitance C_1 must go up to the pF order of magnitude. An off-chip capacitor directly interfacing the microphone is considered to cope with eventual area overhead associated with this value.

Still considering a typical on-chip value for C_f, the resistance value of R_f goes up to the $G\Omega$ order of magnitude. Typical on-chip polysilicon resistor density prevents implementing such a high resistance value. This issue will be addressed in Chapter 6. By setting the HP corner to 25 Hz in order to respect the margin considerations, the resistor and capacitor values are given by : $C_1 = 11\,pF$, $C_f = 325\,fF$, and $R_f = 20\,G\Omega$[1]. Considering a Metal-Insulator-Metal (MIM) capacitor with a density of $2\,fF/\mu m^2$ for the feedback capacitor, C_f occupies an on-chip area of 162.5 μm^2.

As C_1 is an off-chip capacitor, we can search for a suitable model on distinct manufacturers websites. The selected model is the a surface mount (SMD) multilayer ceramic capacitor from *MuRata* (Series: GJM, reference: GJM1555C1H110GB01D) [42]. As expected, the capacitance is 11 pF. This model was chosen as the temperature tolerance ranges from -55°C to 125°C while ensuring a ±2% tolerance value. The maximum voltage for the capacitor is 50 V which is much higher than any voltage source in this application. We should note that the soldering process must be carefully realized as it could damage the capacitor and impacts its overall performance.

[1]It is important to stress that this combination of values is not unique. Other combinations could yield the desired HP corner.

Chapter 5

OTA design and implementation

We should pay particular attention to the OTA design as this block defines most of the LNA performance, such as the power consumption, input noise and bandwidth. This chapter thus begins with a summary of the main figures of merit for an OTA in Section 5.1. The choice of a suitable topology and the study of its working principle are detailed in Sections 5.2 and 5.3.

The design process is organized into two main parts. First, the g_m/I_D sizing methodology allows generating a functional yet not optimized design. Section 5.4 explains the main principle of the g_m/I_D methodology and proposes a design flow based on the analytical expressions of the chosen OTA. In Section 5.5, this design flow is implemented using a Matlab template to have an immediate insight of the OTA main performance. These performance are next compared for the same sizing in Section 5.6 with Spice simulations using Eldo. This initial step in the design is useful to understand performance trade-offs linked with the chosen topology. To that end, we seek a proper matching between Matlab and Eldo simulations.

Second, the OTA is optimized by a genetic algorithm. In Section 5.7, we analyze the theory of genetic algorithms and explain how these apply in the design of analog circuits. To comprehensively complete the optimization, it is split up into two steps, namely preselection and fine-tuning. This typically alleviates constraints associated with random initialization.

Finally, Section 5.8 validates the final sizing through PVT corners analysis. At the end of this chapter, we also present a layout implementation of the OTA in Section 5.9 and a complete review of its main performance in Section 5.10.

5.1 Main figures of merit

Open-loop DC gain

The open-loop DC gain represents the amplification factor between input and output voltages. If V_{in} denotes the voltage difference between positive and negative input terminals of the OTA, we write

$$A_{v,0} = 20 \log \left(\frac{V_{out}}{V_{in}} \right) \Bigg|_{\omega=0} \qquad [\text{dB}] \,. \tag{5.1}$$

As in this work the LNA operates in closed-loop, it is essential to have $A_{v,0}$ greater than $A_{v,LNA} = 30\,dB$ to avoid erroneous behavior and ensure sufficient bandwidth.

Gain-bandwidth product

Considering a first-order OTA frequency response, the gain-bandwidth product (GBW) product is given by

$$f_T = f_{p,1} \cdot A_{v,0} \qquad [\text{Hz}] \,, \tag{5.2}$$

where $f_{p,1}$ stands for the dominant pole. Also referred to as the transition frequency in the literature, the GBW product defines the amount of gain that can be targeted for a given bandwidth requirement in closed-loop. In addition, considering a real OTA response, the relative position between the transition frequency and the non-dominant pole determines the available phase margin.

As the LNA target $A_{v,LNA} = 30dB$ and $f_{LP,LNA} > 16\,kHz$, the GBW product should be at least $GBW > 10^{\frac{30}{20}} \cdot 16000 \approx 506\,kHz$. To ensure a sufficient margin for the LP corner, the GBW product requirement is set to 550 kHz in order to avoid overlapping with the microphone frequency response.

Power consumption

In the context of this work, this metric is of the utmost importance. Power consumption should be minimized while carefully evaluating performance trade-offs. Practically, the power consumption of an OTA in Watts is computed as the product between the supply voltage and the total DC current as

$$P = V_{DD} \cdot I_{DD} \qquad [\text{W}] \,. \tag{5.3}$$

Stability

In a closed-loop configuration, stability is central to avoid positive feedback issues. The phase margin ϕ_M is the amount of change in open-loop phase needed to induce an unstable response in closed-loop [43]. Stability in closed-loop can be evaluated thanks to the open-loop frequency response of the OTA. The phase margin indeed corresponds to

$$\phi_M = \phi\big|_{f=f_T} + 180^\circ \qquad [^\circ] \,. \tag{5.4}$$

Noise performance

The electrical noise is a randomly time-fluctuating electrical signal that exhibits a zero mean, a given amplitude, and a power spectral density (PSD) S. Performing noise analysis, each transistor acts as a noise source. As relatively low frequencies are considered in this work, the dominating noise source is the flicker noise, whose PSD is inversely proportional to frequency. The thermal noise also contributes to the overall noise but with a less significant impact. The PSD of this noise exhibits a constant amplitude across frequency. The output voltage noise in RMS is computed according to

$$\sigma_{v_{OUT}} = \sqrt{\int_{f_{min}}^{f_{max}} S_{v_{OUT}}(f)\, df} \qquad [\mathrm{V}]\,, \tag{5.5}$$

with $S_{v_{OUT}}$ being the total output voltage noise PSD expressed in V^2Hz^{-1} and f_{min} (resp. f_{max}) being the minimum (resp. maximum) frequency considered for the noise analysis, here the LNA bandwidth. The IRN can be computed in a similar fashion using $S_{v_{IN}}(f)$. The metric that bridges the gap between input and output noise is the gain value. Dividing the output voltage noise by the gain yields the IRN. Eldo simulations have supported this statement. The IRN is a metric that typically needs to be minimized to improve the minimum acoustic level of detection.

Slew rate

The slew rate (SR) is essentially a large signal performance defined as the maximum rate of output voltage change per unit of time (often in microseconds). In other words, it is essential to ensure that significant swing variations at the input do no impact the transient performance at the output. The SR is computed by applying a large step signal at the OTA input and then measuring the rate of change at the output from 10% to 90%. Mathematically, we write

$$SR = \frac{\Delta V_{OUT}}{\Delta t} = \frac{V_{OUT,90\%} - V_{OUT,10\%}}{t_{90\%} - t_{10\%}} \qquad [\mathrm{V}/\mu\mathrm{s}]\,. \tag{5.6}$$

Common mode rejection ratio

The common mode rejection ratio (CMRR) defines the ability of an amplifier to reject the common-mode voltage on both inputs. It is defined as follows

$$CMRR = 20\log\left(\left|\frac{A_d}{A_{cm}}\right|\right) \qquad [\mathrm{dB}]\,, \tag{5.7}$$

where $A_d = V_{out}\,/\,(V_{in,+} - V_{in,-})$ represents the differential gain and $A_{cm} = V_{out}\,/\,\frac{1}{2}(V_{in,+} + V_{in,-})$ the common-mode gain.

Input offset

The input offset mostly results from the mismatch of the differential pair. This mismatch is associated with the statistical variability of the transistor parameters. For this reason, the input offset is seen as a random variable whose distribution is studied thanks to Monte-Carlo simulations. The provided offset in papers often refers to the 3σ offset covering 99.7 % of the possible values.

Statistical variability from one component to another is inevitable as the process causes time-independent random variations in physical quantities of identically manufactured devices [44]. This phenomenon is caused, for example, by the granularity of the oxide material involving oxide thickness fluctuation, the granularity of the gate material causing line edge roughness (LER) and discreteness of the dopant atoms resulting in random dopant fluctuations (RDF) [45]. Transistor parameters can therefore be considered as realizations of random variables.

This gets even worse with technology scaling as the number of dopant atoms reduces in the channel. According to Pelgrom's law, we have

$$V_{th} \sim \mathcal{N}(V_{th,0},\, \sigma_{V_{th}}) \;, \tag{5.8}$$

with $\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{W \cdot L}}$ meaning that the threshold voltage is proportional to the inverse square root of the channel area. Nevertheless, $A_{V_{th}}$ tends to improved with technology scaling but not as quickly as $\sqrt{WL}$ [46].

5.2 Selection of the OTA topology

Choosing a topology is a critical step in the overall OTA design. This task is a prerequisite for achieving adequate performance for the AO chain as the OTA performance determines most of the performance of the LNA interfacing the microphone. However, it is still challenging to choose or even reuse a given topology since the analog sizing process is specific to its target application and depends on the technology. Nothing guarantees that a topology suited for an application will be adequate for another.

An automatic, generic method for topology selection of analog circuits has been proposed in [47] based on a decision tree in which each node represents an OTA architecture. This paper aims to implement an efficient analog reuse method to reduce analog design time and avoid knowledge-based topology selection. To remain as general as possible, the paper is restricted to a specific number of architectures, focusing on the automotive field. A generic method resulting in predesigned circuits is helpful to speed up the process evaluation design, and the associated topologies are generally more robust. Nonetheless, in a context constrained by power consumption, such a methodology exhibits limitations since the paper constrains the bias source of the distinct OTAs to a same value and does not mention the technology it uses. However, the approach developed in this paper is still relevant and gives an orientation for the architecture choice of the OTA.

The LNA expected performance and main FoMs for an OTA oriented the search towards topologies featuring low-voltage, low-power, low-noise performance while meeting bandwidth requirements. Additional investigation in state-of-the-art papers highlighted the need for a two-stage OTA to ensure sufficient open-loop gain, especially using 65nm LP CMOS as the intrinsic gain $\left(\frac{g_m}{g_d}\right)$ is rather small in this technology [48]. This search yielded architectures initially designed for biomedical front-end [38, 39, 40, 41]. This fact is not irrelevant as this field is close to audio sensing, except that bandwidth requirements are lower than audio sensing. Among these papers, it was also preferable that symbolic equations be available to facilitate the g_m/I_d sizing methodology. Among topologies of interest, the paper [40] proposes an improved Miller (IM) OTA, presented in Fig. 5.1, that yields promising results. In this paper, the OTA power consumption is 550 nW and the DC open-loop gain is 73 dB for a 0.35 μm CMOS process. The GBW product is rather small (13 kHz) due to the employed sizing relying on large transistor dimensions. This paper also has the advantage of presenting detailed equations that describe its working principle.

5.3 Operation of the selected topology

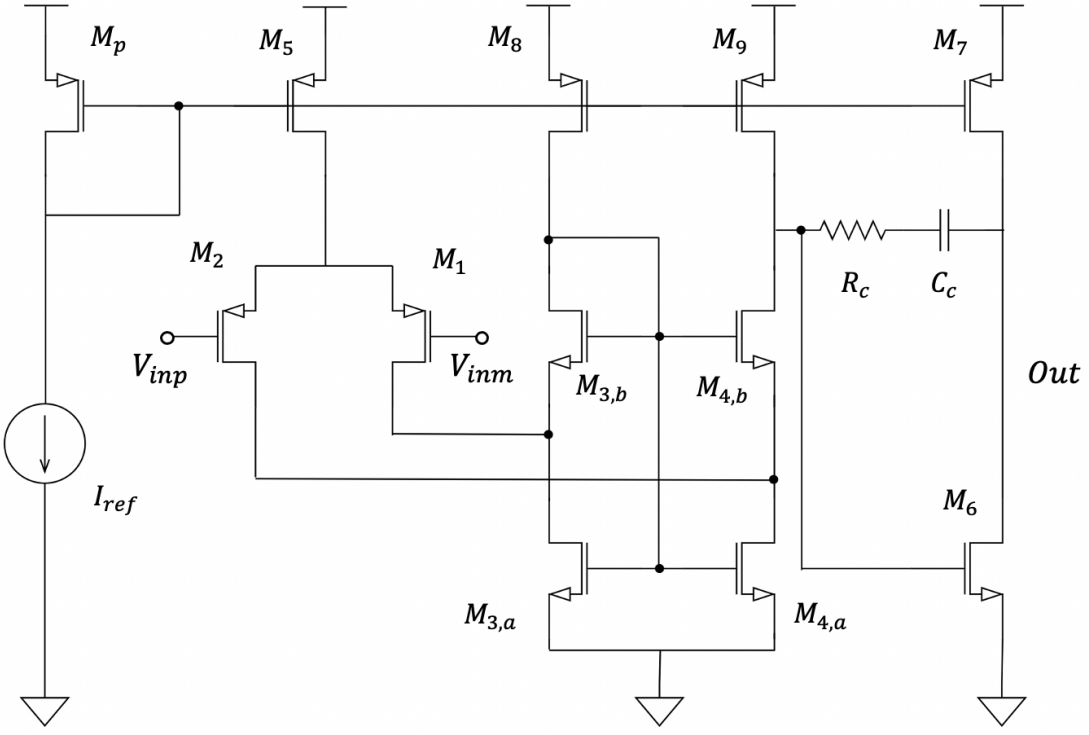


Figure 5.1: Improved Miller OTA - Topology

Working principle

In Fig. 5.1, we can highlight major components of the IM OTA.

1. **The input differential pair** is made of transistors $M_{1,2}$, where the gate of M_2 corresponds to the positive input terminal as an increase in V_{inp} tends to decrease $V_{GS,6}$ implying that more current can flow into the load capacitor C_L, not represented in Fig. 5.1, and increasing the output voltage. We note that a change has been made here with respect to the original paper as this latter features a bulk-driven differential pair for input signal swing considerations. As a design choice, this solution was not retained because the transconductance g_{mb} is typically lower than g_m. Hence a gate-driven differential pair offers more GBW product for the OTA.

2. **The PMOS biasing current mirrors network** is formed of M_5, $M_{8,9}$ and M_7. Each of these transistors replicates the current I_{ref} according to a factor that depends on the transistors aspect ratios with respect to $\frac{W_P}{L_P}$, as these must be matched and present the same g_m/I_D value. To remain consistent with the paper implementation, the current $I_{D,5}$ that biases the differential pair is kept the same as I_{ref}, while currents $I_{D,8,9} = \frac{1}{2} \cdot I_{ref}$ and $I_{D,7} = 5 \cdot I_{ref}$.

3. **A Composite transistor** is formed by $M_{3a,4a}$ and $M_{3b,4b}$. It features a constant $V_{DS,3a,4a}$. Hence, $V_{DS,1}$ and $V_{DS,2}$ should be identical and constant which improves the matching of the differential pair and yields better offset performance. The initial purpose of the composite transistor is to implement a level shifter. The idea comes from the fact that if the common-mode voltage is close to ground in a classical Miller OTA, the differential pair distorts the signal since its active load starts switching off [40]. To cope with the issue, batteries should theoretically be placed in series with the active load. To emulate the theoretical behavior of batteries (a voltage drop), these have been replaced by common-gate transistors, here $M_{3b,4b}$. A mathematical expression for $V_{DS,3a,4a}$ is provided in a further subsection.

4. **The Output stage** is a class-A stage. This stage is realized thanks to $M_{6,7}$.

5. **Frequency compensation** is achieved by the negative RC feedback that connects the output node to the drain of $M_{4,b}$ and M_9 featuring Miller compensation and ensuring better stability. The series (or nulling) resistor R_c is particularly useful to cancel the impact of the zero on the OTA frequency response.

Small-signal analysis

The gate voltage of transistors $M_{3a,4a}$ and $M_{3b,4b}$ acts as an AC ground [40]. Consequently, the AC small-signal model of the OTA represented in Fig. 5.2 describes the elements on the nodes along the signal path. The notations used in this figure are the following: $g_{m,i}$ and $g_{mb,i}$ are respectively the gate-to-source and bulk-to-source transconductance associated with the transistor M_i. Besides, $r_i = g_{d,i}^{-1}$ represents the output resistance associated with the transistor M_i. Finally, $C_{n,i}$ is the parasitic capacitance associated with voltage node v_i.

We also use the following assumptions to draw Fig. 5.2

$$g_{m,i} \geqslant g_{d,i}\,, \qquad C_L \geqslant C_{n,out}\,, \qquad g_{mb,i} \approx \frac{g_{m,i}}{4}\,, \qquad f_{p1,\,p2,\,z1} \ll f_{p,z,other} \Rightarrow neglected\,,$$

where f_{p1} is dominant pole, f_{p2} the non-dominant pole and f_{z1} the position of the zero. The third assumption relies on the fact that $g_{mb,i}$ varies from 20% to 30 % of $g_{m,i}$ [49].

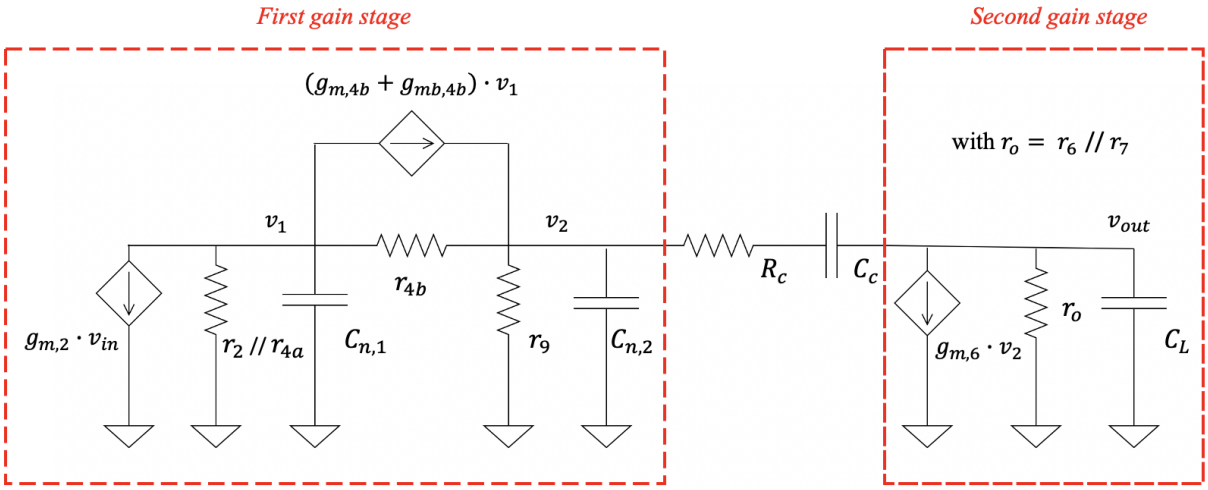


Figure 5.2: AC small-signal model of the improved Miller OTA

From Fig. 5.2, it is possible to derive the transfer function of the IM OTA. We can simplify the previous figure by gathering parallel and series components together to obtain the following equation system

$$\begin{cases} g_1 = g_{d,2} + g_{d,4a} + g_{C_{n,1}} \\ g_2 = g_{d,9} + g_{C_{n,2}} \\ g_L = g_{d,6} + g_{d,7} + g_{C_L} \\ g_4 = g_{m,4b} + g_{mb,4b} \\ g_c = \frac{1}{Z_c} \end{cases} \tag{5.9}$$

with $Z_c = R_c + 1/s{\cdot}C_c$ and $g_{C_x} = s{\cdot}C_x$. The mathematical development of the IM OTA transfer function based on Kirchhoff current law (KCL) is presented in Appendix A Section A.1. The transfer function is obtained as

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m,1} \cdot (g_{d,4b} + g_4)}{\left[(g_2 + g_c + g_{d,4b}) \cdot (g_1 + g_4 + g_{d,4b}) - g_{d,4b} \cdot (g_{d,4b} + g_4)\right] \cdot \frac{(g_L + g_c)}{(g_c - g_{m,6})} - g_c \cdot (g_1 + g_4 + g_{d,4b})}\,. \tag{5.10}$$

This cumbersome formula was used to analyze the matching between Matlab and Eldo simulations.

The expressions for the poles and the zero are found according to the AC small-signal analysis

$$f_{p1} = \frac{g_{m,1}}{2\pi \cdot A_{v,0} \cdot C_c}, \qquad f_{p2} = \frac{g_{m,6}}{2\pi \cdot C_L}, \qquad f_z = \frac{1}{2\pi \cdot C_c \left(R_C - \frac{1}{g_{m,6}}\right)}. \tag{5.11}$$

We notice that the locations of the non-dominant pole and the zero are similar to those of a classical Miller topology with an RC negative feedback. Furthermore, the value of the resistor provides flexibility in positioning the zero in the OTA frequency response. To derive the expression of the open-loop gain $A_{v,0}$, the capacitors in Fig. 5.2 form open circuits yielding

$$A_{v,0} = \frac{g_{m,1} \cdot g_{m,6}}{g_{d,67} \cdot \left[\frac{(g_{d,9}+g_{d,4b})}{g_{d,4b}+g_{m,4b}+g_{mb,4b}} \cdot g_{d,24} + g_{d,9}\right]} \approx \left(\frac{g_{m,1} \cdot g_{m,6}}{g_{d,9} \cdot g_{d,67}}\right), \tag{5.12}$$

given that $g_m \gg g_d$.

Composite transistor architecture

A composite transistor is essentially composed of two transistors, respectively M_a and M_b. The source of M_b is connected to the drain of M_a and both gates are connected together. We write G, D, S the gate, drain and source of the composite transistor [50]. From Fig. 5.3 we immediately state that

$$I_{DS,a} = I_{DS,b} \tag{5.13}$$

and

$$V_{DS,a} = V_{GS,a} - V_{GS,b}. \tag{5.14}$$

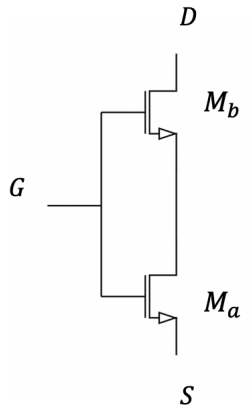


Figure 5.3: Composite transistor

When the drain-to-source voltages of M_b and M_a are greater than $V_{dsat} \approx 100mV$ at ambient temperature, the drain-to-source voltage of M_a can be rewritten as

$$V_{DS,a} \approx nU_T \cdot \log\left(\frac{W_b/L_b}{W_a/L_a}\right), \tag{5.15}$$

with log the natural logarithm. A mathematical development is provided in Appendix A, Section A.2. As a result of Eq. 5.15, the drain-to-source voltage of M_a is kept constant by cascode effect regardless of the access voltage applied to the composite transistor. This voltage only depends on transistors sizes which is helpful to form the level shifter mentioned in Section 5.3. It is important to retain that Eq. 5.15 is valid only for transistors operating in weak inversion.

Systematic offset avoidance

Attention must be paid to the DC bias between the stages to avoid any systematic offset at the output of the differential amplifier [40]. From the expression of the current as a function of the transistor dimensions in weak inversion, we find an expression that links the aspect ratios of transistors in order to avoid any systematic offset.

Indeed, at DC point we know that $I_6 = I_7$ and that $\frac{I_5}{2} + I_9 = I_{4,a}$, yielding

$$\frac{I_7}{I_{4,a}} = \frac{I_6}{I_{4,a}} = \frac{I_7}{\frac{I_5}{2} + I_9} \, . \tag{5.16}$$

Systematic offset can therefore be avoided given that

$$\frac{(W/L)_6}{(W/L)_{4,a}} = 2 \cdot \frac{(W/L)_7}{(W/L)_5 + 2 \cdot (W/L)_9} \, . \tag{5.17}$$

5.4 g_m/I_D sizing methodology

Conventional methodology

Unlike digital circuit design, analog circuit design is made difficult by the many degrees of freedom available to the designer. This design technique, relying on the transconductance-to-drain current ratio of MOS transistors (g_m/I_D), proposes a systematic approach to address the complexity of analog circuit design. It also helps to size transistors so that designers can choose the level of inversion for the transistors [51].

The initial step often identifies the relationships between available parameters and circuit specifications throughout a precise behavioral analysis of the topology, done at a symbolic level. Small-signal and large-signal analyses of the chosen topology are therefore required. To describe the 65nm low-power CMOS transistors from TSMC, technological data are gathered in look-up tables (LUT) extracted thanks to the Eldo Spice simulator. A fundamental characteristic describing the transistor behavior is the g_m/I_D vs. normalized I_D curve. Considering a given drain current, it highlights a clear relation between transconductance g_m and the transistor aspect ratio (W/L). In a top-down approach, g_m/I_D values can be inferred by circuit specifications. By fixing a value for the length, it is thus possible to determine W [52].

It is also possible to adopt a bottom-up sizing approach. By setting admissible values of g_m/I_D, fixing the lengths and the drain currents, it is possible to determine the distinct widths of the transistors throughout the topology. It starts from the drain currents as an input parameters giving initial insight into the OTA power consumption at constant supply voltage, which is relevant for low-power design implementation.

Additional dependencies

The original g_m/I_D methodology, initially designed for micrometer-long transistor designs, does not address all dependencies that coexist between the transistor parameters for deeply scaled CMOS technologies [52]. Due to the employed technology, a sound design choice is to take into account g_m/I_D, L, I_D, and V_{DS} as input parameters to have a clear overview of the circuit performance estimation. The original methodology takes only the three first parameters into account.

Technological curves thus need to be extracted as successive sweeps in Eldo according to g_m/I_D, L and V_{DS} since I_D determined from the target power consumption. As another design choice, the length of each transistor has been set to a constant value of $1\,\mu m$ allowing to discard a degree of freedom and alleviate the short-channel effects that occur if minimum length sizing was adopted. With this in mind, technological data can be interpreted as a three-dimensional LUT. Figure 5.4 highlights the variation of transistor technological curve with respect to drain-to-source voltage.

As an example, for a constant value of normalized current I_N, the ratio g_m/I_D increases for an increasing voltage V_{DS}. Again for an increasing V_{DS}, we state that V_{GS} versus I_N is slightly shifted towards the right. As the fixed length is approximately one order of magnitude above the minimum length, the impact of V_{DS} is not significant and particularly in the weak inversion regime. However, this more extensive LUT for NMOS and PMOS transistors better match the Matlab and Eldo simulations, which is desirable.

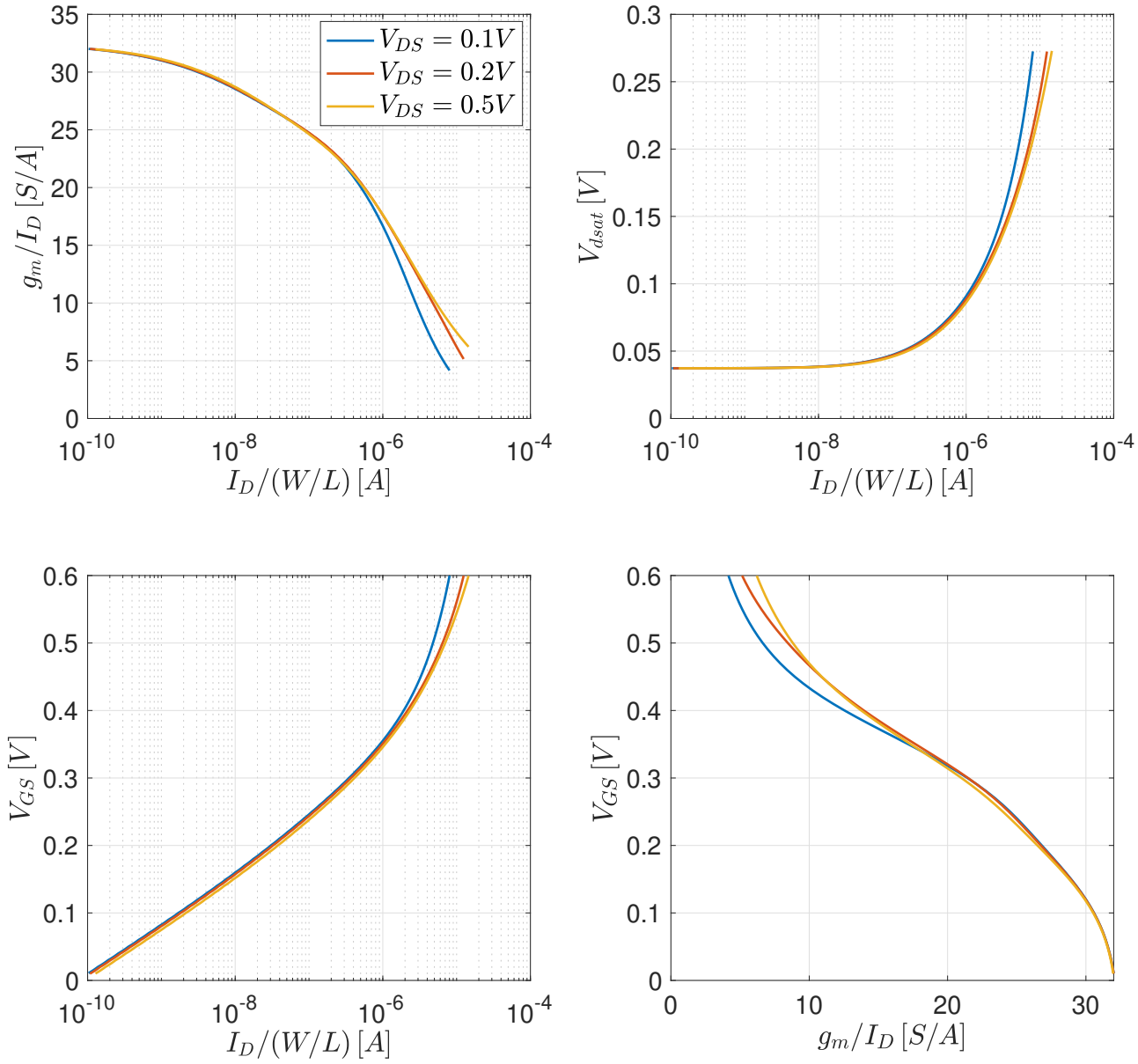


Figure 5.4: Technological data extracted at 25°C for a low-V_{th} NMOS core transistor - 65nm LP CMOS process

Design Flow

The diagram presented in Fig. 5.5 details the steps to find the sizing for all the transistors of the IM OTA. The reasoning has been carried out by setting a target a power consumption and deducing the biasing drain currents in each branch from the PMOS biasing current mirrors ratios. The values for V_{DS} and g_m/I_D have been set such that each transistor operates in saturation in weak inversion. Adding V_{DS} as an input parameter introduces a key degree of freedom in the design, which is definitively appropriate to ensure that transistors are operating in saturation.

The parameters whose values have been set to an suitable but arbitrary value are shown in red. The output parameters of the sizing methodology are depicted in green. The orange arrows refer to the use of the LUT. Voltages shown in blue are not directly fixed but rather obtained thanks to Kirchhoff voltage law (KVL). The arrows with text written on the right side refer to the use of one of the IM OTA symbolic equation.

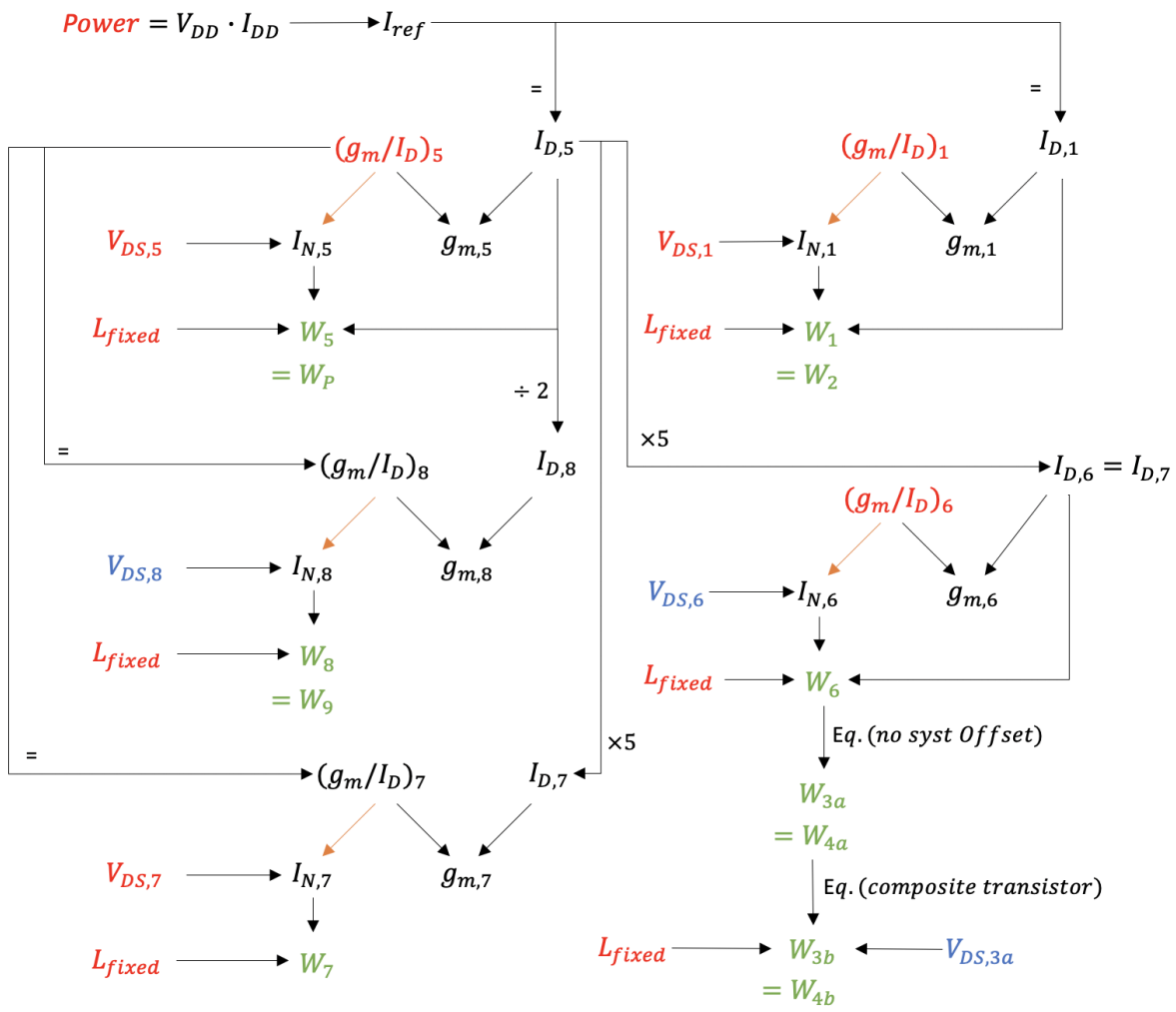


Figure 5.5: Design Flow - g_m/I_D sizing methodology using V_{DS} as additional input parameter

5.5 Matlab Simulations

A Matlab template has been implemented according to the design flow in Fig. 5.5. The values for the design inputs are discussed in the following subsection.

Design inputs

- $\mathbf{L = 1\mu m}$ **:** All transistors lengths have been set to a fixed value of L = $1\mu m$. The constant value simplifies the analysis for determining the width. A value in the order of magnitude of μm seems sufficient to prevent short-channel effects and exacerbated statistical variations due to local mismatch.

- $\mathbf{C_L = 100\,fF}$ **:** A typical value of on-chip capacitor has been chosen for the load capacitance value [53]. From the TLD architecture of the AO chain, we indeed observe that the OTA does not need to drive a high capacitance load.

- $\mathbf{C_C = 500\,fF}$

- $\mathbf{R_C = (1/g_{m,6})}$**:** This choice pushes the position of the zero theoretically at infinity to limit its impact on the frequency response.

- $\mathbf{I_{ref} = 125nA}$ **:** For the sake of comparison an initial power consumption of $600\,nW$ is targeted, as in the initial paper. Referring to the design flow and current flowing through each branch, this yields a reference current of $125\,nA$ given the supply voltage $V_{DD} = 0.6\,V$.

- $\mathbf{V_{DS,x} > 100mV}$ **:** The drain-to-source voltage of each transistor has been set so that each transistor within the topology is saturated.

- $\mathbf{(g_m/I_D)}$ **:** Referring to Eq. 5.11 the differential pair have been set to a higher transconductance-to-drain current ratio than the other transistors to target higher GBW product, that is $(g_m/I_D)_{1,2} = 30$. PMOS current mirrors have the same $(g_m/I_D) = 27$ values for matching purpose. This value is not unimportant and will be discussed in Section 5.6. Concerning M_6, a value of $(g_m/I_D)_6 = 27$ has been set. As seen in the design flow, this value cascades down to determine the sizing of transistors $M_{3a,4a}$ and $M_{3b,4b}$ through the symbolic equations of the IM OTA. This value thus mainly prevent $M_{3a,4a}$ and $M_{3b,4b}$ to exhibit wide dimensions.

Results and comments

The transistor sizes and performance obtained with the g_m/I_D sizing methodology are summarized respectively in Table 5.1 and 5.2. The Bode diagram obtained with Matlab is presented in Fig. 5.7. To extract this diagram, output resistances at each stage, as well as parasitic capacitances $C_{n,1}$ and $C_{n,2}$ have been evaluated thanks to the LUT and the design outputs. As a consequence of the low C_L value, the non-dominant pole is pushed far from the transition frequency yielding a phase margin of 85.7°. Thanks to the additional series resistance, the position of zero is theoretically pushed toward infinity.

Stage	Transistor	Aspect ratio ($\mu m/\mu m$)
Bias stage	$M_{P,5}$	5.2/1
First stage	$M_{1,2}$	14.5/1
	$M_{3a,4a}$	4.5/1
	$M_{3b,4b}$	33.7/1
	$M_{8,9}$	2.6/1
Second stage	M_6	22.4/1
	M_7	25.9/1

Table 5.1: Transistors sizes - g_m/I_D sizing methodology

Performance	Value
Open-loop gain	52.5 dB
GBW	475 kHz
Dominant pole	1.2 kHz
Non-dominant pole	4.97 MHz
Zero	$+\infty$
Phase Margin	85.7°

Table 5.2: Matlab performance - g_m/I_D sizing methodology

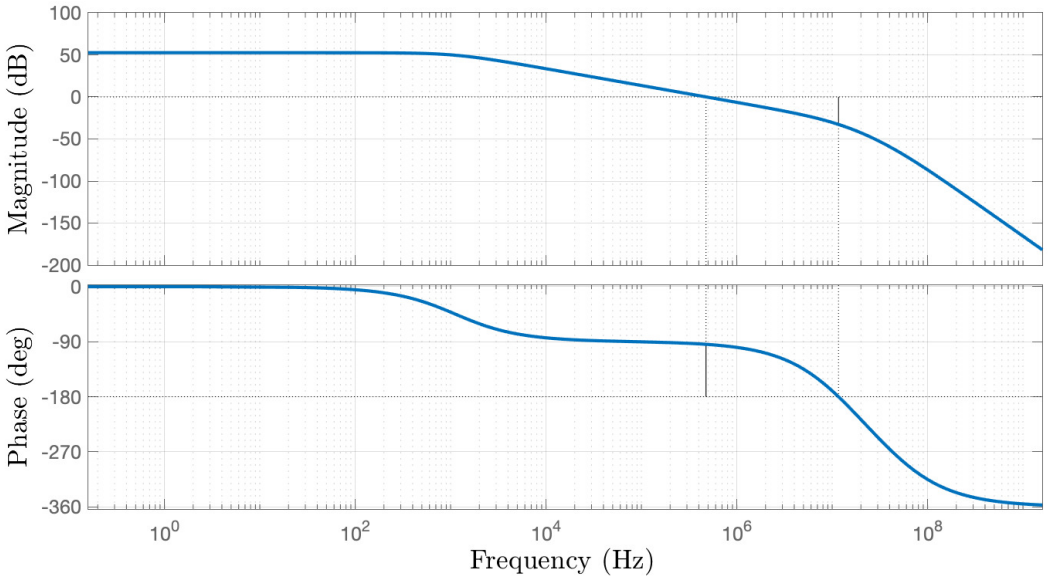


Figure 5.6: Bode diagram of the transfer function presented in Eq. 5.10. All the values of this equation have been obtained by the g_m/I_D sizing methodology.

5.6 Matlab vs. Eldo matching

Eldo testbench

From Matlab to Eldo, no fine-tuning on the widths and lengths values has been realized to achieve a strict comparative approach. The Eldo simulation results were obtained with the exactly same supply conditions as in the Matlab template, that is $V_{DD} = 0.6\,V$ and $I_{ref} = 125\,nA$.

Results and comments

The Bode diagrams from Matlab and Eldo simulations are presented in Fig. 5.7. A comparison of the main performance from Matlab and Eldo is proposed in Table 5.3. This comparison gives interesting conclusions.

First, we notice an overall accurate matching. The GBW product is sharply evaluated from Matlab and supports the mathematical validity of the hand-derived equation 5.10. We can nevertheless notice a slight discrepancy between the open-loop gains. From Eq. 5.11 this also translates in a scant gap in the positioning of the dominant poles f_{p1}. We hypothesize that the increase in gain is justified by the drain current mismatch between transistors M_P and M_5 in Eldo. Indeed the drain current biasing the differential pair $I_{D,5}$ is slightly lower than the reference one I_{ref} due to mismatch. As measurements showed a same $(g_m/I_D)_{1,2}$ between Matlab and Eldo, this implies an increase in $g_{m,1}$ for Eldo with respect to Matlab. This translates into more gain according to Eq. 5.12.

In addition, we see that the positioning of the non-dominant pole is closer to f_T in Eldo, implying a 6° phase margin loss. Though it does not represents a serious issue, the main assumption to justify this phenomenon relies on the parasitic capacitances evaluation in Matlab. An assumption from Section 5.5 states that $C_L > C_{n,out}$. Given $C_L = 100\,fF$ and the computed values for $C_{n,1}$ and $C_{n,2}$ (evaluated around tens of fF in Matlab), the parasitic output capacitance may not be that negligible. According to the non-dominant pole equation, this brings the position of this pole closer to the transition frequency which is detrimental to the phase margin. Moreover, the parasitic capacitance C_{gb} which is often dominating in weak inversion [54] has not been taken into account into the parasitic capacitances evaluation in Matlab.

Related to the comment on non-negligible output parasitic capacitance, since the ratio between M_7 and M_5 has been fixed to five, we prefer to avoid very large $(g_m/I_D)_5$. Indeed, if a high value is chosen, due to the exponential relationship between I_N and (g_m/I_D), a slight increase in $(g_m/I_D)_5$ induces an exponentially smaller $I_{N,5}$. Hence, for a constant drain current and a fixed length, this results in a very high W_5 value, multiplied by five to obtain W_7. At this point, the parasitic output capacitance is tremendous, the phase margin is killed, and a terrible matching between Matlab and Eldo is obtained. It has been the most difficult part of this section of the work and justifies the choice for $(g_m/I_D)_5 = 27$.

	Matlab	Eldo
V_{dd} [V]	0.6	0.6
I_{tot} [μA]	1	0.98
$Power$ [nW]	600	589
DC Gain [dB]	52.5	57
f_T [kHz]	475	464
PM [°]	85.6	79.6
GM [dB]	43.2	36.9

Table 5.3: Comparison between Matlab and Eldo results

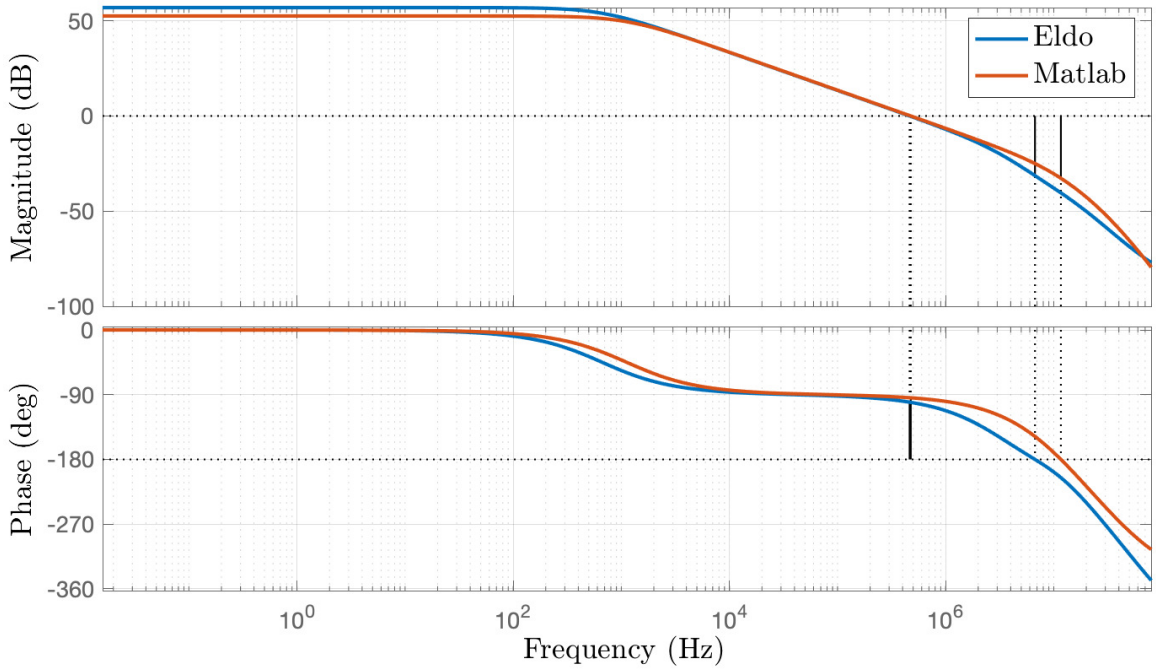


Figure 5.7: A Bode diagram illustrating the matching between Matlab and Eldo results. We state that the GBW product is accurately predicted by Matlab.

Review on the g_m/I_D sizing methodology

The point of the g_m/I_D sizing was to develop a proper understanding of the topology and yielding a functional OTA. However, the GBW product remains lower than the target 550 kHz value at this design stage, pointing out the need for further optimization. Moreover, the IRN has been measured to 38.9 μV_{rms}. Brought back into the acoustic domain, this value corresponds to 43 dB_{SPL}, which is higher than the requirement for the minimum acoustic level of detection.

5.7 Genetic algorithm

This section develops the two-step optimization implemented using a genetic algorithm.

Working principle

Genetic algorithms (GA) are part of a larger class of algorithms, called evolutionary algorithms. GAs mimic Darwin's theory of evolution by emulating natural selection to find solutions to complex problems. The selection of individuals, called items, occurs based on their ability to fit constraints and optimize objectives [55].

Within a population, each item is composed of a specific genome to which a score is attributed. From one generation to another, the genomes of old items are altered. A fitness function is then applied to attribute a score to each new item. Afterward, a selection is operated among the new items whose performance respect the constraints and fit the problem objectives. This hopefully yields an improved version from the old generation to the new one.

The algorithm may initialize with a random population whose constitutive parameters of the genome are randomly selected within acceptable ranges or with a population that already meets some of the constraints. The algorithm stops whenever a suitable solution is found or after a given number of generations, determined by the programmer.

Mechanisms of genome alteration

There are four types of mechanisms used to alter the genome of an item.

1. **Random selection :** The new genome is generated randomly within a defined range of values. Randomly settled items are less likely to outperform items resulting from generation-long optimization.

2. **Elitism :** Since there is a certain guarantee that the old generation respects the established constraints, it is possible to pass on some of the best items of the old generation directly to the next generation.

3. **Cross-over :** The genome of the new item is generated based on parent genomes. The genome of the new item contains a percentage $a\%$ of the genome of parent A and another percentage $(100 - a\%)$ from parent B. The designer defines the proportion of the genome from parent A to parent B during algorithm setup.

4. **Mutation :** This mechanism involves selecting an item from the old generation and modifying a specified percentage of its genome. Since only a small part of the genome is modified, we can expect a score that does not vary drastically from the old item and is hopefully better. As a rule of thumb, mutations occur to maintain diversity and prevent premature convergence [56].

Application of the genetic algorithm to the OTA design

OTA design optimization is a complex task as performance evaluation usually relies on multiple metrics [57]. One talks of a multi-objective optimization problem when several metrics are defined as objectives. Hence, a multi-objective GA has been used in this work to optimize the reference IM OTA obtained with the g_m/I_D sizing methodology.

Referring to the Fig. 5.8, the performance objective can be interpreted as a function $f_i(\boldsymbol{x})$ of the design parameters $\boldsymbol{x} = (x_1, ..., x_n) \in D$. The ensemble D is the set of design parameters and contains all the circuit configurations. As far as the improved Miller OTA is concerned, the dimensions of the transistors have been chosen as input parameters. We have $D = (W_1, L_1, ..., W_N, L_N)$. If the topology had been more complex, it would have been wise to choose higher-level parameters. The ensemble of design parameters directly maps to the ensemble of achievable performance F through the f_i function. To take circuit requirements into account in addition to performance objectives, the designer may also define constraints on the set of achievable performance. These constraints are here denoted as $c_j(\boldsymbol{x}) \lessgtr C_j$. The greater (resp. smaller) symbol is used when a higher (resp. smaller) value is targeted for the constraint.

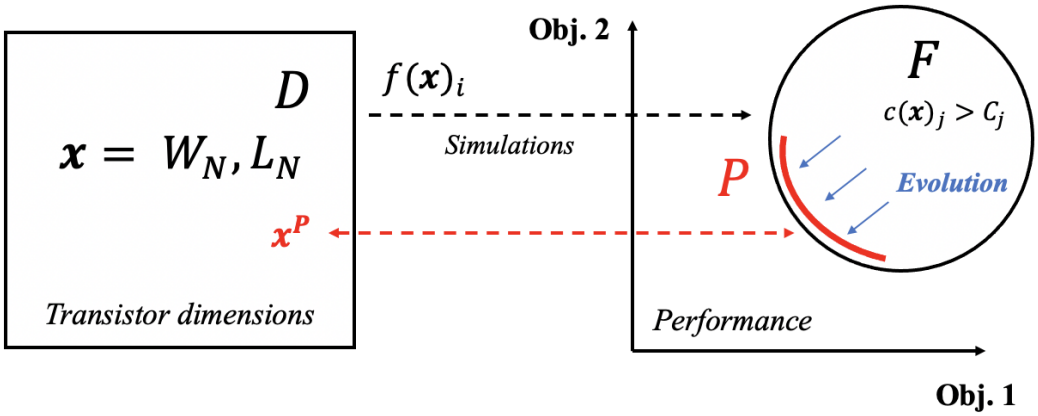


Figure 5.8: Genetic algorithm applied in OTA design for a two-objectives optimization.

The multi-objective GA aims to determine a subset $P \in D$ such that P optimizes the objective performance. Regarding the multi-optimization problem, no single solution exists that simultaneously improves each objective at the time. Objective functions are somewhat conflicting, yielding a front of the Pareto of optimal solutions. The so-called Pareto front is reached whenever the evolution can improve none of the objective functions without being detrimental to the other objective. When P is attained after N generation, the design can find a subset of ideal design parameters x^P corresponding to the Pareto front employing an inverse mapping from F to D.

Optimization process

It is of utmost importance to have a clear idea of the optimization process before carrying on any simulations. On the one hand, the key requirement associated with the IM OTA is definitively the input noise. Indeed a low IRN results in a lower minimum acoustic level of detection. On the other hand, as ultra-low power is also essential, a noise-power trade-off seems the most appropriate for the design. However, one main limitation associated with GAs is the startup time resulting from random initialization. For the IM OTA, the GBW product constraint turns to be severe for the noise vs. power optimization. This initialization deadlock makes sense as the GBW product reached by g_m/I_d sizing (464 kHz) is lower than the target constraint value (550 kHz). To overcome this problem, the adopted solution is to run the template initially according to a GBW product vs. power optimization, by considering the noise as a constraint. This first optimization can be seen as a preselection step. Afterward, it is possible to feed forward the N items of the Pareto front respecting the GBW product constraint as the initial population of the noise vs. power optimization, called fine-tuning. Key parameters have been added between the first and the second optimization process to avoid the two optimizations to go against each other. An illustration of the OTA design including the full optimization process is provided in Fig. 5.9.

The PSD study of an OTA coming out of the Pareto front from the preselection step showed that the flicker noise is dominant up to 1 kHz. To reduce the flicker noise, we rely on increasing areas of the transistors that mainly contribute to it. Mathematical models describing the flicker noise are for instance the mobility fluctuation model and the number fluctuation model, developed in [58]. Both agree that an increase in the transistor area reduces the flicker noise. As a design choice, the lengths of the transistors $M_{3a,4a}$ and $M_{8,9}$ have been added between preselection and fine-tuning as these transistors are the ones that contribute the most to flicker noise. The lengths of $M_{1,2}$ have also been added as the differential pair is a critical element in an OTA. If the differential pair is large and thus well-matched, this reduces the input offset and the IRN because the first stage of the OTA has a larger gain. The dimensions obtained at the end of the preselection and fine-tuning steps are presented in Appendix B for the sake of conciseness.

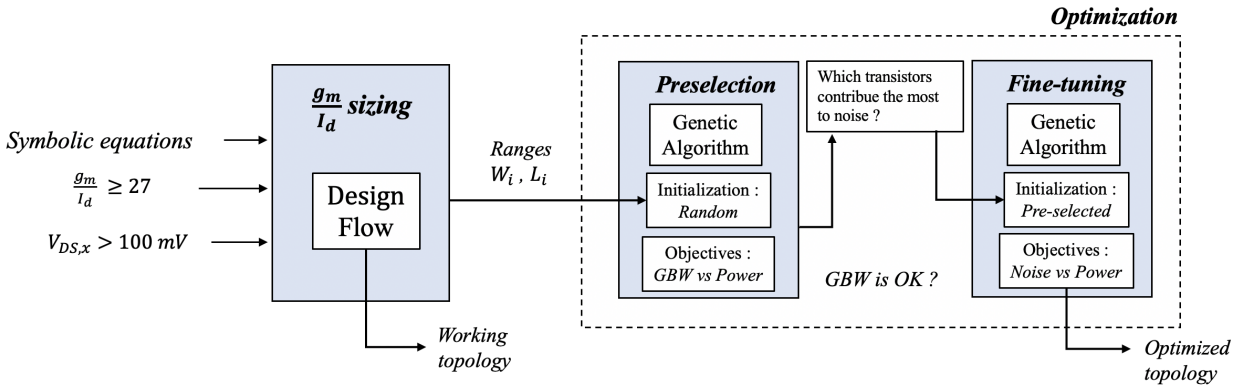


Figure 5.9: Complete design process with the two-step optimization

Preselection

The preselection initializes randomly from parameter ranges set around the g_m/I_D sizing results. The algorithm uses nine input parameters. These parameters are listed in Table 5.4. As a design choice, the ratios between PMOS current mirrors are the same as in the g_m/I_D sizing. Hence, $W_{7,8,9}$ are found from W_5. The links between the OTA parameters, illustrated by the symbolic equations of the IM OTA in Section 5.3, have not been included in this optimization. The interest is to understand how the algorithm will evolve and find an ideal solution by itself. [1]

Parameter	**Range**
Length of all transistors, L	[1, 3] μm
Width of differential pair, W_1	[3, 40] μm
Width of PMOS current mirror, W_5	[3, 25] μm
Width of composite transistor (down), $W_{3a,4a}$	[3, 15] μm
Width of composite transistor (up), $W_{3b,4b}$	[10, 50] μm
Width of output branch transistor, W_6	[10, 50] μm
Value of feedback Miller capacitor, C_c	[0.3, 1] pF
Value of feedback Miller resistor, R_c	[55, 60] $k\Omega$
Reference current, I_{ref}	[70, 150] nA

Table 5.4: Parameter ranges - Preselection

Simulations have typically shown that lighter constraints ease the initialization throughout the design space while rigid constraints induce a serious clustering effect resulting in stiff optimization that appears as clusters of points moving along together. In that case, the number of generations required to obtain the Pareto front is typically two times higher.

The constraints for the preselection are provided in Table 5.5. The preselection results are shown in Fig. 5.10. An attentive reader may observe that a slight clustering effect occurs around the 7-th generation. However, this phenomenon fades away quite quickly. After the 15-th generation, we already see a front emerging. It still evolves until the 40-th generation. Afterward, the algorithm stagnates and remains stuck with the Pareto front. It is therefore useless to devote more than 40 generations to the preselection. From Fig. 5.11, we assess that OTAs whose parameters are randomly initialized quickly disappear. At the end of the evolution process, the proportion of the old generation represents 95% of the population, confirming that the Pareto front is reached. With respect to the reference design, this optimization increases the GBW product by approximately 60%, for the same power consumption.

[1] We should mention that another possibility to use GAs would have been to enter all dimensions as input parameters. However, this would significantly deteriorate the computation time and the interpretability of the results.

Constraints	Value
OL Gain	40 dB
IRN	45 μV_{rms}
Phase margin	60°
Slew rate	0.06 $\frac{V}{\mu s}$
Offset	10 mV
CMRR	45 dB

Table 5.5: Constraints for the preselection step

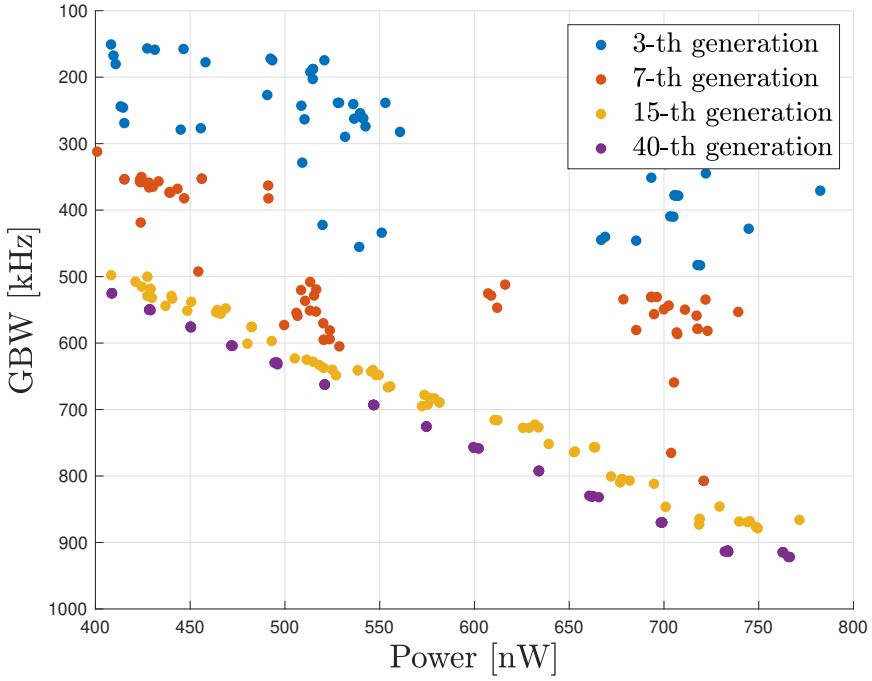


Figure 5.10: GBW product vs. power optimization - Preselection

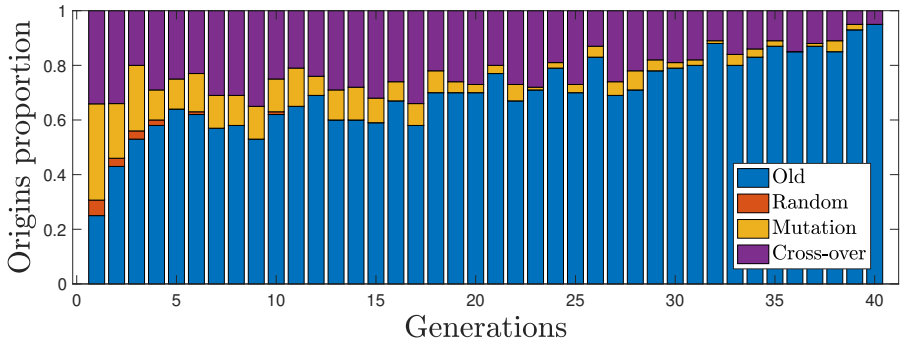


Figure 5.11: Population composition throughout the generations - Preselection

Fine-tuning

The noise vs. power optimization is initialized with the latest generation from preselection respecting the GBW product constraint at 550 kHz. As discussed previously, additional parameters have been added from preselection to fine-tuning. These new input parameters are summarized in Table 5.6. The constraints are not recalled here since the only change implies referring to the GBW product as a constraint.

Parameter	**Range**
Length of M_8 transistor, $L_{8,9}$	[1, 8] μm
Length of composite transistor (down), $L_{3a,4a}$	[1, 8] μm
Length of differential pair transistors, $L_{1,2}$	[1, 8] μm

Table 5.6: Additional parameters - Fine tuning

Referring to Fig. 5.12 the first generation already forms a kind of front. This is consistent as the noise scales inversely with the power provided to an OTA. The algorithm evolves less quickly because the new parameters easily unbalance the IM OTA. In this genetic optimization, 80 generations are required to reach an optimized design. Nevertheless, we observe that the ideal smooth Pareto front is not fully achieved after 80 generations, suggesting that there is still some room for optimization. Figure 5.13 confirms this assumption as we notice that the old proportion tends to decrease again slightly around the 77-th generation. However, we make the reasonable assumption that the room for improvement remains small and would require a more significant number of generations and more simulation time. This assumption is based mainly on the observed improvement from generation 50 to 80, which is meager. In addition, we note that the IRN has been divided by two with respect to the reference design (for approximately the same power consumption).

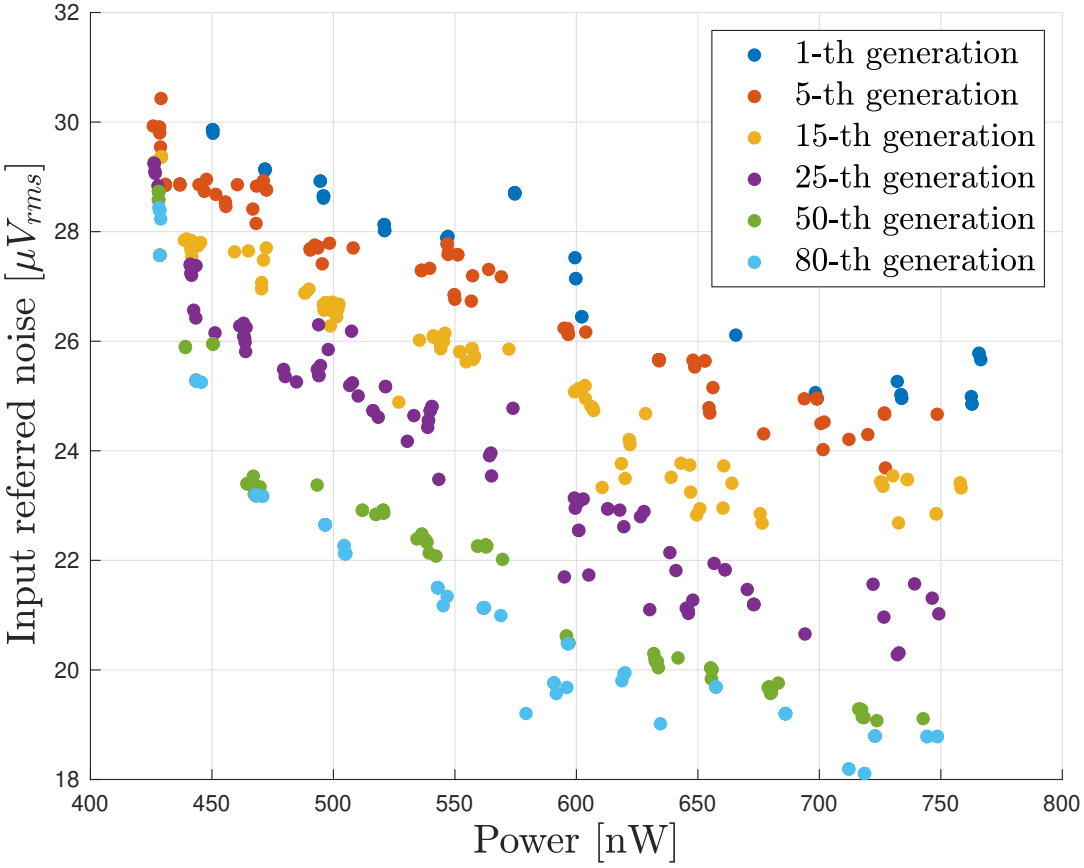


Figure 5.12: IRN-Power trade-off - Fine-tuning

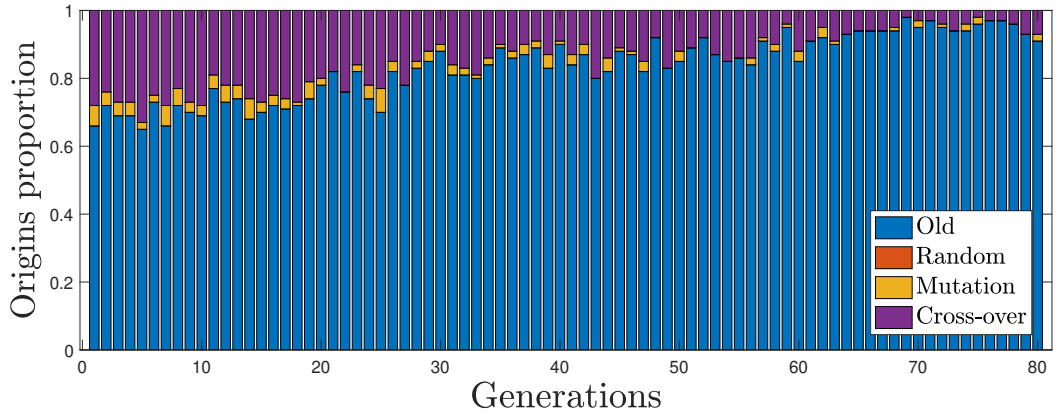


Figure 5.13: Population composition throughout the generations - Fine-tuning

5.8 PVT corners

As the final sensor will be employed in an outdoor environment, it is relevant to evaluate the performance of the optimized IM OTA in distinct temperature corners before moving to the last stage of the design, which is the layout. The lowest, typical, and highest temperatures are respectively -40°C, 25°C, and 85°C. The range [-40°C, 85°C] is referred to as the industrial temperature range [59]. Assuming a stable supply voltage, process corners also need to be addressed carefully. Moreover, by evaluating the temperature and process corners simultaneously and not independently, the robustness of the design is better assessed. Process corners are due to the manufacturing of the device. The variability associated with corners is either fast, typical or slow for both NMOS and PMOS transistors. This results in five main process corners respectively denoted as TT, FF, SS, SF and FS. We conclude that there are in total fifteen corners to be checked, regardless of supply voltage variation.

Regarding Table 5.7, we notice that all the open-loop gains still allow a gain of 30 dB in a closed-loop configuration as these are all significantly higher. From Eq. 2.2 we observe that the saturation voltage V_{dsat} scales linearly with temperature, implying that reaching saturation is more challenging at high temperatures as $V_{dsat,85^\circ} = 123\,mV$. It is therefore not surprising that the worst case occurs in the SS corner at 85°C. In this corner, the GBW product falls to 497.4 kHz, which means for $A_{v,LNA} = 30\,dB$ that the LP corner of the LNA is reduced to 15.73 kHz instead of being higher than 16 kHz. Considering that the probability of being in this corner is reasonably low and that the associated bandwidth loss is not significant, a new design implementation has not been searched.

Temperature	**Process corner**	**Open-loop gain [dB]**	**GBW [kHz]**
T = -40°C	TT	60.4	606.29
	FF	61.3	624.47
	SS	58.98	541.93
	SF	60.8	637.17
	FS	59.93	565.4
T = 25°C	TT	64.75	565.2
	FF	64.1	568.78
	SS	64.13	535.94
	SF	65.02	584.25
	FS	64.27	545.29
T = 85°C	TT	58.78	525.43
	FF	51.43	536.3
	SS	64.6	497.4
	SF	63.64	546.23
	FS	53.86	505.8

Table 5.7: Open-loop gain and GBW product performance for distinct temperature and process corners - IM OTA

5.9 Layout implementation of the improved Miller OTA

The realization of the layout respects the general considerations mentioned in Chapter 2. The transistors to be matched are the following: $M_{1,2}$, $M_{3a,4a}$, $M_{3b,4b}$ as well as all the transistors forming the biasing PMOS current mirrors network.

The common centroid arrangement of the PMOS current mirror was particularly laborious given its complexity and arrangement. Finally, it was realized so that the sources of these transistors are aligned and easily connectable to V_{DD}. The other blocks of matched transistors arranged in common centroid were less problematic to implement.

To implement the C_C capacitance, a MIM capacitor has been used, whose density is $2fF/\mu m^2$. A polysilicon resistor without salicide has been chosen to implement the series resistor as it exhibits a high resistance density of $153\,\Omega$/square. An illustration of the fully optimized IM OTA layout is presented in Fig. 5.14 and its corresponding Bode diagram is given in Fig. 5.15.

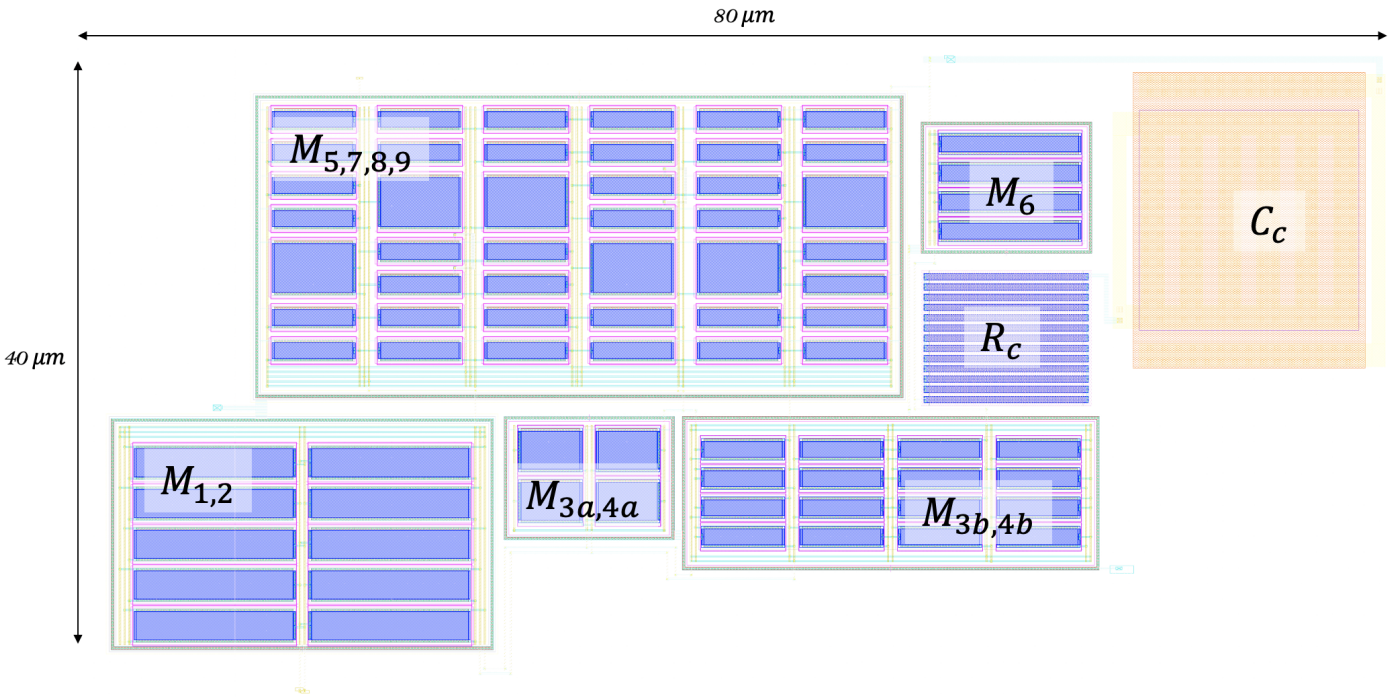


Figure 5.14: Layout of the fully optimized IM OTA

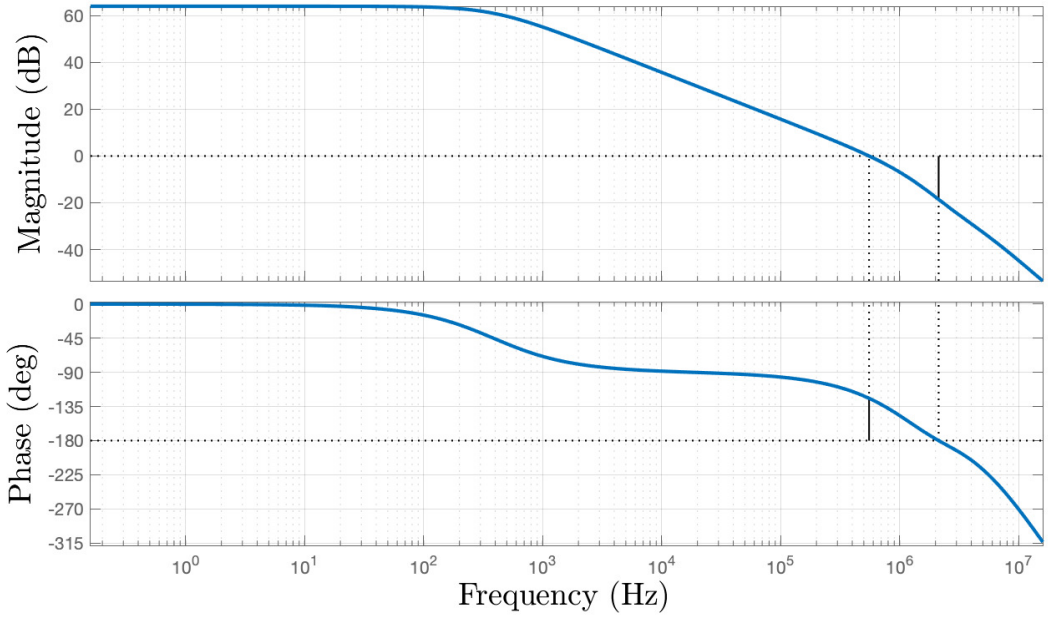


Figure 5.15: Bode diagram of the layout implementation - IM OTA

5.10 Performance summary

This section focuses on comparing the performance of the reference paper used for the OTA design [40], the implementation sized employing the g_m/I_D methodology, an IM OTA of the Pareto front of the preselection and the best OTA of the fine-tuning optimization. The comparative table 5.8 allows highlighting the trade-offs associated with each step of the sizing process for nearly similar power consumption.

First, we state that all implementations meet the power consumption requirement set in Chapter 4.

Second, the open-loop gain value is higher regarding the refining optimization performance. This makes sense as this optimization tends to increase the differential pair dimensions to improve the IRN value. Always concerning the open-loop gain, the initial paper features a higher value due to its technology. The intrinsic gain associated with transistors indeed decreases with technology scaling [48, 60].

Third, the GBW product achieved with the sizing process is more than one order of magnitude above the one of the reference paper. This was an expected result as the authors use a load capacitance value of $15\,pF$. We state that the GBW product increase during the preselection optimization, mainly due to a decrease in the C_c value. This increase of GBW product is obtained at the expense of phase margin as the non-dominant pole remains globally fixed by C_L, which is not an input parameter for the optimization process.

Another strength of the optimization manifests in the IRN value. It decreases by a factor of two from the implementation obtained with g_m/I_D methodology to refining. The obtained IRN level brought back in the acoustic domain is equivalent to $37\,dB_{SPL}$ level, which is below the minimum acoustic level of detection at $40\,dB_{SPL}$.

Finally, we state that the post-layout extraction maintains the performance from the optimization. We notice a slight decrease in open-loop gain and GBW product which is not damageable to the LNA performance. From schematic to post-layout extraction, a beneficial decrease in power consumption and input-referred noise is also stated. Moreover, a slight degradation of the phase margin is observed, which comes from the parasitic capacitances related to the routing.

Performance	[40]	g_m/I_D sizing	Preselection	**Fine-tuning**	Post-layout
Technology	$0.35\mu m$ CMOS	65nm LP CMOS	65nm LP CMOS	65nm LP CMOS	65nm LP CMOS
Open-loop gain [dB]	73.5	57	57.8	64.4	64
GBW product [kHz]	13	464	725	565	553
Power consumption [nW]	550	589	575	579	509
IRN [μV_{rms}]	NA	38.7	28.7	19.2	18.8
Phase margin [°]	54.1	79.57	62	61.7	55.7
Slew rate [V/μs]	0.015	0.185	0.277	0.214	NA
C_L [fF]	15000	100	100	100	100

Table 5.8: Comparison table: IM OTA performance throughout the whole design process

Chapter 6

Resistive feedback design and implementation

In order to finalize the design of the LNA, it is essential to find a suitable implementation for the feedback resistance R_f. The frequency response of the LNA points out the need for an enormous R_fC_f couple to implement a low HP corner below the 90 Hz target. However, we can neither rely on very high values of resistance and capacitance when it comes to on-chip implementation. Namely, MIM capacitors and polysilicon resistors suffer from poor density, requiring unacceptable silicon area. For instance, if we consider the expected value for $R_f = 20\,G\Omega$, a polysilicon resistor without salicide would occupy an unacceptable area of $34\,mm^2$ given its density. Therefore, we investigate alternative existing resistor types in this chapter and select an appropriate solution for our power target.

First, Section 6.1 begins with a search in state-of-the-art papers implementing large resistance without employing polysilicon resistors. Second, Sections 6.2 and 6.3 provide details on the chosen topology and its working principle. Afterward, Section 6.4 tries to find a right compromise for the sizing. Section 6.5 ends this chapter by providing a candidate solution to cope with the limitation of the chosen topology.

6.1 State-of-the-art search

Numerous designs emulating a resistive behavior exist in the literature. Among these designs, we find mainly switched-capacitor resistors and pseudo-resistors.

On the one hand, switched-capacitor resistors rely on clock signals to emulate the resistive behavior. These exhibit excellent tunability and show satisfying robustness to temperature and process corners. Nevertheless, these topologies require additional dedicated hardware for the clock signal generation, which consumes power. A state-of-the-art low-power topology that mimics a resistive behavior is typically found in [61]. The operating principle is based on a sample and average feedback resistor (SAFR), providing corner frequency programmability across temperature variation. Clock generation in such advanced work is estimated to 62 nW.

On the other hand, pseudo-resistors (PRs) can either consume power through biasing circuits [62] [63] or consume no power [64] [65]. In this case, PRs are used as passive circuit elements. Nevertheless, PR values are known to vary with respect to voltage swing, temperature, and frequency. Active PRs often aim at reducing those impacts.

A qualitative comparison between four distinct state-of-the-art topologies emulating a resistive behavior is presented in Table 6.1.

Features	[Deepu C.J.] [64]	[Zhang S.] [65]	[R. Nagulapalli] [63]	[Rothe R.] [61]
Architecture	Conventional PR	Swing-robust PR	Biased PR	SAFR
Application	ECG	ECG/EEG	ECG/EMG	Audio sensing
Technology	$0.35\,\mu m$ CMOS	$0.18\,\mu m$ CMOS	$65\,nm$ CMOS	$0.18\,\mu m$ CMOS
Tunability feat. by	Sizing/Trimming	Sizing/Trimming	Biasing current	Clock frequency
Power consumption	None	None	150 nW	62 nW
Sens. to voltage swing	High	Compensated	NA	NA
Sens. to PVT corners	High	High	Low (CTAT bias)	Minimized
Sens. to frequency	Relies on sizing	Relies on sizing	NA	Low

Table 6.1: Comparison between state-of-the-art architectures emulating a resistor

6.2 Design choice

First, when compared to the conventional PR implementation [64], the topology proposed in [65] shows improved robustness to voltage swing. Second, among the power-consuming architectures, [61] exhibits lower power consumption and a high robustness with respect to temperature. As such, two solutions emerge as our most suitable candidates.

The passive voltage swing robust PR by Zhang S. et al. was kept as design choice. As such, we avoid any power consumption overheads associated with clock generation or additional bias circuitry. Using the SAFR in the AO chain, the total power consumption associated with resistor implementations would represent 12 % of the AO chain target power consumption as a second resistor is required for the low-pass filter following the rectifier.

The chosen topology implements a pseudo-resistor that benefits from the complementarity of back-to-back MOS-bipolar PRs and back-to-back MOS PRs to propose an efficient passive architecture resilient to voltage swing. We explain the working principle of these architectures next. The exposed results in Section 6.3 are obtained for minimum size transistors.

6.3 Physics of the pseudo-resistor

MOS-bipolar pseudo-resistor

A MOS-bipolar pseudo-resistor has its gate connected to the drain and its bulk to the source as shown in Fig. 6.1. Considering a PMOS operating in sub-threshold, if a positive V_{BA} is applied, the device exhibits similar behavior to a diode-connected PMOS. On the contrary, if a negative V_{BA} is applied, the transistor is cut off and operates as a diode-connected BJT due to the parasitic P-N-P bipolar junction transistor that is activated. I-V, as well as Z-V characteristics, are presented in Fig. 6.3a.

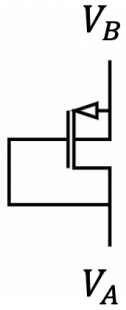


Figure 6.1: MOS-bipolar PR

MOS pseudo-resistor

A MOS pseudo-resistor is almost identical to a MOS-bipolar PR. As illustrated in Fig. 6.2, the bulk connection is changed. With a positive V_{BA}, it acts like a diode-connected MOS transistor. Unlike MOS-bipolar PRs, the n-well substrate is connected to a moderately lower voltage due to the present connections, typically implying a lower threshold voltage and increasing in turn the current in the channel. When a negative V_{BA} is applied, the device works as a reverse-biased PN junction. Hence, the reverse saturation current fixes the equivalent resistance. The I-V and Z-V curves for a MOS pseudo-resistor are presented in Fig. 6.3b.

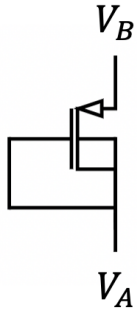
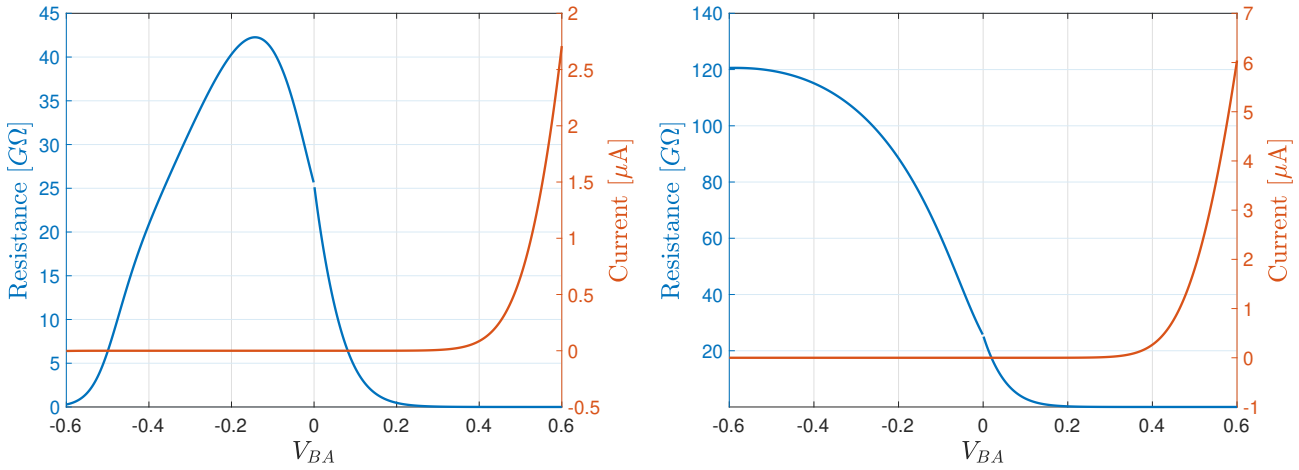


Figure 6.2: MOS PR



(a) MOS-bipolar pseudo-resistor

(b) MOS pseudo-resistor

Figure 6.3: I-V and Z-V curves. The slight increase in current associated with the MOS pseudo-resistor is equal to 3.5 μA at $V_{BA} = 0.6\,V$ in comparison with the MOS-bipolar pseudo-resistor.

Mathematical derivation of the equivalent resistance value

Both pseudo-resistor architectures have their PMOS transistors biased in sub-threshold regime. Therefore, we use Eq. 2.1 to derive a theoretical model of the equivalent resistance value. As a first step, the drain-to-source current is rewritten as [66]

$$I_{DS} = I_{S,0} \cdot e^{\frac{V_{GS}}{nU_T}} \cdot \left(1 - e^{\frac{-V_{DS}}{U_T}}\right), \tag{6.1}$$

with $I_{S,0}$ given by

$$I_{S,0} = \left(\frac{W}{L}\right) e^{\frac{-V_{th}}{nU_T}} \cdot I_S = 2n\mu C'_{ox} \cdot \left(\frac{W}{L}\right) \cdot {U_T}^2 \cdot e^{\frac{-V_{th}}{nU_T}}. \tag{6.2}$$

In this equation, n is the sub-threshold slope, C'_{ox} is the gate oxide capacitance per unit area, μ represents carrier mobility and U_T is the thermal voltage. Focusing on the point where $V_{GS} = 0$ and $V_{DS} = 0$, the equivalent resistance value can be derived from Eq. 6.1 as

$$\begin{aligned} R_{eq} &= \left[\left.\frac{\partial I_{DS}(V_{DS})}{\partial V_{DS}}\right|_{V_{DS=0}, V_{GS=0}}\right]^{-1} \\ &= \left[\frac{I_{S,0}}{U_T}\right]^{-1}. \end{aligned} \tag{6.3}$$

This simple but yet comprehensive model allows instantly catching most of the inference of the parameters on the equivalent resistance value near $V_{BA} = 0$.

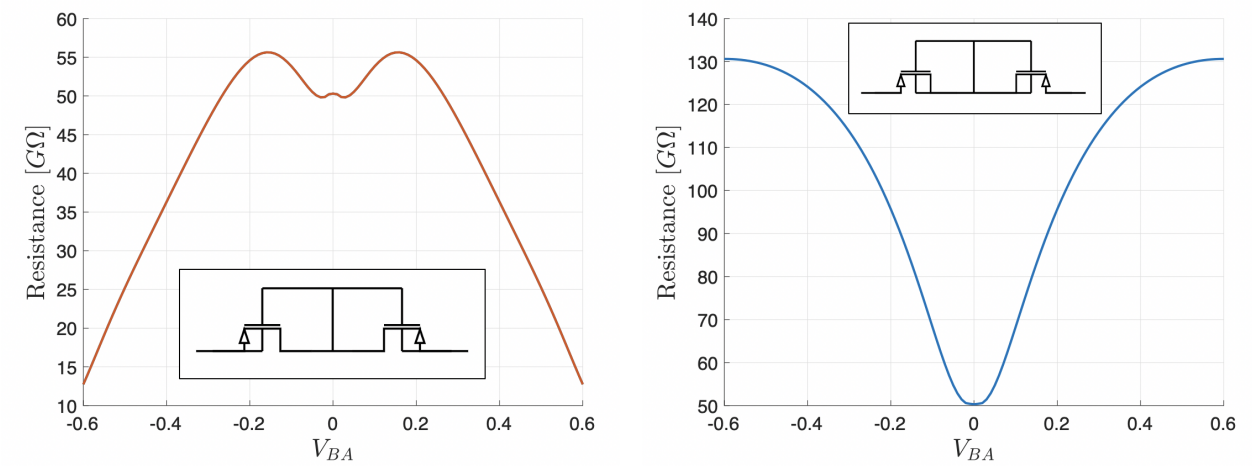
Assuming a constant temperature, the resistance value scales inversely with the aspect ratio $\left(\frac{W}{L}\right)$. A transistor in a diode configuration shows a higher equivalent resistance if its channel is large. On the other hand, we notice the μ factor linked to the mobility of the charge carriers (holes in PMOS). Hence, it is understandable why high-values PRs are more frequently implemented with PMOS transistors as electrons mobility in NMOS is approximately three times higher than holes mobility. Focusing on the exponential term in Eq. 6.2, we finally state that transistors with a low-threshold voltage (lvt) are more susceptible to target lower resistance values than high-threshold voltage (hvt) transistors.

The way frequency and PVT corners impact the equivalent resistance is rather complex and will be addressed in Section 6.4.

Back-to-back configurations

In practice, single MOS-bipolar PRs or MOS PRs cannot be used to emulate resistors as these do not exhibit symmetrical characteristics around $V_{BA} = 0$. To cope with this issue, we can rely on a simple implementation trick that consists in putting pseudo-resistors back-to-back in series. The simulation results are presented respectively for the MOS-bipolar PR and MOS PR in Figure 6.4a and 6.4b.

For both configurations, we notice that the resistance value at $V_{BA} = 0$ is twice the value of a single transistor configuration. This makes sense as resistances in series add up.

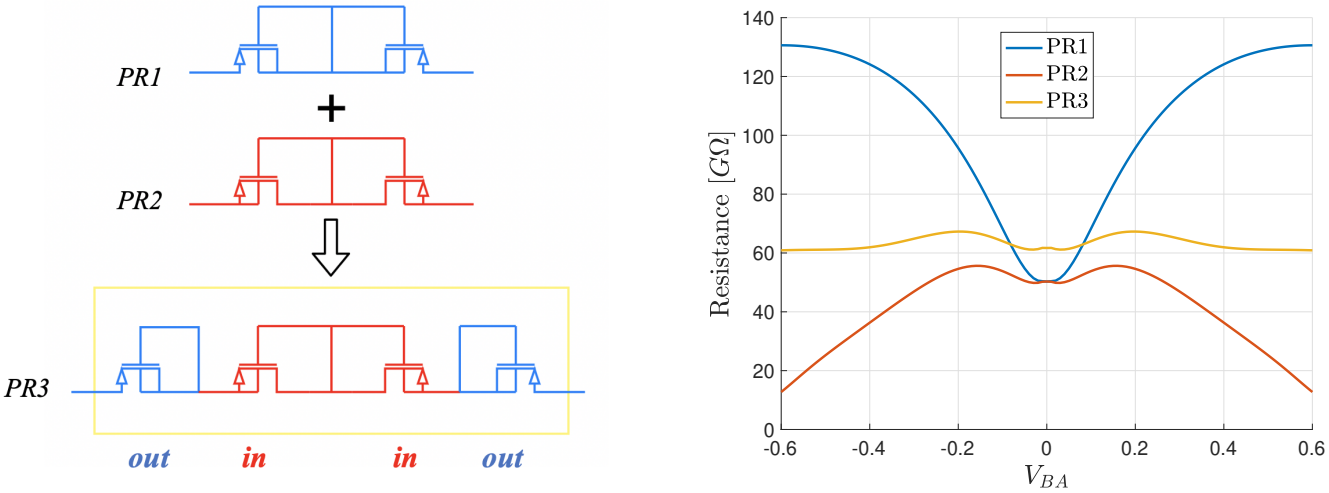


(a) Back-to-back MOS-bipolar pseudo-resistor (b) Back-to-back MOS pseudo-resistor

Figure 6.4: Back-to-back configurations

Voltage swing robust pseudo-resistor

Let us denote PR1 the back-to-back MOS PR and PR2 the back-to-back MOS-bipolar PR for the sake of readability. The most interesting aspect of the curves presented in Fig. 6.4 is their complementarity. We can take advantage of this complementarity by combining PR1 and PR2 as represented in Fig. 6.5a. As such, the resistance values compensate each other across V_{BA} to feature a voltage swing robust pseudo-resistor named PR3. Still, as the resistances values of PR1 and PR2 do not exactly compensate each other across V_{BA}, a weighting between the PR1 and PR2 dimensions is required. Considering the same lengths and widths for the transistors, this weighting process is obtain using multipliers. Simulations have shown that the best results occur for a multiplicative factor of $W_{PR3,out}/W_{PR3,in} \approx 5$. Simulation results are presented in Fig. 6.5b.



(a) Combination of PR1 and PR2 (b) Simulation results

Figure 6.5: Voltage swing robust pseudo-resistor. The combination of PR1 and PR2 yields a voltage swing robust pseudo-resistor.

To quantify the improvement, we rely on the root mean square error (RMSE) between the ideal resistance value (at $V_{BA} = 0$) and the actual resistance value across V_{BA}. Mathematically this translates to

$$RMSE = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(R_i - R|_{V_{BA}=0}\right)^2}\,, \tag{6.4}$$

with N the number of points at which the resistance have been evaluated and R_i the resistance at a given value of V_{BA}. The results are provided in Table 6.2 and clearly show the improvement on voltage swing robustness for PR3.

Metric	PR1	PR2	**PR3**
RMSE $[G\Omega]$	59.8	16.1	**2.8**

Table 6.2: Performance comparison based on the RMSE between PR1, PR2 and PR3

6.4 Sizing

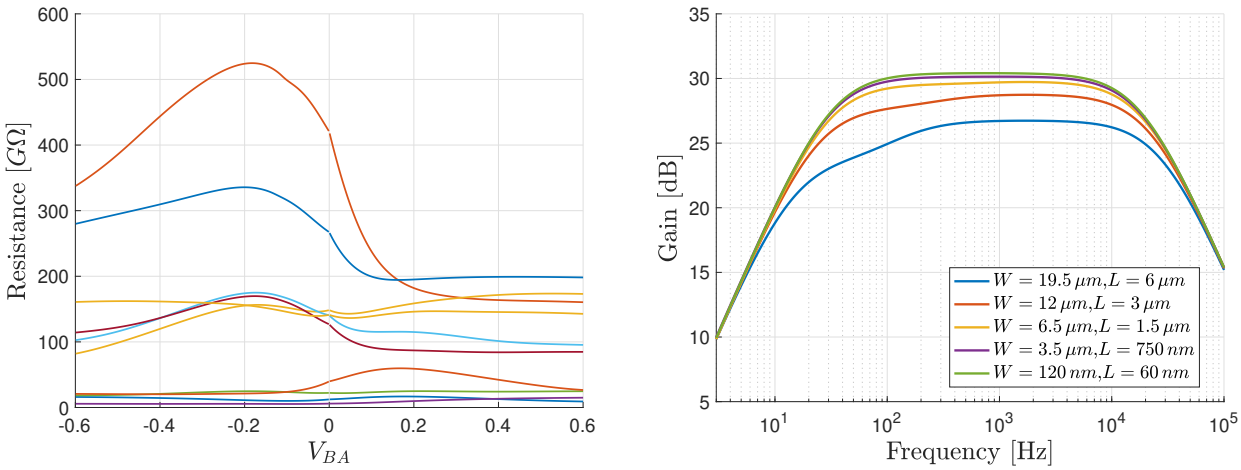
As the voltage swing issue has been addressed, we should be careful with fluctuations of the resistance value due to changing frequency, statistical variability due to local mismatch and PVT variations. Given the PR3 topology, the sizing can be realized in order to limit the two first issues. However, PVT corners have a huge impact and cannot be solved by sizing.

Statistical variability and frequency response

Unfortunately, sizing requirements to cope with resistance fluctuation induced by frequency and statistical variability go against each other. Indeed, mismatch issues that result in center resistance variations and non-symmetrical characteristic around $V_{BA} = 0$ can be alleviated by increasing the dimensions of the transistors. With minimum size transistors, a Monte-Carlo simulation with only ten runs is shown in Fig. 6.6a.

However, larger dimensions translate to larger parasitic capacitances. First, in Fig. 6.6b, we state that the larger the PR3 dimensions, the less the LNA gain. We hypothesize that this issue is due to the addition of the parasitic capacitances of PR3 to the LNA feedback capacitance C_f. Hence this decreases the gain as $A_{v,LNA} = \frac{C_1}{C_f}\left[\frac{V}{V}\right]$. Second, for the largest dimensions (blue and red curves), we observe that the gain is distorted around the HP corner. As $f_{HP,LNA} = \frac{1}{2\pi \cdot R_f C_f}$, if the R_f strongly depends on frequency, it is not surprising to state a gain distortion around the HP corner.

Both phenomena are unacceptable, and a trade-off between these has to be found. The constraints are: maintaining at least 30 dB gain without HP corner distortion while providing the minimum standard deviation with respect to the pseudo-resistor target value. We find the best compromise satisfying constraints in gain variability and statistical variability by sweeping $W_{PR3,in}$ and L_{PR3} while maintaining the multiplicative ratio between $W_{PR3,out}$ and $W_{PR3,in}$ to feature voltage-swing robustness. The result is shown in Fig 6.7. The expected value for the LNA feedback resistance R_f is 20 $G\Omega$. However, we state in this figure that the design space targeting this value is very narrow (orange area). To enlarge the design space and provide a better evaluation of the trade-off, we target a resistance value of 80 $G\Omega$ (green area) that can be set in a parallel configuration to obtain the expected value. In this area, we highlighted nine sizing candidates for PR3. The results in Table 6.3 show the performance for each sizing candidate.



(a) Monte-Carlo simulation - Minimum size PR3 (b) Impact of PR3 sizing on the LNA response

Figure 6.6: Issues encountered with minimum size transistors (left) and larger transistors (right).

Candidate	L_{PR3} [μm]	$W_{PR3,in}$ [μm]	σ_{PR3} [$G\Omega$]	$A_{v,LNA}$ [dB]	HP corner distortion [dB]
1	0.5	1.9	34.8	30.3	None
2	0.75	2.55	32	30.2	None
3	1	3.15	30.8	30.1	None
4	1.25	3.85	29.5	30.1	None
5	**1.5**	**4.6**	**28.3**	**30**	**None**
6	1.75	5.3	27.6	29.8	-0.2
7	2	6.1	26.3	29.7	-0.3
8	2.25	6.8	26	29.5	-0.4
9	2.5	7.4	25.1	29.4	-0.5

Table 6.3: Evaluation of the trade-off for the distinct sizing candidates targeting a same 80 $G\Omega$ value. The HP corner distortion is defined as the difference between $A_{v,LNA}$ and actual the gain value at 100 Hz, which is above the HP corner.

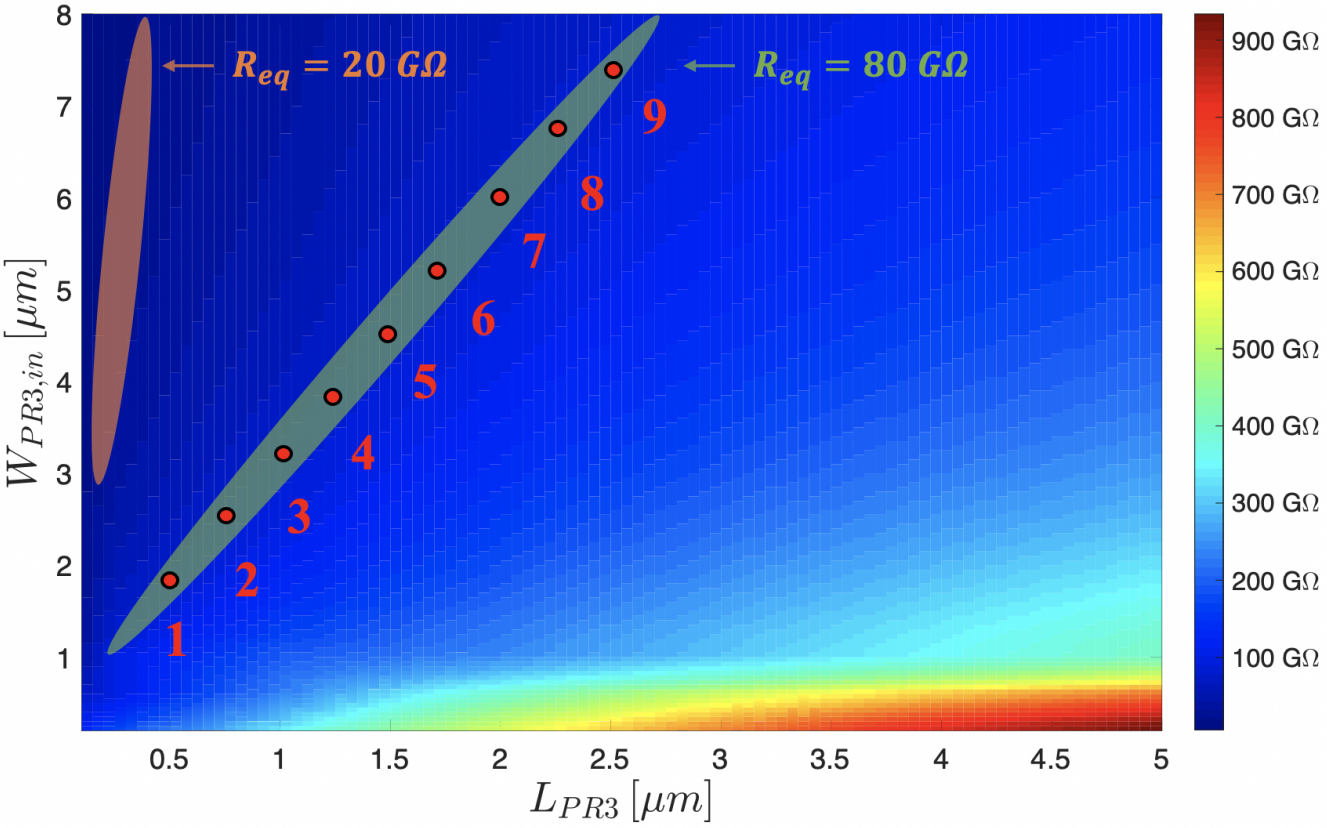


Figure 6.7: In this figure, we highlight the design area for a PR3 targeting a 20 $G\Omega$ value and an 80 $G\Omega$ value. We state that the second design area is more significant, allowing a better evaluation of the trade-off. The selected candidate is number 5.

The chosen sizing is number 5 as it exhibits no gain distortion before the HP corner while maintaining $A_{v,LNA} = 30\,dB$. Despite this sizing candidate offers the best compromise between gain variability and statistical variability constraints, we state that the standard deviation still corresponds to 35% of the $80\,G\Omega$ target value. This is enormous and a trimming solution needs to be introduced. This solution is discussed in Section 6.5.

PVT corners

Equation 6.3 allows anticipating a considerable variation in equivalent resistance value with respect to PVT corners. In particular, we know that both the thermal voltage and mobility impact the equivalent resistance value. The thermal voltage scales linearly with the temperature, while the mobility tends to decrease for an increasing temperature [67]. In addition, process variations typically impact the threshold voltage and the sub-threshold slope factor. The overall impact of PVT corners on PR3 is thus challenging to describe by an equation due to the combination of PR1 and PR2 and the numerous impacted parameters.

Temperature and process corners have been simulated simultaneously for the sake of completeness. The results are presented in Fig. 6.8. The lower the temperature, the higher the resistance value, meaning that the impact of the U_T through the exponential and quadratic term in Eq. 6.2 is dominant. While voltage swing robustness is maintained for all corners, we state a two order of magnitude variation for the equivalent resistance from -40°C corners to 85°C corners. The variability with PVT corners raises a real issue confirming the need for a trimming solution, already discussed in the previous subsection.

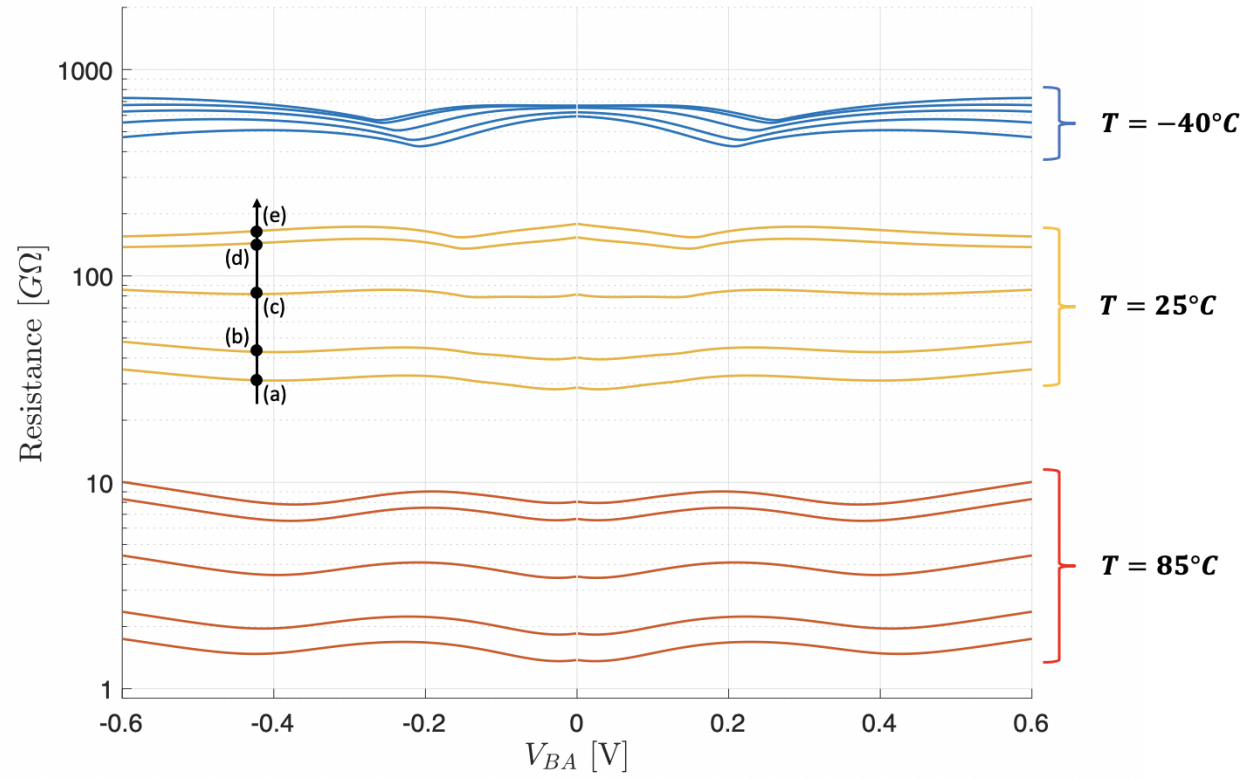


Figure 6.8: Pseudo-resistor (PR3) value across PVT corners. The arrow on the left hand side of the figure indicates the respective corners : (a) FF, (b) SF, (c) TT, (d) FS, (e) SS. This order is the same at each temperature.

6.5 Further discussion - Trimming solution

We propose a digital trimming solution featuring a programmable pseudo-resistance to cope with the statistical variability and PVT corner issues. Considering the solution presented in Fig. 6.9, the range of resistances values covers two orders of magnitude $[R/4, 15R]$ where R represents the equivalent value of a single PR3. The number below the resistance provides the number of series-connected PRs. This architecture requires huge switched-off resistance values so that the switches do no interfere with the equivalent resistance value.

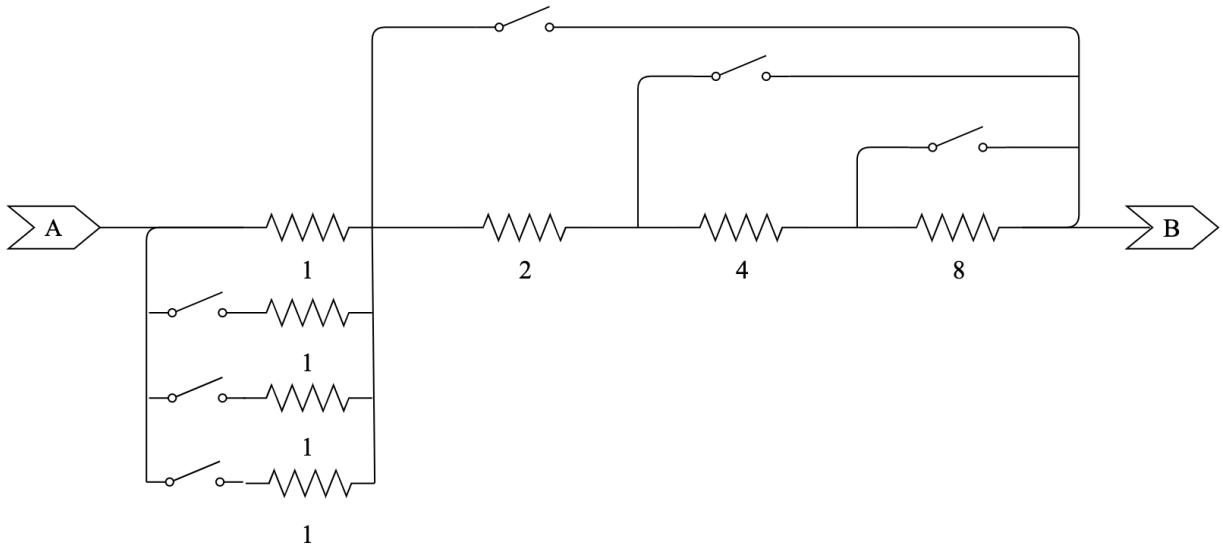


Figure 6.9: Potential trimming solution featuring a programmable pseudo-resistor. This would allow coping with the variation of the equivalent resistance with statistical variability and PVT corners.

This trimming solution could feature real-time temperature compensation in this application but this would require a temperature sensor embedded on the edge of the device. However, this is not guaranteed and would bring additional power overhead. The implementation of this solution is beyond the scope of this work but should be considered and evaluated if the pseudo-resistor model chosen for the final sensor matches the one proposed in this chapter.

Chapter 7

Energy detection stage

This chapter focuses on the extraction of the signal energy from the LNA. Obtaining a metric reflecting the energy of an AC signal cannot be performed directly on the signal centered around half-V_{DD}. We have to convert the energy contained in an AC signal into a DC quantity reflecting this energy. Such a task can be typically achieved by a rectifier followed by a low-pass filter. The low-pass filter does not strictly extract the energy of the AC signal but rather performs an averaging of the rectified signal. As the low-pass filter implementation is relatively straightforward, this chapter emphasizes the design and implementation of the rectifier circuit, which is more challenging.

Several FoMs for the rectifier are discussed in Section 7.1. Sections 7.2 and 7.3 provide the design choice for the rectifier and its working principle. The sizing process is established in Section 7.4 and the main simulation results presented in Section 7.5. A critical discussion on the circuit sizing is developped in Section 7.6. Afterward, Sections 7.7 and 7.8 propose respectively the layout implementation of the rectifier and a summary of its performance. This chapter ends by the implementation of the low-pass filter in Section 7.9.

7.1 Main figures of merit

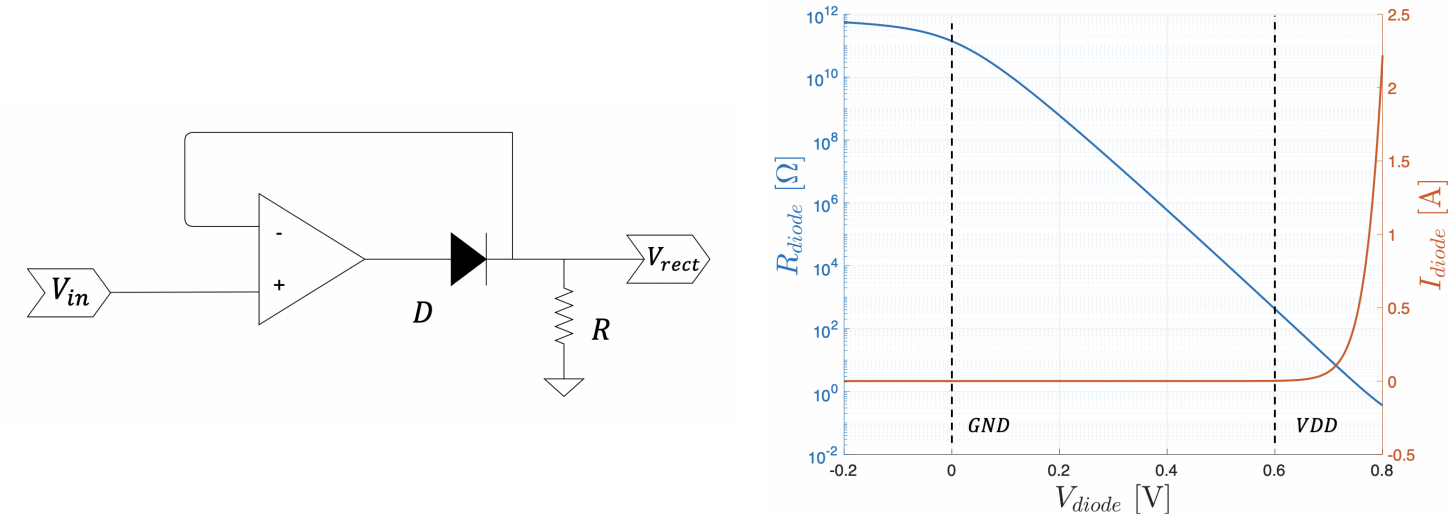
Concerning the rectifier circuit, it is more challenging to establish well-defined figures of merit. As a rule of thumb, it is beneficial for the rectifier to provide some gain while adequately maintaining the required bandwidth and preserving the signal integrity. This latter requirement means limiting the noise, avoiding distortions and offsets on the signal. These notions will be discussed in the context of this chapter.

7.2 Design Choice

A rectifier essentially operates by successively blocking and passing part of an AC signal. Half-wave rectifiers keep only one-half of the AC cycle, full-wave rectifiers keep both cycles while rectifying one. The key electrical component in rectifiers is the diode. Various rectifier implementations exist in the literature, with common architectures mostly targeting applications in power electronics: the simple rectifier, the diode bridge and the precision

rectifier. By operating in the voltage domain, one intrinsic limitation with rectifiers is the diode dead-zone induced by the threshold voltage $V_{th} = 0.7\,V$ (for silicon diodes). Indeed, the voltage across a diode needs to overcome V_{th} before conducting.

The first design choice for the rectifier implementation led to choose the precision rectifier, represented in Fig. 7.1a. Indeed, this topology allows coping with the diode dead zone by connecting the anode of the diode to the output terminal of an amplifier and the cathode to the negative input terminal. Thus, when the voltage alternates positively at the positive input terminal of the amplifier, the diode is conducting, and the amplifier is in a follower configuration. Conversely, when the voltage alternates negatively, the diode is blocked, and the output node remains constant at 0V. As a consequence of the low supply voltage in this work, the amplifier output ranges from 0 to 0.6 V, typically yielding a diode that never actually reaches its conducting mode but instead adopts the behavior of variable resistance as it never goes beyond V_{th}, as shown in Fig.7.1b. We conclude that this topology suits amplifiers with higher supply voltages.



(a) Precision rectifier architecture

(b) I-V and Z-V characteristics of a diode

Figure 7.1: Study of the precision rectifier illustrating the variable resistance issue in the supply range.

Another effective approach for the problem is to achieve the rectifying operation in the current domain [68] [69] [70]. However, most topologies introduced in the literature exhibit power consumptions above µW, violating our specifications. The selected circuit for the AO chain is a half-wave rectifier performing the rectification operation in the current domain, but dedicated explicitly to low-power audio applications [71]. First, the AC voltage is converted into a current by a transconductance amplifier G_m. Then a current-mode rectifier only keeps half of the AC cycle. Finally, the current is converted back into the voltage domain by a transimpedance amplifier ${G_m}^{-1}$.

7.3 Working principle

The topologies proposed for the G_m, current-mode, and G_m^{-1} blocks in the reference paper have been kept identical for the sake of comparison at the end of this chapter.

Transconductance amplifier - G_m

A simple differential-pair OTA including five transistors is used to realize the transconductance stage that converts the voltage into a current. The topology is presented in Fig. 7.2. Key benefits of this simple topology are minor mismatch effects, low power consumption, and low noise. Wide transistors for $M_{3,4}$ and M_B are favored to improve on voltage swing. Increasing the sizes of $M_{1,2}$ is beneficial for the matching of the differential pair, offering lower input offset according to Pelgrom's law, already considered in Section 5.1. The voltage $V_{bias,gm}$ controls the main power consumption of the OTA as it controls its biasing current.

In this case, only the positive input terminal of this OTA is connected to the AC signal from the LNA. Hence the negative input terminal V_{inm} can be connected to a biasing voltage, helpful to center the output current around 0 A. Undoubtedly, an apparent mismatch between positive peak current value and negative peak current value, i.e., a DC current shift, would generate incorrect rectified current values at the current-mode rectifier output.

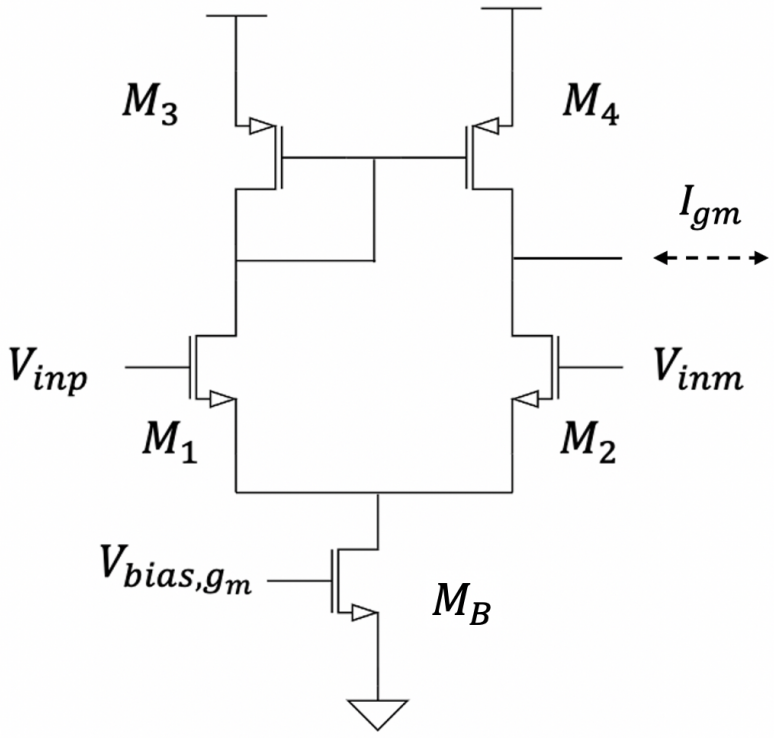


Figure 7.2: A tranconductance amplifier implemented with a simple differential-pair OTA.

Current-mode rectifier

The topology implementing the current-mode rectifier is presented in Fig. 7.3. The purpose of this circuit is straightforward and consists in keeping only the positive current I_{out} from the input current I_{gm}.

The critical elements in this topology are transistors $M_{5,6}$ that emulate a current-mode diode behavior. The gate voltages of these transistors are $Bias_{up}$ and $Bias_{down}$. Along with sizing, these gate voltages impact the conductivity of M_5 and M_6, allowing to tune the diode characteristics. These transistors also essentially act as the load for the G_m circuit. The current peak values can be increased if we increase $W_{5,6}$ or bring $Bias_{up}$ (resp. $Bias_{down}$) closer to the positive (resp. negative) rail. Attention must be paid to the diode biasing and sizing as higher currents mean higher power consumption.

Furthermore, transistors $M_{8,9}$ form a current mirror, providing a copy of the drain current flowing through M_6 to I_{out}. Sufficiently large dimensions should be considered to have long-channel transistors, ensuring a small mismatch and a decrease in non-linearity associated with drain-to-source voltage variation. Finally, an additional transistor M_7 was added in [71] to cope with the slew rate occurring at the beginning of the conduction of M_8. M_7 thus provides M_8 with a tiny current to ease initial conduction while the inversion layer is forming under its gate. This current $\approx 2\,nA$ is typically lower than $I_{gm} \approx 45\,nA$ (for the smallest acoustic signal) considering $Bias_7 = 500\,mV$ and $\left(\frac{W_7}{L_7}\right) = \left(\frac{5\mu m}{1\mu m}\right)$. It has been explicitly removed as a design choice to improve power consumption.

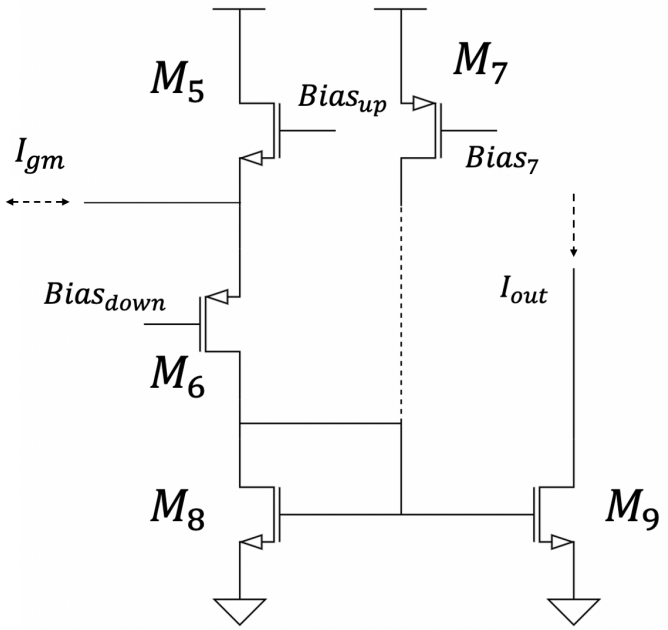


Figure 7.3: Current-mode rectifier. The key transistors in this topology are $M_{5,6}$ emulating a current-mode diode

Transimpedance amplifier - G_m^{-1}

A resistance value is needed at the end of the rectifier to convert the current back into the voltage domain efficiently. Typical on-chip resistance values are limited to tenths of $k\Omega$, while pseudo-resistors developed in Chapter 6 typically target range spanning from $G\Omega$ to $T\Omega$. Unfortunately, the resistance value required at the end of the rectifier falls into a dead zone between these two ranges, i.e., hundreds of $k\Omega$. A transconductance block in negative feedback is chosen to emulate a resistive behavior. An illustration of this circuit is presented in Fig. 7.4. The argument favoring a doublet differential pair is improved linearity over the input range. By adding this doublet differential pair, the saturation level for I_{out} is 87 % higher than with a simple differential pair. The drawback with this implementation is the area overhead. The ratio between gate-connected transistors of the differential pair M_{11}/M_{13} and M_{12}/M_{14} is kept high to improve resilience against distortion.

Referring to Fig. 7.4, when the current $I_{out} = 0\,nA$, we have $I_{D,15} = I_{D,11} + I_{D,13}$ (blue arrows). To provide current as I_{out} increases, $I_{D,15}$ increases while $I_{D,11} + I_{D,13}$ decrease (red arrows). As a results, a negative voltage appears at node V_{out} due to the current-to-voltage conversion by the transimpedance block. If I_{out} is huge, M_{11} and M_{13} are shut off and $I_{D,11} = I_{D,13} = 0\,nA$. In this case all the current available from the bias sources flows into M_{16}, is mirrored by M_{15} and a saturation level is reached.

The bias voltages play an essential role in this topology. Indeed, $V_{bias,1}$ is used to properly maintain the DC level of the output voltage at half-V_{DD} while $V_{bias,2}$ determines the drain currents that flow through M_{17} and M_{18} and therefore the available current for I_{out}. As for the transconductance amplifier, $V_{bias,2}$ dictates the power consumption as it controls its biasing current and should be carefully selected in that regard.

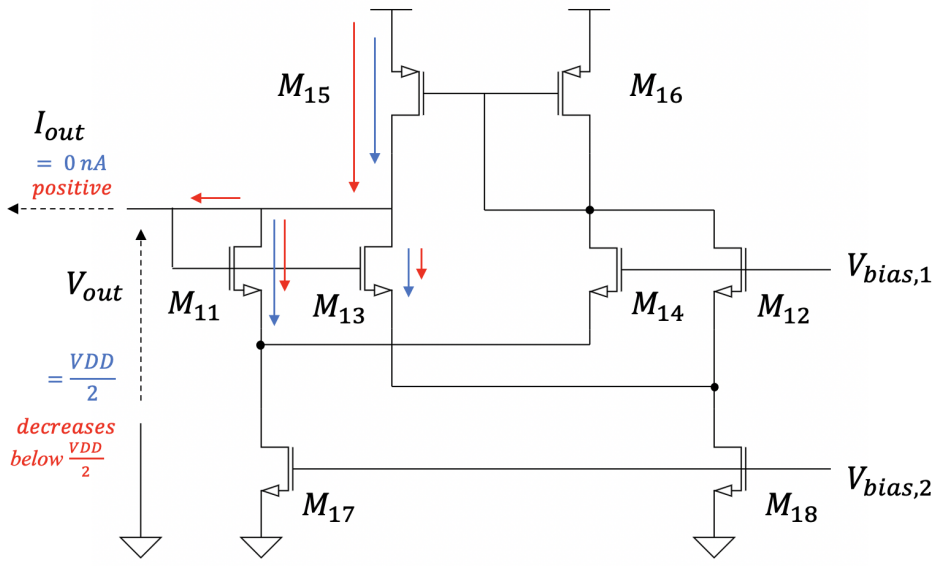


Figure 7.4: Schematic of the transimpedance amplifier illustrating the different behaviors with $I_{out} = 0\,nA$ and I_{out} increasing.

Rectifier gain - Theoretical approach

One advantage in using transconductance and transimpedance amplifiers together is the ratio that these form between g_m and g_m^{-1}. The rectifier features gain according to

$$A_{v,rect} = 20 \log \left(\frac{g_m}{g_m^{-1}} \right) \qquad [\text{dB}] \,. \tag{7.1}$$

A major aspect that allows maintaining a linear gain for distinct input signals amplitudes is the sizing of the transconductance and transimpedance amplifiers as well as the $V_{bias,2}$ voltage. This will be discussed in Section 7.5. A typical gain of 6 dB can be targeted.

7.4 Sizing process

The combination of the three rectifier sub-blocks with different constraints makes its sizing challenging. Necessarily, the operating behavior of one block must not disturb one of its neighbors. The purpose of the sizing is to feature a proper rectifying operation and a rectifier gain that varies as few as possible with respect to the input voltage. We relied upon an iterative sizing process, depicted in Fig. 7.5. We state that this sizing is split up into two parts, the first dedicated to the sizing of two first blocks and the second dedicated to the transimpedance block sizing when the G_m and current-mode rectifier efficiently perform the current rectification. The dimensions of the transistors resulting from this sizing are presented in Table 7.1 and the biasing voltages in Table 7.2.

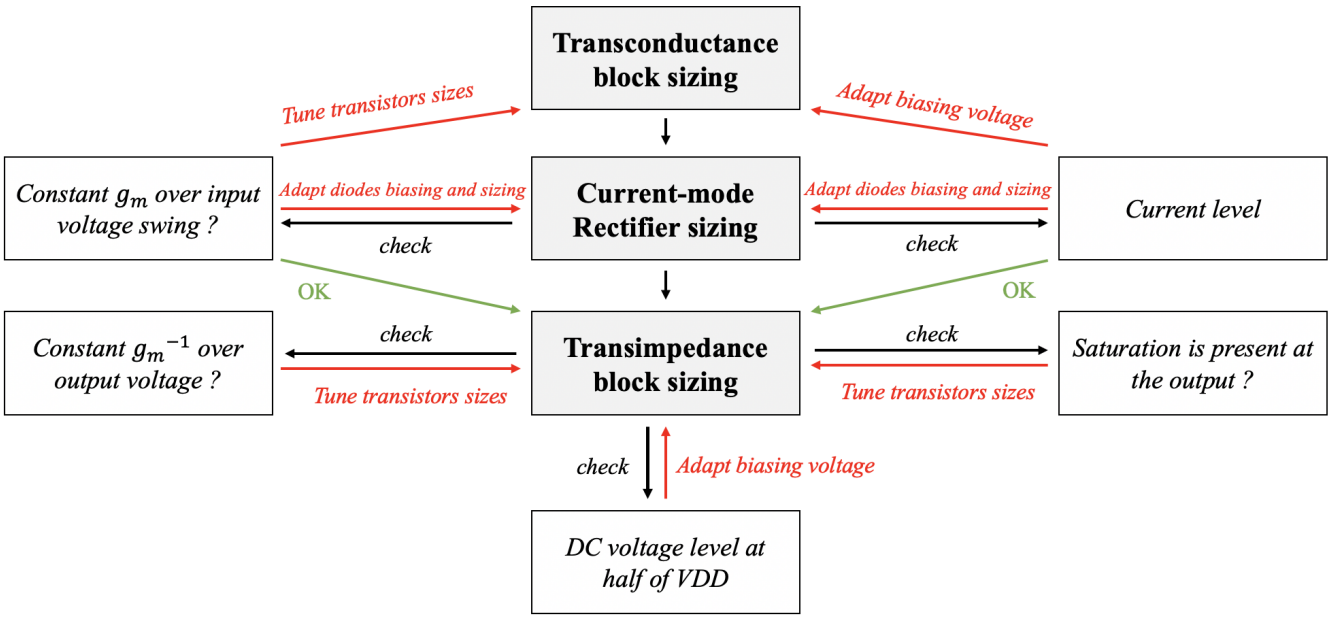


Figure 7.5: Iterative sizing process for the half-wave rectifier

Stage	Device	Aspect ratio ($\mu m/\mu m$)
Transconductance amplifier	M1, M2	5/1
	M3, M4	20/1
	MB	20/1
Current-mode rectifier	M5	1/15
	M6	2.5/15
	M8, M9	5/1
Transimpedance amplifier	M11, M12	28/1
	M13, M14	4/1
	M15, M16	30/1
	M17, M18	4/1

Table 7.1: Transistors sizes - Half-wave rectifier

Bias voltage	Value [mV]
V_{inm}	303
$V_{bias,gm}$	200
$V_{bias,up}$	500
$V_{bias,down}$	100
$V_{bias,1}$	292
$V_{bias,2}$	206

Table 7.2: Bias voltages - Half-wave rectifier

It is crucial to remain critical regarding the proposed sizing. As it is the case for the other analog circuits, the sizing is by no means unique and will be critically discussed in section 7.6.

7.5 Simulation results

Typical transient simulation

Figure 7.6 shows a typical transient simulation that illustrates the main voltage and current waves throughout the rectifier. A sinusoidal voltage with $V_{peak} = 50mV$ at $1\,kHz$ has been applied at the input of the transconductance amplifier.

It can be seen that the gain is 6 dB (factor 2) as the peak value of the rectified signal is $V_{peak,rect} = 300\,mV - 2 \cdot 50\,mV = 200\,mV$. Moreover, Spice simulations yield a power consumption of 420 nW for the considered sizing.

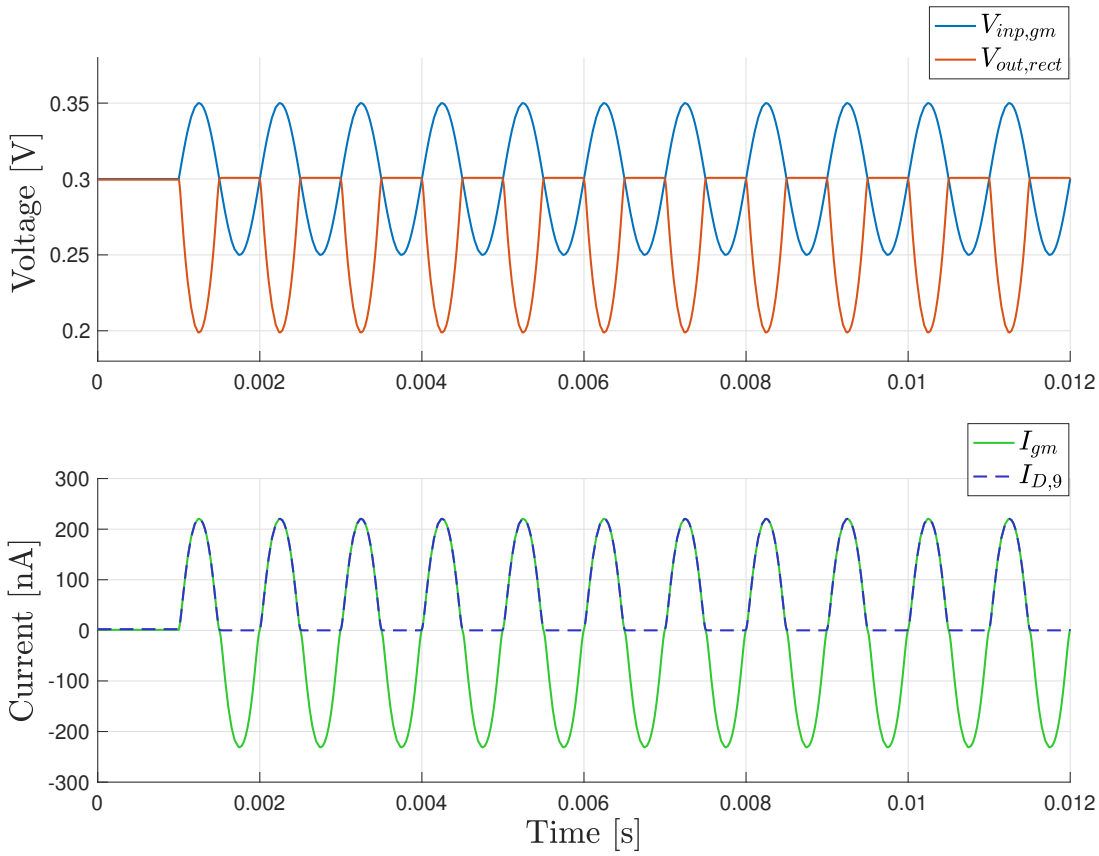


Figure 7.6: Typical transient simulation - Half-wave rectifier

Rectifier gain

Figure 7.7 illustrates the rectifier gain for distinct values of $V_{bias,2}$, as the latter bias voltage plays an essential role in the value of g_m^{-1} and the linearity of the rectifier gain. We can observe that a slight change of $V_{bias,2}$ ($\pm 4\,mV$) impacts the linearity of the gain.

In addition, there is an apparent saturation phenomenon occurring when V_{in} reaches 100 mV. This saturation is the consequence of the limit current that M_9 can draw from the transimpedance block. Indeed, when a large input voltage arrives at the transconductance block input, this results in a significant rectified drain current $I_{D,9}$. On the transimpedance block side, $M_{11,13}$ are thus shut-off, and the total current from the bias transistors $M_{17,18}$ is provided to M_9. As a consequence, if this current is insufficient, saturation will occur. An idea could be to diminish the g_m value in order for the current I_{gm} to be lower, but this would also directly affect the overall rectifier gain according to Eq. 7.1.

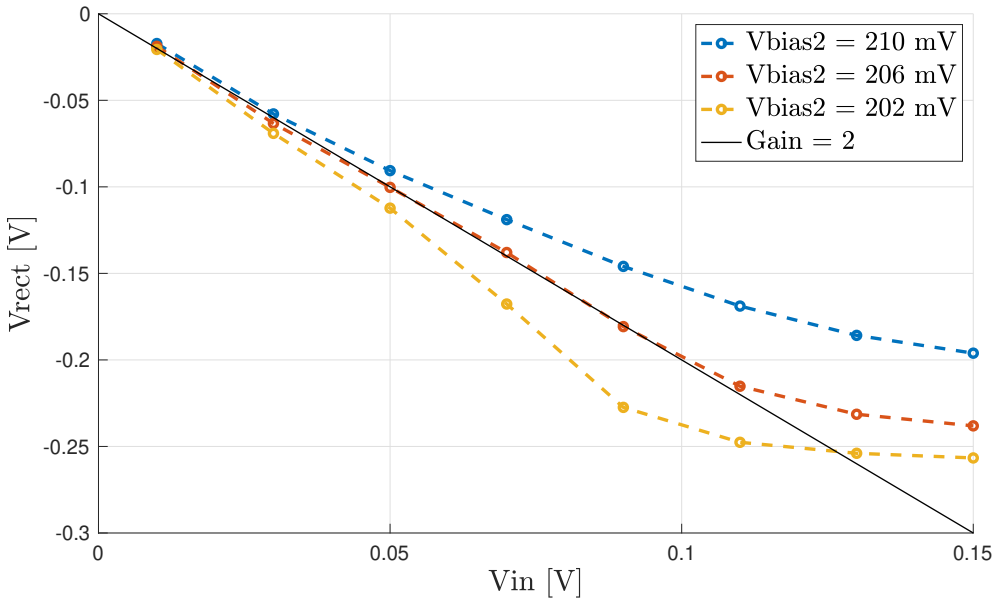


Figure 7.7: Half-wave rectifier gain. V_{in} represents the input of the circuit (stated V_{inp} previously), V_{rect} is the voltage amplitude at the output of the rectifier (stated V_{out} previously). This figure clearly highlights the impact of $V_{bias,2}$ on the gain linearity.

Frequency response

To ensure that the rectifier can operate at a frequency higher than 16 kHz, we study its frequency response. It is presented in Fig. 7.8. We state that the 6 dB gain is maintained well beyond the maximum target frequency.

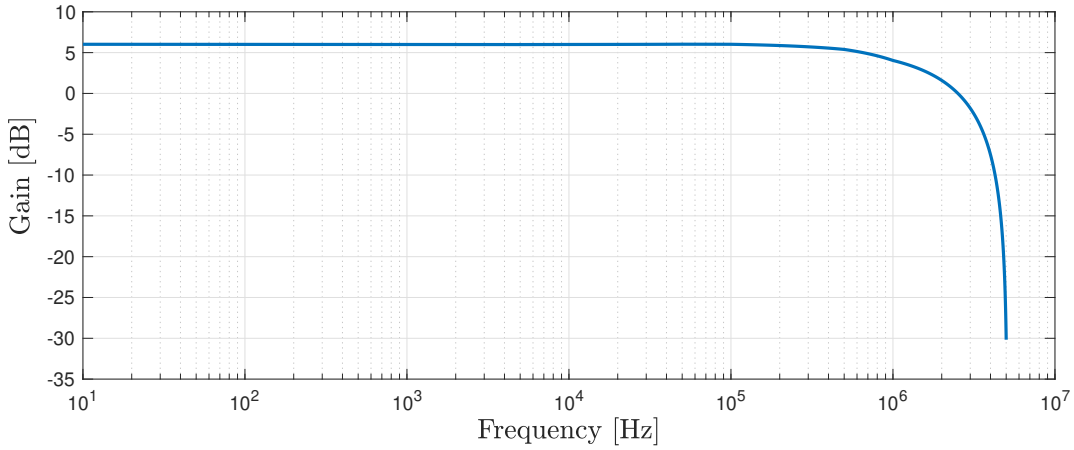


Figure 7.8: Frequency response - Half-wave rectifier

7.6 Further improvements

In the current state of the circuit, power consumption is already acceptable. Thanks to supply voltage reduction with respect to the reference paper ($V_{DD} = 1\,V$), a 30% improvement in power consumption has been obtained. However, the discussion on rectifier gain paves the way for further power reduction. Indeed by simultaneously decreasing the g_m and g_m^{-1} mainly through a gradual decrease in biasing voltage V_{bias,g_m} and $V_{bias,2}$, the gain remains constant ≈ 2 while power consumption significantly decreases. By performing simulations with a constant amplitude of $50\,mV$ and a specific frequency of $1\,kHz$, a power consumption as low as 80 nW has been obtained.

However, the current amplitude in the current-mode rectifier decreases due to the decrease in g_m, making it more sensitive to noise. In addition, for lower amplitudes, the additional M_7 transistor might be required to compensate for the initial slew rate at the beginning of the conduction of M_8. Therefore, the 80 nW gleefully announced a few lines earlier must be seen with a critical eye. It exclusively shows that this rectifier could decrease its already low power consumption at the cost of additional design efforts.

7.7 Layout implementation

The sizing proposed in Section 7.4 has been kept for the layout implementation. A compact layout was challenging to achieve because the proposed sizing contains unbalanced dimensions. Moreover, numerous transistors have to be matched. This topology has three current mirrors and two differential pairs (one of these being a doublet). The final layout was realized as a single block and is presented in Fig. 7.9. Despite the unbalanced dimensions, the area remains fairly low $\approx 1400\,\mu m^2$. The post-layout performance are compared in Section 7.8 along with reference paper and schematic performance.

7.8 Performance summary

In this section, we propose a comparison of the half-wave rectifier main performance. We compare the performance of the reference paper [71], the schematic implementation and the layout implementation. Table 7.3 shows that the proposed sizing exhibits better performance than the reference paper. Bandwidth is increased by a factor 5 while power consumption is reduced by nearly 200 nW. It should be noted that the supply voltage used in this paper is not identical to the one used for the AO chain. As discussed in Section 7.6, the power consumption could be further decreased at the expense of noise performance by tuning the g_m and g_m^{-1} simultaneously. Further works could evaluate quantitatively this performance trade-off associated with power consumption. The power consumption of the layout is slightly higher than the schematic due to the adaptation of the bias voltages to maintain a linear gain.

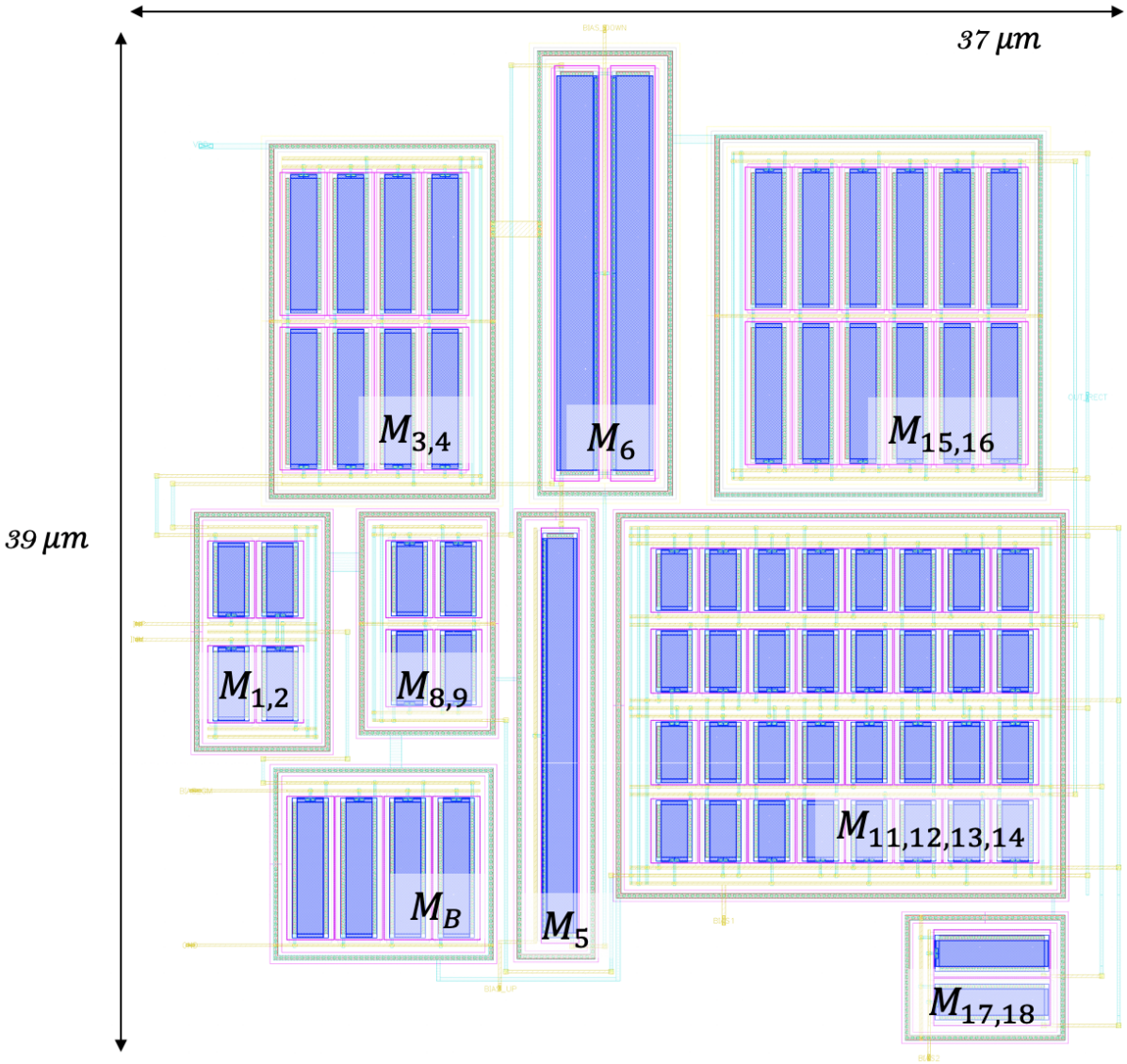


Figure 7.9: Layout implementation - Half-wave rectifier

Performance	[71]	**Proposed sizing**	Post-layout extraction
Technology	0.35μm CMOS	65nm LP CMOS	65nm LP CMOS
Gain [dB]	5.1	6	6
Maximum frequency [kHz]	200	$\approx$ 1000	$\approx$ 800
Supply voltage [V]	1	0.6	0.6
Power consumption [nW]	600	420	440
Saturation of the gain	NA	at 100 mV	at 100 mV

Table 7.3: Comparison table : Half-wave rectifier performance

7.9 Low-pass filter

To provide the comparator with a DC signal reflecting the signal energy, an LPF is required at the output of the half-wave rectifier. A simple RC passive topology seems most appropriate to prevent any power consumption overhead associated with an active LPF. The circuit topology is illustrated in Fig. 7.10. The LP corner of this passive LPF should be suited to extract the mean of the rectified signal at any frequency between 90 Hz and 16 kHz. Hence, it must be conveniently chosen. A very high value would induce large ripples on the capacitor voltage at low frequency while a low value could prevent the capacitor from charging at high frequency. An LP corner at 30 Hz offers the right compromise between low and high frequency constraints. As $f_{LP,lpf} = \frac{1}{2\pi \cdot R_{lpf} C_{lpf}}$, a possible choice for the resistor and capacitor values is $C_{lpf} = 5\,pF$ and $R_{lpf} = 1\,G\Omega$.

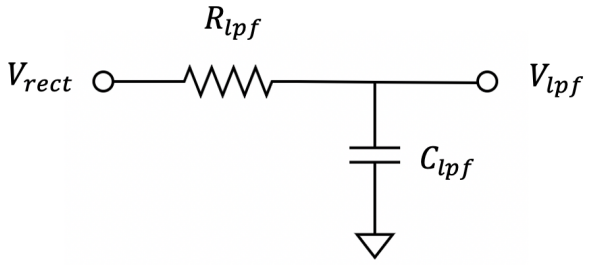


Figure 7.10: A passive low-pass filter

Given the density of MIM capacitors granted earlier in this work, the area associated with a 5 pF represents 2500 μm^2, which comparable in area to the IM OTA layout. Concerning R_{lpf}, $1\,G\Omega$ can be targeted employing an NMOS pseudo-resistor. As introduced in Section 6.3, NMOS pseudo-resistors exhibit a lower equivalent resistance value as the mobility of electrons is three times larger than the mobility of holes. This would avoid utilizing many PMOS pseudo-resistors in parallel. The sizing process for this pseudo-resistor is comparable to the one proposed in Section 6.4 and is not recalled in this section for the sake of conciseness. A typical transient simulation of the half-wave rectifier followed by the LPF is illustrated in Fig. 7.11.

For low acoustic level values, the voltage amplitude across the LPF capacitor is in the mV order of magnitude. The minimum voltage drop across the capacitor C_{pf} required to trigger the hysteresis comparator following the LPF has been fixed to 4 mV. Indeed, a smaller voltage drop points out the need for a very low hysteresis value, which constraints the sizing of the comparator (developped in the next chapter). Taking into account the half-wave rectifier response, the LNA gain and the sensitivity of the microphone, 4 mV across the LPF capacitor translates back to 57 dB_{SPL} in the acoustic domain. This value hence determines the **minimum toggle level** for the AO chain.

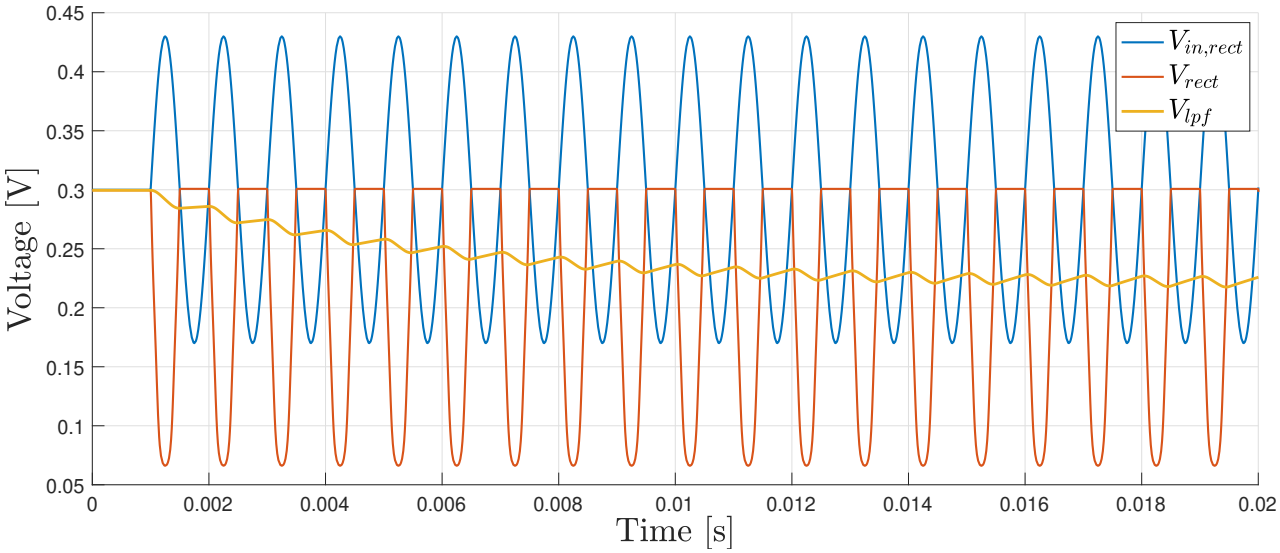


Figure 7.11: The voltage on the capacitance of the rectifier increases steadily to extract the mean of the rectified signal. An attentive reader would note that the amplitude of the input signal is slightly higher than 100 mV. This means that the rectifier signal does not strictly exhibit a 6 dB gain.

Chapter 8

Decision stage

The last stage of the AO chain is a comparator taking a decision based on the voltage on the LPF capacitor. As the output of the comparator interfaces the second stage of the sensing system, stability of the binary output signal is essential, leading to the choice of an hysteresis comparator. However, if the binary output signal were directly processed as an interrupt request (IRQ) for the microcontroller unit (MCU), hysteresis would not have been specifically required. The voltage change on the capacitor when the minimum acoustic toggle level is reached is 4 mV, pointing out the need for hysteresis of that same value.

Sections 8.1, 8.2, 8.3 deal with the main FoMs, the design of the comparator, and its working principle. Then, Section 8.4 proposes two possible sizings, among which only one of them has been layouted in Section 8.5. Finally, the performance and limitations associated with these two sizings are comprehensively discussed in Section 8.6.

8.1 Main figures of merit

Input noise

In conventional comparator architectures, input noise is critical as it may influence the binary output signal stability. Hysteresis comparators are specifically designed to exhibit robustness against noise. In addition, design efforts have been made to decrease both thermal and flicker noise. The flicker noise from the LNA has been minimized thanks to GA optimization, while a passive low-pass filter precedes the hysteresis comparator featuring thermal noise reduction. The RMS voltage noise at the output of the LPF has been estimated to 3.53 μV_{rms} employing a transient noise analysis. The IRN of the comparator has also been calculated in the same way as in Section 5.1and is given by 9.6 μV_{rms}. Both quantities are nearly three orders of magnitude below the target hysteresis of 4 mV, hence the noise level is considered negligible at the input node of the comparator.

Input offset

The offset at the input of a comparator is inherently due to the mismatch of the differential pair and plays a crucial role in the comparator performance. Indeed, a voltage offset that

is present at the comparator input induces a biased toggle level. In most cases, the input-referred offset is systematic. Hence, many compensations techniques have been developed throughout the literature to cope with it. In an hysteresis comparator, the offset manifests as a shift of the hysteresis curve along with the V_{in} (input of the comparator). Denoting the hysteresis as V_{hyst}, we illustrate the impact of an offset in Fig. 8.1 for an hysteresis comparator.

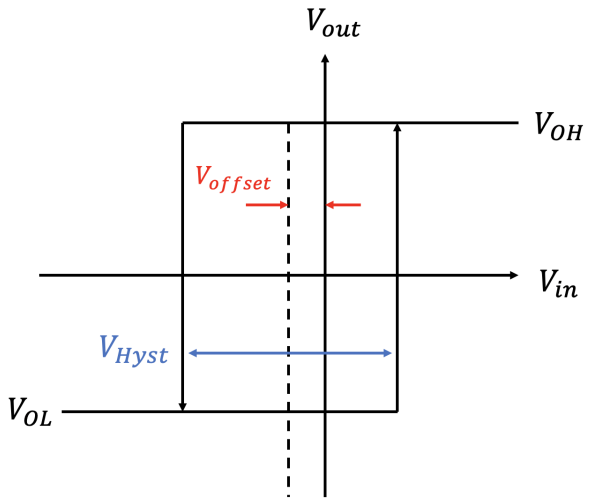


Figure 8.1: Influence of an offset on an hysteresis comparator.

Transition time

This metric is associated with the speed of the comparator. It is defined as the time interval between the moment when the input voltage exceeds V_{TRP}^{+} (rising transition time) or V_{TRM}^{-} (falling transition time) and the moment when the output voltage effectively reaches $V_{DD}/2$. In this low-frequency application, transition time should not raise a particular issue as long as it remains in the μs order so that no delay is accumulated when waking up the rest of the sensor.

8.2 Design choice

This chapter was introduced by pointing out the need for a hysteresis comparator that exhibits robustness against input noise and ripples. This is a strong requirement for the search in state-of-the-art papers. Secondly, to avoid additional power overhead linked to clock signal generation, a non-clocked comparator has been chosen for the AO chain.

These two simple statements narrow the field of possibilities to continuous time comparators that exhibit hysteresis properties. The hysteresis can either be external through an external feedback loop or internal, thanks to cross-coupled transistors. The next two subsections discuss the external and internal hysteresis comparator architectures.

External hysteresis comparator

The most straightforward way to implement an hysteresis comparator is certainly by applying positive feedback to a simple amplifier as represented in Fig. 8.2. Note that the pull-up resistance R_p at the output is represented since most of comparators designs have open-drain outputs [72]. When V_{in} is low, the output is at a high level. Hence, R_{fb} is in parallel with R_1 inducing a comparison voltage higher than $V_{DD}/2$ at the positive input terminal of the comparator. When this reference voltage is exceeded, the output is set to a low level and R_{fb} is now in parallel with R_2 inducing a comparison voltage lower than $V_{DD}/2$ [73]. Trip points are given by

$$V_{TRP}^{+} = V_{DD} \cdot \frac{R_2}{R_2 + R_1||(R_p + R_{fb})} \tag{8.1}$$

and

$$V_{TRM}^{-} = V_{DD} \cdot \frac{(R_2||R_{fb})}{(R_2||R_{fb}) + R1} \,. \tag{8.2}$$

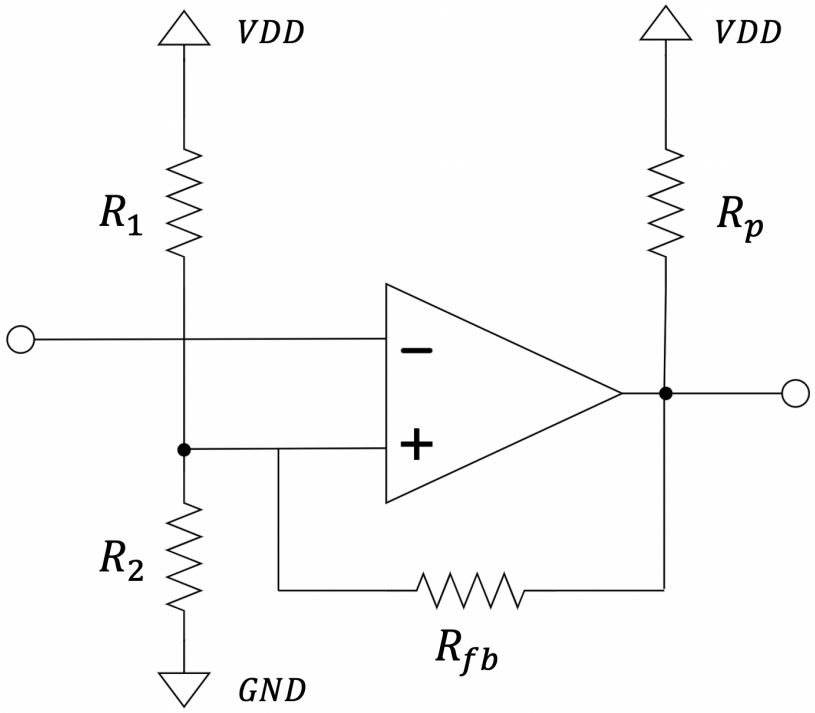


Figure 8.2: An external hysteresis comparator is achieved through a positive resistive feedback.

Internal hysteresis comparator

The main disadvantage associated with a comparator with external hysteresis is the presence of resistors. For instance, if R_1 and R_2 are not sufficiently high, the current flowing into this branch will be higher, deteriorating power consumption. If R_1 and R_2 need to be sufficiently high, this will lead to area overhead or a pseudo-resistor implementations, which, as seen in Chapter 6, are sensitive to PVT variation and statistical variability. In addition, large external resistors inevitably add noise on the reference voltage or on the signal path, which is undesirable.

Accordingly, an internal hysteresis comparator design is better suited for on-chip designs. The most prevalent design for implementing such a comparator is illustrated in Fig. 8.3 [49]. This comparator architecture presents a low complexity. Indeed, we can distinguish a classical OTA design with a class AB output stage to which only a cross-coupled feedback has been added (M_6 and M_7). The proper operating principle has already been obtained with a 90nm CMOS technology in [74] but targeting higher power consumption (in that case 2.09 mW).

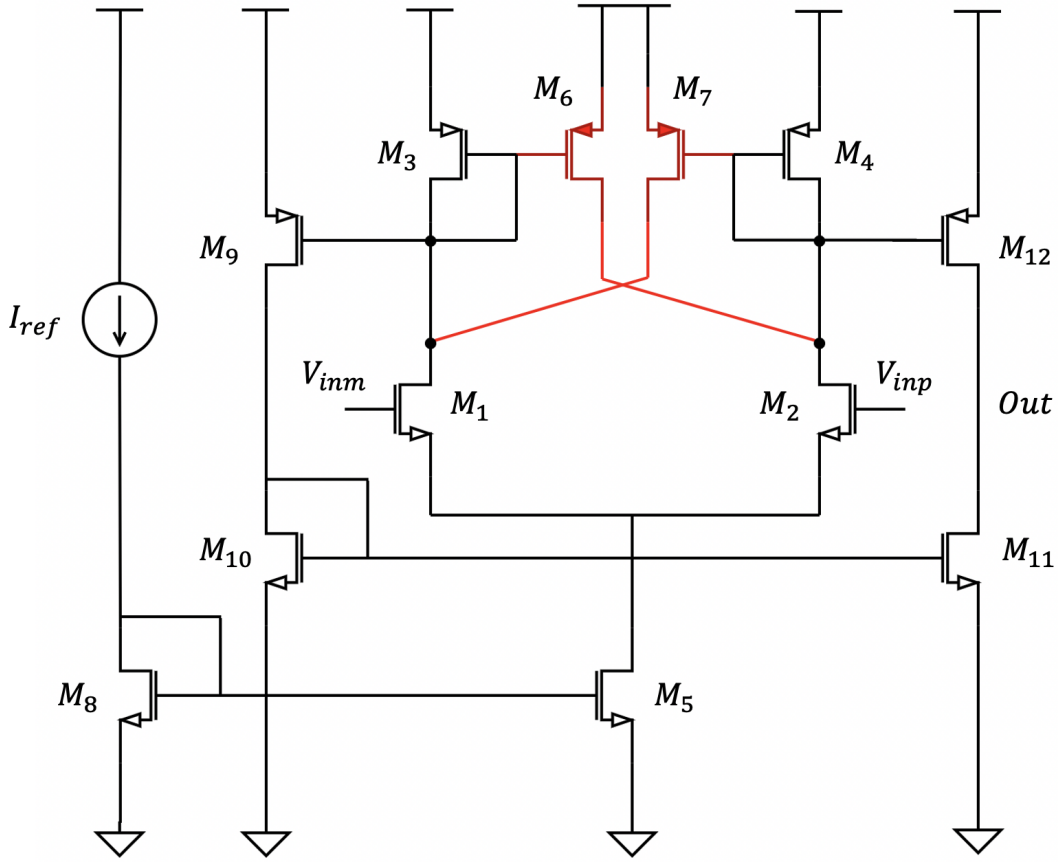


Figure 8.3: An internal hysteresis comparator is obtained by the addition of a cross-coupled feedback to a conventional OTA. The cross-coupled feedback in highlighted in red.

8.3 Working principle

This section highlights the key elements of the topology presented in Fig. 8.3.

1. **Conventional OTA topology** : Disregarding the cross-coupled feedback, one distinguishes an OTA with a simple differential stage and an class AB output stage.

    - **The biasing current mirror** made of M_5 and M_8 provides the differential pair with a constant bias current equal to the reference current I_{ref}.
    - **The differential pair** consists of transistors M_1 and M_2. The gate of M_2 is the positive input terminal as a voltage increase at this node induces an increase in current $I_{DS,4}$. This current is then mirrored in M_{12} which charges the load capacitor, increasing the output voltage.
    - **The output stage** is formed by transistors M_{11} and M_{12}. These allow a better voltage swing than the simple differential stage and provide a class AB type of driving capability.

2. **Feedback paths**

    - **The negative feedback path** is a current-series feedback through the common-source node of M_1 and M_2.
    - **The positive feedback path** is a voltage-shunt feedback trough gate-to-drain connections of M_6 and M_7 [49].

It is worth mentioning that presence or absence of hysteresis is defined by the ratio between the positive and negative feedback paths $\frac{\beta_6}{\beta_3} = \frac{\beta_7}{\beta_4}$. If this ratio is less than unity, there will be no hysteresis occurring. Conversely, hysteresis will occur if the ratio is above unity. Determining how the trip points evolve with the other parameters is central to the design of the comparator and is discussed in the following subsection.

Trip points evaluation - Mathematical model

In this section, a mathematical model is studied to determine the trip points V_{TRP}^{+} and V_{TRM}^{-} of the comparator. As $V_{TRP}^{+} = -V_{TRM}^{-}$, we can focus on the positive trip point alone. The literature only provides the position of these trip points when the comparator is operating in the strong inversion regime [49] which is not the case in this work as transistors operate in weak inversion. The method developed below is not inspired by any papers and will be thoroughly discussed.

Let us first consider that the positive and negative rails are respectively V_{DD} and 0, that the gate of M_1 is tied to $\frac{V_{DD}}{2}$ and the gate of M_2 is well below $\frac{V_{DD}}{2}$. We thus have M_1 conducting and M_2 blocking. At this point $I_{DS,1} = I_{DS,5}$. The current that M_6 is trying to source is equivalent to

$$I_{DS,6} = \frac{(W/L)_6}{(W/L)_3} \cdot I_{DS,1} = \frac{(W/L)_6}{(W/L)_3} \cdot I_{DS,5} \,. \tag{8.3}$$

If the gate voltage of M2 steadily increases, a small amount of the current $I_{DS,5}$ will begin to flow in the source of M2. When the total current in M2 is equal to $I_{DS,6}$, the comparator will switch state. Therefore we must evaluate the point where $I_{DS,2} = I_{DS,6}$ to determine the trip point. At as result, we have

$$I_{DS,5} = I_{DS,1} + I_{DS,2} \qquad \text{and} \qquad I_{DS,2} = I_{DS,6}\,, \tag{8.4}$$

which implies from Eq. 8.3

$$I_{DS,1} = I_{DS,5} - I_{DS,2} = I_{DS,5} - \frac{(W/L)_6}{(W/L)_3} \cdot I_{DS,1}\,. \tag{8.5}$$

Finally, by rearranging terms we obtain

$$I_{DS,1} = I_{DS,3} = \frac{I_{DS,5}}{1 + \frac{(W/L)_6}{(W/L)_3}}\,. \tag{8.6}$$

Now, we need to substitute these current values into the expression of V_{TRP}^{+} given as

$$V_{TRP}^{+} = V_{GS,2} - V_{GS,1}\,. \tag{8.7}$$

By making the assumption that M_1 and M_2 operate in saturation in weak inversion ($V_{DS} > 100$ mV at ambient temperature), we use Eq. 2.1 to write the gate-to-source voltage as

$$V_{GS} = nU_T \cdot \log\left(\frac{I_{DS}}{I_S \cdot (\frac{W}{L})}\right) + V_{th}\,, \tag{8.8}$$

with log representing the natural logarithm. Assuming identical threshold voltages V_{th}, characteristic currents I_S and a same aspect ratio for the transistors of the differential pair, we can develop Eq. 8.7 as

$$\begin{aligned} V_{TRP}^{+} &= nU_T \log\left(\frac{I_{DS,2}}{I_{DS,1}}\right) \\ &= nU_T \log\left(\frac{I_{DS,5} - I_{DS,1}}{I_{DS,1}}\right) \\ &= nU_T \log\left(\frac{I_{DS,5} - \frac{I_{DS,5}}{1+(\beta_6/\beta_3)}}{\frac{I_{DS,5}}{1+(\beta_6/\beta_3)}}\right) \\ &= nU_T \log\left(\frac{\beta_6}{\beta_3}\right)\,. \end{aligned} \tag{8.9}$$

The result of Eq. 8.6 has been used in the second line of this mathematical development. As the g_m/I_D versus normalized current characteristic exhibits a constant plateau in weak inversion as

$$\left(\frac{g_m}{I_D}\right)\Bigg|_{max} = \frac{1}{n \cdot U_T} \qquad \left[\frac{\mathrm{S}}{\mathrm{A}}\right]\,, \tag{8.10}$$

the $n = 1.2$ value has been evaluated through the technological curves of the transistors.

Discussion of mathematical model validity

The central result from Eq. 8.9 theoretically means that the hysteresis value does not depend on the bias current. Nevertheless, as shown in Fig. 8.4 that illustrates the variation of V_{TRP}^{+} for distinct β_6/β_3 ratios at $I_{ref} = 50\,nA$, we observe that the mathematical model does not match the simulations results. Simulations have shown that the hysteresis varies slightly with other biasing currents.

Even if the mathematical model catch the overall tendency of the simulated curve (logarithmic behavior), we state a discrepancy. We hypothesize that the discrepancy in V_{TRP}^{+} value rely on the misguiding weak inversion assumption. A g_m/I_D value equal to $28\,\frac{S}{A}$ (design choice proposed in the next subsection) is not strictly situated on the weak inversion plateau if we consider the transistors technological curves presented in Fig. 5.4. Therefore the validity of the mathematical model is questionable as the main assumption relies on the fact that transistors operate in weak inversion. To be more accurate in predicting the hysteresis, a LUT based on Spice simulations was build for a fixed reference current value.

8.4 Sizing of the comparator

Initial sizing

This section aims to obtain an operating topology that exhibits a proper working principle as it will be further tuned in the next section. Unlike the improved Miller OTA, which operates in a closed-loop configuration, the comparator operates in an open-loop configuration. Consequently, evaluating the frequency response or stability is not relevant. In other words, the comparator would be unstable in a closed-loop configuration. This might be undesirable using analog compensation technique such as autozeroing, which is not the case in this work.

As a design choice, the Matlab template used for the sizing fixes the same $g_m/I_D = 28$ for all transistors. This value was chosen as a higher value quickly results in extensive widths for the transistors. The reference current is set to $I_{ref} = 50\,nA$, targeting low power consumption. The LUT mentioned is Section 8.3 is built for this same reference current value. Also, transistors lengths are fixed to feature a straightforward design process. Moreover, we set the width ratio between transistors $M_{9,12}$ and $M_{3,4}$, called here γ, to unity for the sake of power consumption. $\frac{\beta_6}{\beta_3}$ ratio is 1,19 based on the LUT in Fig. 8.4 to ensure $V_{TRP}^{+} = 2$ mV, thus 4-mV hysteresis. A log-log plot has been selected to better highlights the discrepancy between the mathematical model from Eq. 8.9 and the LUT build thanks to Spice simulations. All designs choices are summarized in Table 8.1, associated transistors dimensions are presented in Table 8.2.

For a fixed voltage of $V_{DD}/2$ at the negative input terminal and progressively sweeping a DC voltage at the positive input terminal, the comparator transits from a low state to high state at $V_{TRP}^{+} = 2.1$ mV, yielding $V_{hyst} = 4.2$ mV as shown in Fig. 8.5. Evaluated quiescent power with Spice simulations yields 53 nW.

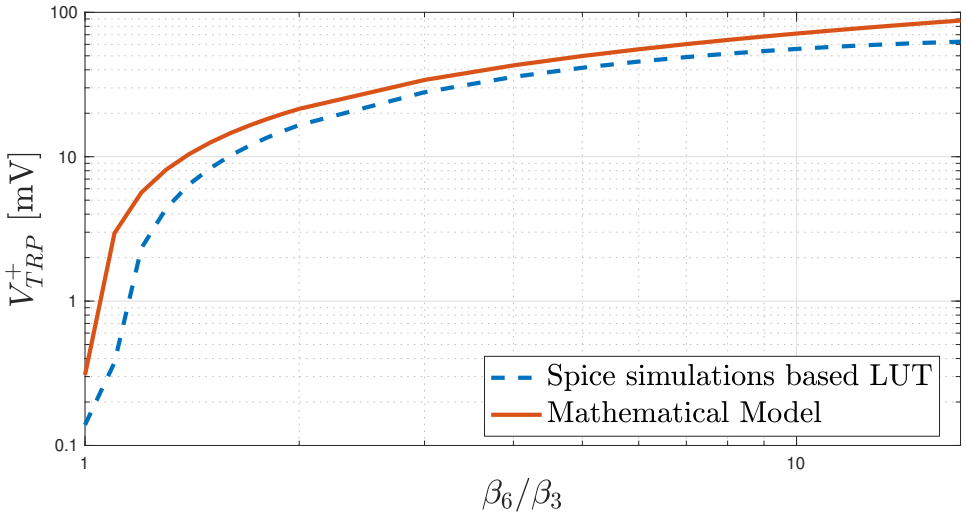


Figure 8.4: An illustration of the discrepancy between the mathematical model from Eq. 8.9 and the LUT extracted with Spice simulations (I_{ref} = 50 nA).

Parameters	**Values**
I_{ref}	50 nA
L_{all}	5 μm
$(g_m/I_D)_{all}$	28 $\frac{S}{A}$
(β_6/β_3)	1.19
γ	1

Table 8.1: Design choices for the hysteresis comparator - Initial sizing

Stage	**Transistors**	**Aspect ratio** ($\mu m/\mu m$)
Bias stage	M8, M5	22.5/5
Differential stage	M1, M2	11.2/5
	M3, M4	11.7/5
Positive feedback	M6, M7	13.9/5
Class AB output stage	M8, M9	11.7/5
	M10, M11	11/5

Table 8.2: Transistors dimensions - Initial sizing

Fined-tuned sizing

The initial sizing presents stunning performance, showing the expected hysteresis value and low quiescent power consumption compared to the earlier blocks in the AO chain. The remaining steps consist in accessing the comparator performance robustness to PVT corners and statistical variability. The fine-tuned sizing primarily focuses on robustness to PVT corners, while statistical variability will be reviewed in Section 8.6.

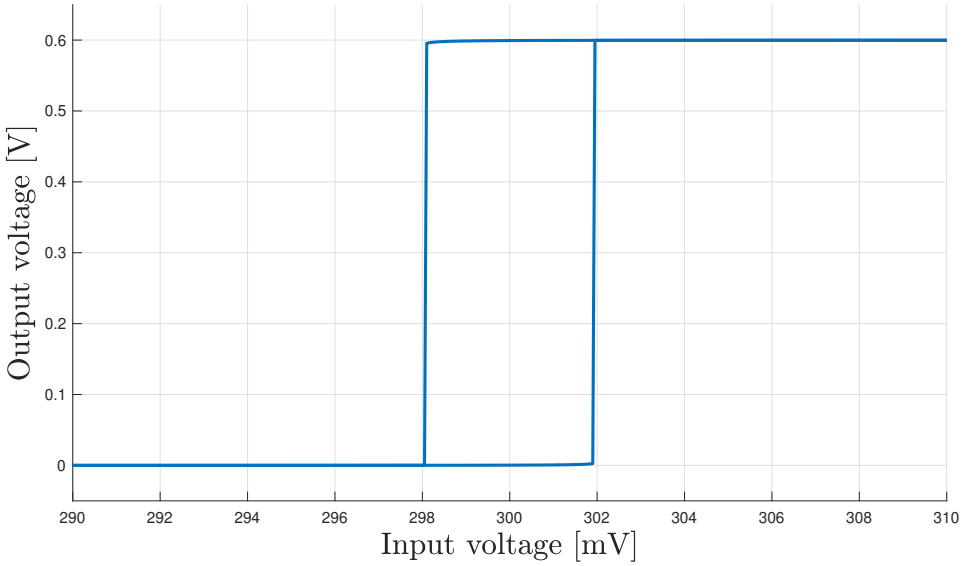


Figure 8.5: Hysteresis curve of the comparator - Initial sizing

Unfortunately, the initial sizing simulations have shown that the hysteresis phenomenon does not occur for FF and SF corners at 85°C, which is not an acceptable performance. This failure is inherently linked with the $\frac{\beta_6}{\beta_3}$ ratio, which goes below unity. The reason for this outcome is the loss of saturation on transistor M_3 as its drain-to-source voltage does not exceed $V_{dsat,85°C} = 123\,mV$. To cope with the issue, more voltage headroom is required for transistors $M_{3,4}$. This increase in voltage headroom can be achieved by decreasing their widths values $W_{3,4}$. With a constant length, this means biasing these transistors more in moderate inversion. In addition, the decrease in $W_{3,4}$ needs to be accompanied by a reduction in the output stage transistors widths to avoid an increase in current consumption, and thus power consumption. The fine-tuning indicates that decreasing $W_{3,4}$ by a factor ≈ 4 along with a decrease of $W_{9,12}$ by a factor ≈ 2 allows the hysteresis phenomenon to reappear in the problematic corners. Fine-tuned sizing is presented in Table 8.3, quiescent power consumption is 66 nW.

Stage	**Transistors**	**Aspect ratio** ($\mu m/\mu m$)
Bias stage	M8, M5	22/5
Differential stage	M1, M2	11/5
	M3, M4	2.5/5
Positive feedback	M6, M7	2.975/5
Class AB output stage	M8, M9	5/5
	M10, M11	5/5

Table 8.3: Transistors dimensions - Fine tuning

8.5 Layout implementation

The fine-tuned comparator layout implementation has been realized and is presented in Fig. 8.6. As $M_{3,4}$ and $M_{6,7}$ play an essential role in the hysteresis, a common centroid organization has been set for all the PMOS transistors in this topology. A common centroid organization has also been realized for transistors $M_{1,2}$ and $M_{10,11}$. This block proved to be straightforward to implement in layout. The quiescent power consumption is $67.2\,nW$, consistent with schematic simulations. However, a 1-mV decrease of the hysteresis led to a value of 3 mV, which is below the expected value. We make the assumption that this discrepancy is linked with well proximity effects. Indeed, transistors close to the well edge have different performance (due to a modified V_{th}) than the transistors placed in the center of the layout [75]. Dummies could therefore be added to cope for the issue. A comparison between the schematic performance and the layout implementation is proposed in Section 8.6.

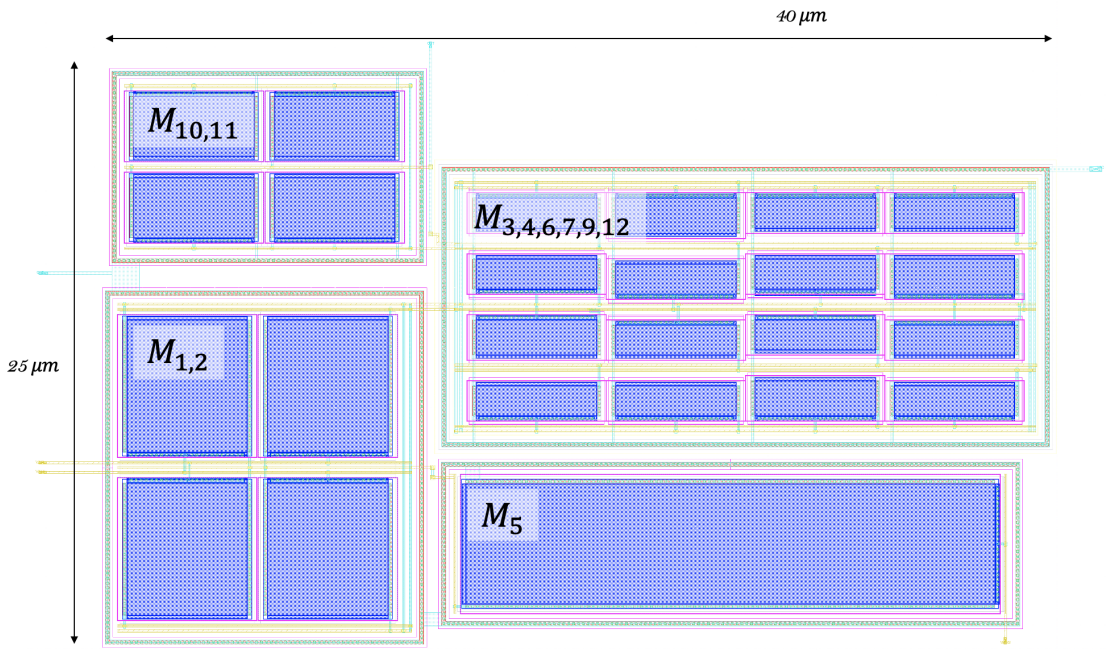


Figure 8.6: Layout implementation - Hysteresis comparator

8.6 Further discussions and main limitations

To close this chapter, we have seen that the limited validity of the trip points mathematical model led to a LUT-based sizing. This sizing allows the comparator to target the expected hysteresis value of $4\,mV$. In addition, since there is no particular bandwidth or gain constraints on the comparator, low power can be achieved. Indeed, when compared to other blocks of the AO chain, the comparator quiescent power consumption is about an order of magnitude below.

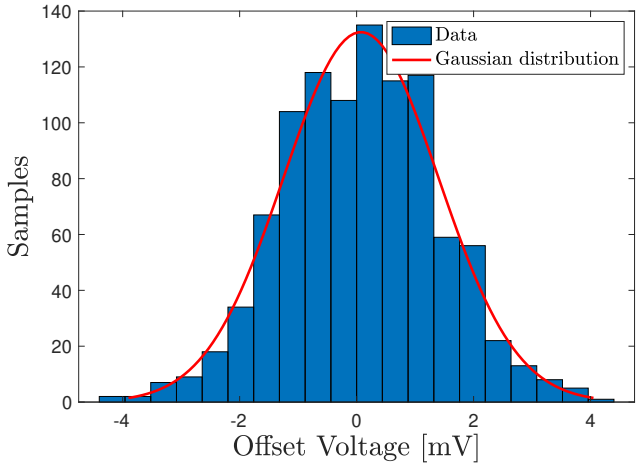
An evaluation of the PVT corners performance typically showed that the initial sizing is not robust to specific corners at 85°C. To overcome this problem, a reduction in the width of the critical transistors involved in hysteresis has been chosen. Nevertheless, this design choice highlights a new trade-off between robustness to PVT variations and statistical variability. Reducing the dimensions of the transistors involved in the hysteresis phenomenon yields a topology that is less robust to statistical variability, resulting in a larger hysteresis variation when running Monte-Carlo simulations ($N_{runs} = 1000$).

The offset and hysteresis variations for the initial and fine-tuned design are presented in Fig. 8.7. Referring to the interpolated Gaussian curves of the hysteresis as $V_{hyst} \sim \mathcal{N}(\mu, \sigma)$, the initial sizing shows $V_{hyst,initial} \sim \mathcal{N}(4.1\,mV, 0.56\,mV)$ while the fine-tuned sizing shows $V_{hyst,tuned} \sim \mathcal{N}(3.9\,mV, 1.2\,mV)$. For a nearly identical mean value, the standard deviation is about two times larger for the fine-tuned design. This trade-off is to be evaluated carefully if the specifications of the AO chain have to be revised afterwards. It is essential to note that decreasing in $W_{3,4}$ is certainly not a unique design solution. A first potential solution consisting in increasing $W_{1,2}$ was investigated but did not yield promising results as the drain of M_1 is not only shared by the transistor M_3 but also, via the cross-coupled pair, to the drain of M_7. A second solution could be to increase the dimensions of $L_{3,4}$ in order to increase the drain-to-source voltage of $M_{3,4}$.

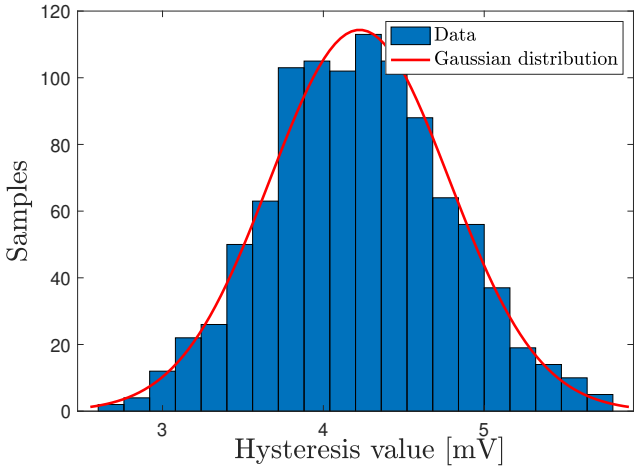
The initial sizing, the fine-tuned sizing, and the post layout performance are summarized in Table 8.4. Transition time and gain values are presented to assess that these metrics do not raise any issues in the comparator design. Indeed, the gain is sufficiently high while the transition time sufficiently low.

Performance	Initial sizing	Fine tuning	Post-layout
Power consumption [nW]	53.1	66	67.2
Hysteresis value (μ, σ)	$\mathcal{N}(4.2\,mV, 0.56\,mV)$	$\mathcal{N}(3.9\,mV, 1.2\,mV)$	$\mathcal{N}(2.7\,mV, 1.1\,mV)$
Input offset (3σ) [mV]	4	5.5	5.8
Rising transition time [μs]	11.7	4.8	5.65
Gain [dB]	57.2	59.3	61.7

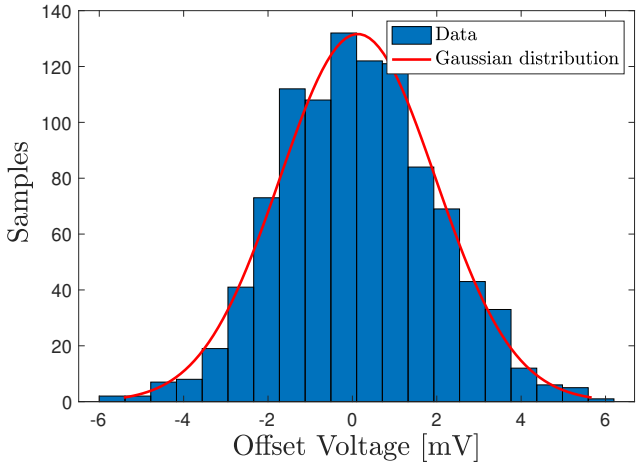
Table 8.4: Internal hysteresis comparator - Performance comparison



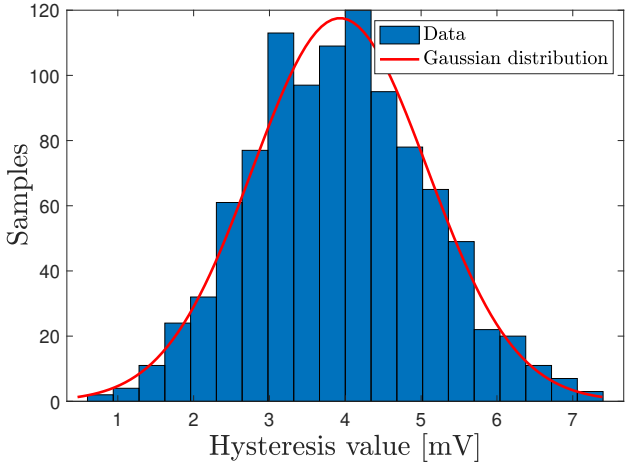
(a) Initial sizing - Offset distribution



(b) Initial sizing - Hysteresis distribution



(c) Fine-tuned sizing - Offset distribution



(d) Fine-tuned sizing - Hysteresis distribution

Figure 8.7: Statistical variability of the offset and hysteresis values for the initial and fine-tuned sizings. The hysteresis is computed as the difference between V_{TRP}^{+} and V_{TRP}^{-} while the offset has been determined following its definition in Fig. 8.1.

Chapter 9

The always-on chain

This chapter aims to assess the performance of the AO chain when gathering the distinct circuits proposed in the previous chapters.

In Section 9.1 a summary of the main performance for each circuits and an evaluation of the total power consumption are proposed. Section 9.2 aims at evaluating the performance of the chain through a worst-case amplitude scenario using a transient noise simulation and proposes a study of the distinct background noise levels. Section 9.3 compares the performance of the AO chain with state-of-the-art papers. Finally, Sections 9.4 and 9.5 respectively present the possible improvements for the AO chain and a critical analysis of its positive and negative points through a SWOT analysis.

9.1 Summary of the always-on chain performance

Figure 9.1 illustrates the main blocks of the AO chain developed throughout this work to clarify the TLD architecture presented in Fig. 2.1. The main connections are depicted for a proper understanding. A summary of the main performance for each circuit is provided in Table 9.1. Only the fine-tuned schematics performance are recalled for the sake of clarity.

The total power consumption is given by the sum of each individual power consumption as

$$P_{AO\,chain} = 530\,nW + 420\,nW + 66\,nW = 1.016\,\mu W \approx 1\,\mu W\ . \tag{9.1}$$

The total power consumption almost respect the initial power consumption requirement: $P_{AO\,chain} < 1\,\mu W$. We note that the actual LNA power consumption is lower than the one predicted by the genetic algorithm, which explains the 50 nW discrepancy between the value presented in Table 9.1 and the one in Table 5.8. From Table 9.1, we build Table 9.2 which provides a summary of the AO chain main performance. As a reminder, the minimum level of detection is determined by the input-referred noise of the LNA, while the minimum toggle level depends on the hysteresis value of the comparator, which justifies the 20 dB difference between these values.

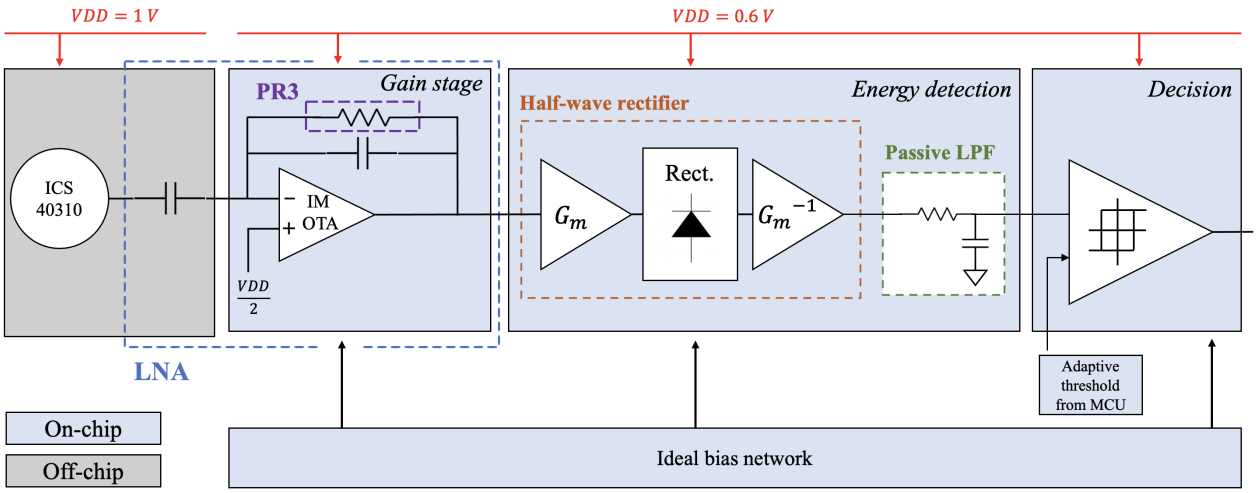


Figure 9.1: Detailed architecture of the always-on chain highlighting the design choices for each circuit. The grey and blue area respectively correspond to off-chip circuit elements and on-chip circuit elements.

Always-on chain	Main performance	Power consumption
LNA	$A_{v,LNA} = 30\,dB$ $f_{HP,LNA} = 25\,Hz$, $f_{LP,LNA} = 17.8\,kHz$ $IRN = 20\,\mu V_{rms}$	530 nW
Half-wave rectifier	$A_{v,Rect} = 6\,dB$ Saturation at $V_{in,rect} = 100\,mV$	420 nW
Low-pass filter	$f_{LP,lpf} = 30\,Hz$	0 nW
Hysteresis comparator	$V_{hyst} \sim \mathcal{N}(3.9\,mV,\, 1.2\,mV)$ $3\sigma_{offset} = 5.5\,mV$ $T_{Rising} = 4.8\mu s$	66 nW

Table 9.1: Summary table of the main performance of each circuit in the always-on chain. We state that the power consumption is mostly dominated by the two first circuits. In addition, the IRN of the LNA is slightly higher than the IRN of the main OTA due to the contribution of the pseudo-resistance to input noise. This contribution is nevertheless meager.

Performance	Value
Power consumption	1.016 μW
Minimum level of detection	37 dB_{SPL}
Minimum toggle level	57 dB_{SPL}
Bandwidth	90 Hz - 16 kHz

Table 9.2: Main performance of the always-on chain

9.2 Verification of the noise performance of the design

A transient noise simulation consists in generating noise sources in the time domain [76]. In the context of this work, a transient noise simulation has been used to verify that the noise generated by each element in the chain does not bias the minimum toggle level. Hence, we realized a transient noise analysis for a sound pressure level of 57 dB_{SPL} at 1 kHz and ambient temperature. Concerning transient noise simulations, an acceptable practice consists in defining the minimum and maximum frequencies as $f_{min} = \frac{1}{T_{sim}}$ where T_{sim} represents the simulation time, and $f_{max} = 10 \cdot f_T$ [77]. In this simulation, the microphone is seen as a black box outputting a pure 1 kHz sinusoidal wave with $V_{peak-to-peak} = 560\,\mu V$ (corresponding to 57 dB_{SPL}) centered around a DC level of 500 mV, determined by the ICS-40310 datasheet. Simulations results are presented in Fig. 9.2.

We state a 7-mV offset voltage between the output voltage of the rectifier and the output voltage of the low-pass filter. This offset is due to the gate leakage current of the differential pair of the comparator. The gate leakage current value is 7 pA. If we multiply this value by the LPF resistance (1 $G\Omega$), we find 7 mV indeed. This offset is typically systematic and independent from the signal amplitude or frequency. However, it varies with statistical variability simulations. We also state that the binary signal at the output of the comparator remains stable despite the ripples on the low-pass filter output voltage thanks to hysteresis. In this simulation, the total power consumption is evaluated to 1.02 μW by Eldo, which is close to the result of Eq. 9.1. We want to stress that this simulation corresponds to a worst-case scenario as the acoustic wave amplitude is low. For instance, 57 dB_{SPL} corresponds to a quiet conversational speech [25]. At a higher sound level, the electrical noise is barely visible.

To feature a context-aware sensor to background noise, distinct comparison voltages for the comparator have been identified. The distinct toggle levels in the acoustic domain and their corresponding comparison voltage are summarized in Table 9.3. To have a better understanding of the distinct toggle levels, let us consider a practical example. Under weather conditions involving a low background noise of 40 dB_{SPL} (light wind and leaf rustling), the toggle level is set to 57 dB_{SPL}. Thus, the AO chain enables the second stage of the sensing system if a bird sings at most 15 meters away from the sensor. Under weather conditions involving a high background noise of 60 dB_{SPL} (rain and/or moderate wind), the toggle level is set to 65 dB_{SPL} and only a bird 5 meters away from the sensor can be detected. Indeed, the bird singing 15 meters away from the sensor falls below the background noise.

Level	**Acoustic level**	**Corresponding sound in forests**	$\mathbf{V_{inp,comp}}$
Minimum toggle level	57 dB	bird songs (15 meters away)	291 mV
Moderate toggle level	65 dB	bird songs (5 meters away)	283 mV
High toggle level	75 dB	bird songs (2 meters away)	270 mV

Table 9.3: Distinct acoustic toggle levels and their corresponding comparison voltage for the comparator. The acoustic toggle level is associated with a corresponding bird song at a given distance.

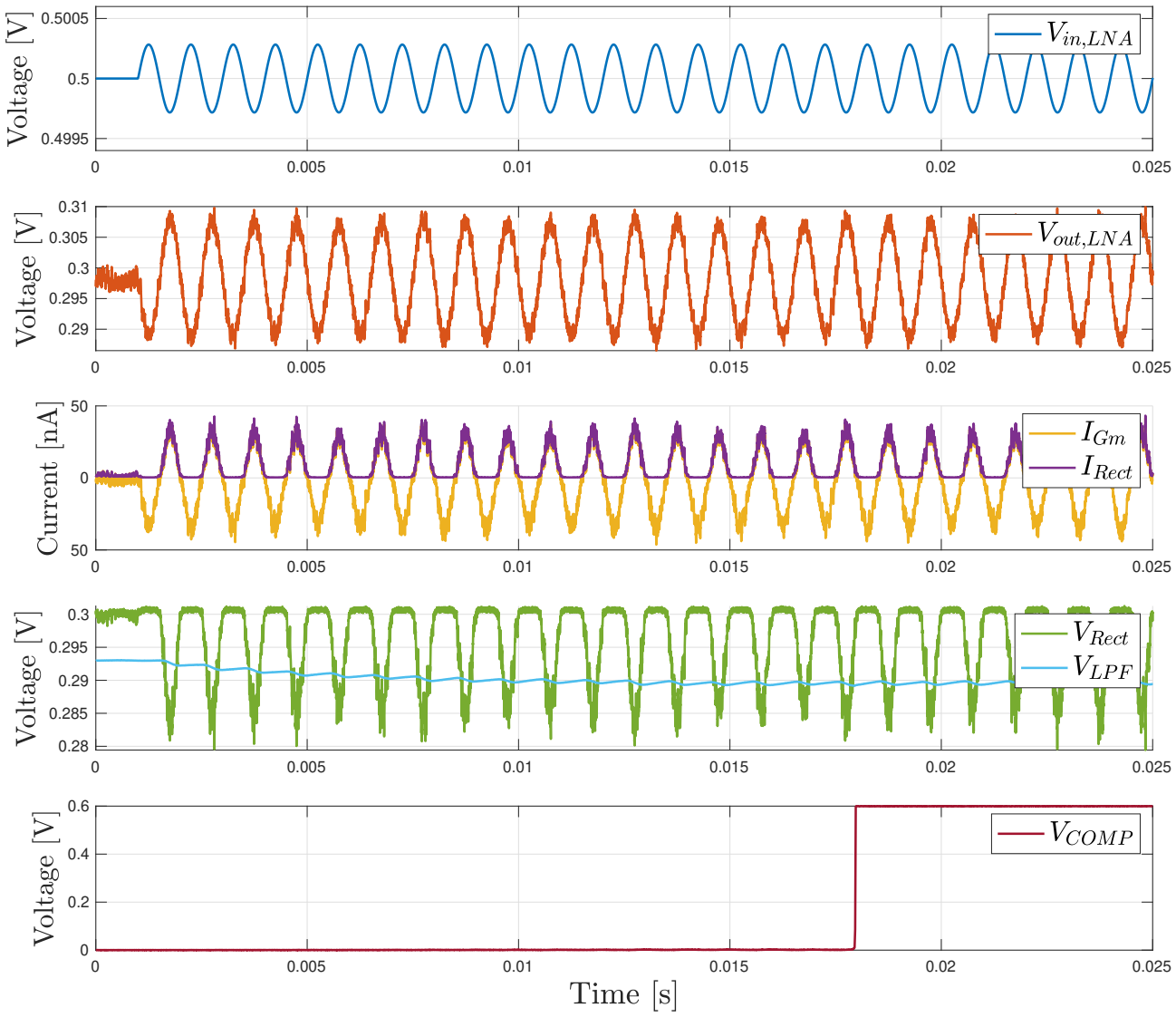


Figure 9.2: Comprehensive transient noise simulation of the always-on chain. The signal from the microphone is amplified by the 30 dB gain of the LNA. Afterward, this signal is rectified with 6 dB gain, and the mean value is extracted thanks to the passive low-pass filter. When this mean value exceeds the comparison voltage, the comparator toggles.

9.3 Comparison with current state-of-the-art papers

Figure 9.3 provides a meaningful comparison with state-of-the-art papers in the field of VAD systems and audio sensors according to a power-bandwidth trade-off. The previous AFE design for the acoustic monitoring in forest project [34] is also included to illustrate the successful contribution of this work. Only the power consumption values of the AFE are considered to fulfill a relevant comparison. This means excluding the microphone power consumption and features extractors for the state-of-the-art papers and the microphone power consumption for this work. We can state that the most recent VAD systems achieve lower power consumption but do not exceed a 5 kHz bandwidth. Interestingly, we distinguish a Pareto front highlighted in green in the optimization direction (red arrows). The proposed architecture for the AO chain aligns with state-of-the-art papers considering the higher target bandwidth. The yellow arrow highlights the contribution of this work with respect to [34]. The AFE power consumption in this latter work is 445,8 μW while a power consumption of 1.02 μW has been obtained in this work. The power consumption has thus been reduced by a factor of **437**. To conclude the comparison, IRN values of state-of-the-art VAD systems papers have been compared to this work in Fig. 9.4. The results from this work also align with state-of-the-art papers concerning the IRN. We should bear in mind that the IRN presented for the following papers: M. Yang [13], M. Cho [14], and S. Jeong [15] refers to a minimal IRN as these architectures offer a variable gain for the AFE and thus an adjustable IRN.

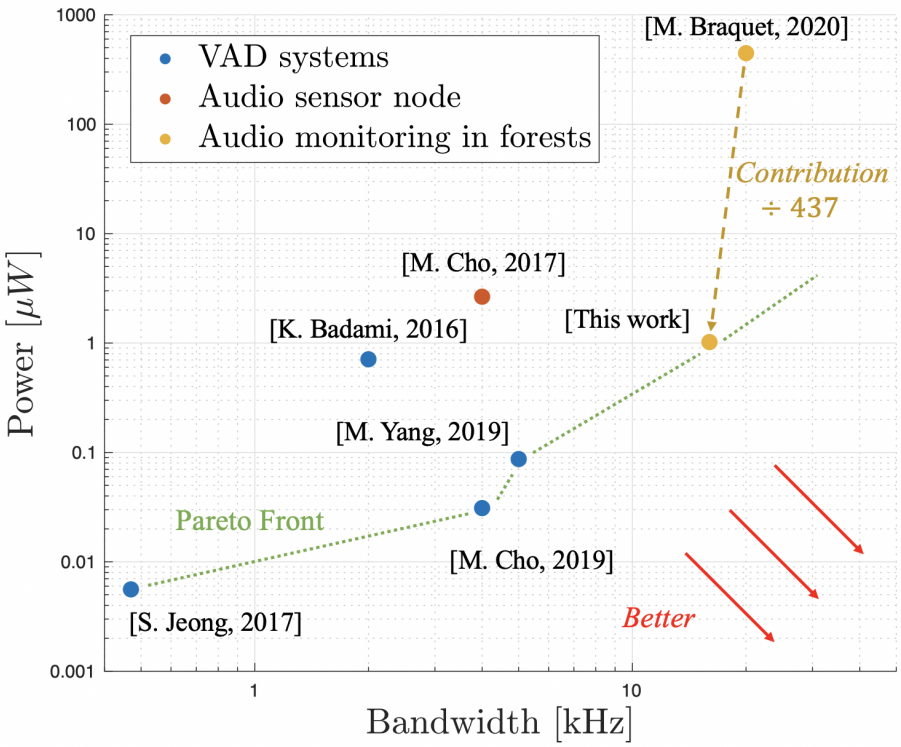


Figure 9.3: Comparison between the always-on chain performance and other audio sensing systems. The obtained performance align with state-of-the-art VAD systems considering the higher target bandwidth in this application. It is substantial to note that the *better* direction is more a general consideration rather than an real objective for all audio sensing systems. It is used here for the sake of comparison.

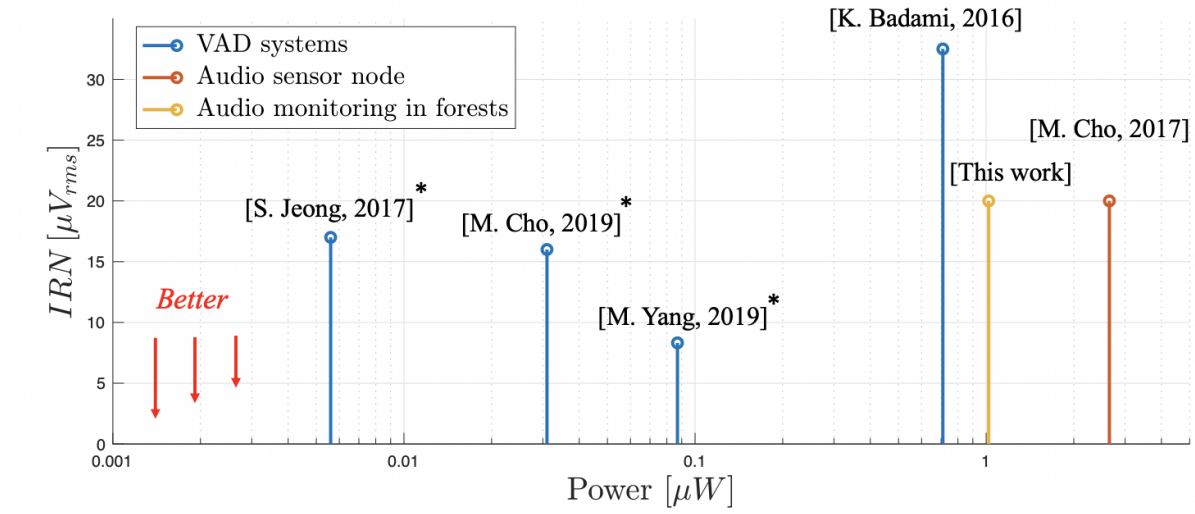


Figure 9.4: Comparison between the always-on chain performance and other audio sensing systems - IRN. The * sign indicates the AFE architectures in these papers are using programmable gain and thus adjustable IRN.

9.4 Improvement perspectives

Remaining challenges

First, an improvement for the AO chain would be to validate its performance through statistical variability simulations and in each PVT corner. Given the current AO chain architecture, the main limiting circuit element is the pseudo-resistance due to its exacerbated sensitivity to PVT corners. It is necessary to implement the trimming solution mentioned in Section 6.5 and evaluate if it allows good tunability on the resistance value without adding significant power overhead nor area overhead. If this proposed solution is insufficient, it will be appropriate to resort to another implementation for the feedback resistor in the LNA. The SAFR proposed in [61] represents a potential candidate as it provides improved robustness to temperature variations at the expense of 60 nW additional power consumption. With the SAFR, the resistance variation with temperature decreases by 226 with respect to conventional pseudo-resistors. It is worth mentioning that the papers compared in Section 9.3 also adopt a pseudo-resistor for the low HP corner implementation but do not mention its impact on their final design performance concerning temperature variations.

Second, to ensure a stable binary signal at the comparator output, it is crucial to solving the issue associated with the hysteresis variation. Currently, the fine-tuned design of the comparator has a standard deviation of 1.2 mV, which is not acceptable given the average value of the hysteresis at 4 mV. As the comparator architecture seems well suited to implement the decision stage, a new sizing should be considered to reduce the standard deviation of the hysteresis by at least one order of magnitude while maintaining robustness to PVT corners. Sizing guidelines have been proposed in Section 8.6.

Fully-differential always-on chain

Another conceivable way to improve the AO chain performance is to move to a fully-differential architecture. Concerning the amplifiers, a fully-differential design features 6 dB increase in signal amplitude, cancellation of even harmonics, and the elimination of common-mode signals, thus improving on CMRR performance [78]. However, such designs require common-mode output voltage stabilization, which can be achieved employing a common-mode feedback loop. Current state-of-the-art VAD systems use fully-differential AFEs.

Implementation of the supply and bias network

In this work, an ideal supply voltage was considered for each circuit. The next step in the design of the AO chain is to implement a low-power supply cell outputting 0.6 V and a low-power bias network. If a large noise amplitude is present on the supply voltage, PSRR performance should be assessed.

Adaptive threshold voltage implementation

An adjustable comparison voltage at the positive input terminal of the comparator is required to implement context-awareness to background noise. For instance, this voltage could come from a final state machine (FSM) implemented in the MCU and providing the comparison voltage to the comparator through a digital-to-analog converter (DAC). A theoretical proposal for this FSM is presented in Fig. 9.5. This solution is far from perfect or unique, but it does pave the way for future works. N_B denotes the background noise.

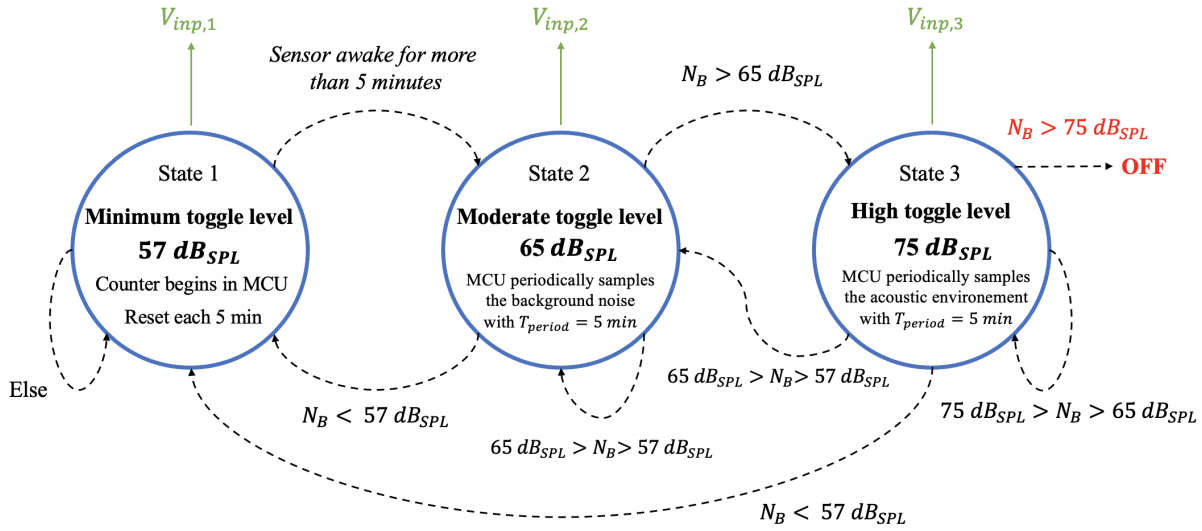


Figure 9.5: A possible implementation for the FSM (in the MCU) providing the comparator with an adjustable comparison voltage. In a given state, the background noise should always be kept under the acoustic toggle level. If the background noise is higher than the maximum acoustic toggle level, the always-on chain should enter OFF mode. As the background noise in forests does not change quickly, a period of 5 minutes seems appropriate.

Additional discussion

This discussion reflects a joint reflection with Thomas Delsart. In his master thesis, he employed a deep learning-based algorithm implemented with a 13 μW CNN network to feature the classification of different sounds in forests. Thomas used a maximum frequency of 8 kHz, twice less than in this work. This frequency is sufficient to classify the sound sources (bird song, poaching activities, gunshots, etc.) with an accuracy of 91.37%. However, the algorithm he implemented does not feature bird species classification. We make the common assumption that a higher frequency than 8 kHz is required to achieve this task. Nevertheless, if future works prove us wrong, this would alleviate some constraints on the AO chain.

One of the main assumptions in this work is that an LP corner for the system above 15 kHz allows the detection of the higher-order harmonics of the sound and would grant a classification between bird species. If it turns out that a maximum frequency of 8 kHz is sufficient for a classification task between bird species, the bandwidth requirements for the AO chain should be lowered to that same value. This would yield a considerable decrease in power consumption, especially for the LNA based on the results of Section 5.7. Nevertheless, another topology than IM OTA should be considered as the IRN value of this topology tends to increase drastically for a decrease in power consumption.

This change in bandwidth constraints would also imply a review of the microphone choice. Therefore, microphones like the VM1010 with a wake-on sound feature or passive microphones could be considered as new potential candidates.

To properly conclude this discussion, a decrease in the bandwidth constraint, combined with design efforts to adapt the sizing of each circuit, could yield a drastic decrease in the total power consumption of the AO chain from 1 μW to couple hundreds of nW. This depends entirely on the ability of a deep learning algorithm to identify the different bird species with a maximum frequency of 8 kHz.

9.5 SWOT analysis

In order to propose a synthetic review of the strengths and weaknesses, opportunities and threats discussed in this work, a SWOT analysis for the AO chain is proposed in Table 9.6.

	Helpful	Harmful
Internal origin	**Strengths** • The proposed topology for the AO chain decreases the power consumption by a factor of 437 with respect to the previous AFE design for the project in acoustic monitoring in forests. • The AO chain aligns with state-of-the-art VAD systems considering the higher target bandwidth. • The architecture of the AO chain exhibits tunability features. Thanks to the optimization Pareto front, a new OTA implementation can easily be selected if GBW product or IRN specifications need to be revised. Moreover, the power consumption of the half-wave rectifier can be decreased if necessary by decreasing the critical bias voltages.	**Weaknesses** • Pseudo-resistor values strongly depend on PVT corners and the hysteresis value of the comparator changes according to statistical variability due to local mismatch. These issues remain to be addressed to ensure the proper working principle for the AO chain. Potential solutions have typically been proposed, respectively trimming for the pseudo-resistance and a new sizing approach for the comparator. • The proposed work is at the simulation stage. Only a tape-out of the proposed circuit can fully validate its working principle.
External origin	**Opportunities** • Given the high bandwidth of the AO chain with respect to VAD systems, the proposed architecture should fit most audio applications requiring a wake-on-sound feature. • There is a high demand for always-listening topologies in the acoustic smart sensors field.	**Threats** • The noise coming from a non-ideal supply voltage could be harmful to the AO chain performance. In addition, PSRR should be evaluated for each circuit in the AO chain. • The robustness of the ICS-40310 to an external environment is not mentioned in its datasheet. A new microphone should eventually be purchased if aging effects occur due to exposure to humidity or harsh weather conditions.

Figure 9.6: SWOT analysis for the always-on chain highlighting the key positive and negative points of this work.

Chapter 10

Conclusion

The extensive deployment of IoT sensor nodes raises serious environmental issues. The employed materials for their designs are rare, difficult to harvest and the replacement of each sensor leads to harmful e-waste for the environment. In the context of acoustic monitoring in forests, we are attempting to develop a non-invasive automated sensor with a long lifespan. Such a sensor requires listening to the surrounding acoustic environment continuously to prevent missing any relevant sound. The main purpose of this thesis was to design an ultra-low-power always-on chain enabling the second stage of the sensing system if the sound level, thus the electrical signal energy, exceeds a particular threshold.

This work began by conducting a thorough search in VAD systems state-of-the-art papers as this field necessitates always-listening topologies. It provided a relevant framework for the TLD architecture of the AO chain. Nevertheless, VAD systems aim at a bandwidth of 5 kHz, which is not appropriate for this application. Indeed, a study of the acoustic environment in forests pointed out the need for higher bandwidth than 15 kHz with a minimum acoustic level of detection at 40 dB_{SPL}. Therefore, the MEMS microphone ICS-40310 from InvenSense was identified as the best-suited microphone for this application.

Afterward, a topology for the LNA was investigated. From the microphone specifications, IRN and bandwidth requirements for the LNA have been identified. The $40\,dB_{SPL}$ acoustic minimum level of detection translates to a 28.25 μV_{rms} IRN value while the bandwidth requirement typically indicates $f_{HP,LNA} < 90\,Hz$ and $f_{HP,LNA} > 16\,kHz$. Appropriate gain and power consumption requirements for this circuit have been set based on a search in state-of-the-art papers. An improved Miller OTA was chosen to meet these requirements. The design of the IM OTA has been realized with an efficient design process relying first on the g_m/I_D sizing methodology and second a two-step optimization employing a genetic algorithm. This allowed satisfying the IRN, bandwidth and power requirements for the LNA. A high feedback resistance value was expected to achieve the HP corner of the LNA and complete its design. However, very high resistance values cannot be achieved with polysilicon resistors as these suffer from poor density. A voltage swing robust pseudo-resistor topology was selected to cope with this issue and implement the resistive feedback. The equivalent resistance of the chosen topology exhibits an improved resilience against voltage swing variation by one order of magnitude (RMSE) in comparison with conventional back-to-back configurations.

Nevertheless, it shows severe resistance variation with statistical variability simulations and PVT corners. Thus, a digital trimming solution has been introduced as a potential candidate to cope with this issue but has not been validated in this work. The total power consumption for the LNA is 530 nW.

Following the LNA, this work studied a half-wave rectifier implemented with the sequence of a transconductance amplifier, current-mode rectifier and transimpedance amplifier. This topology helped to cope with the shortcomings of the precision rectifier at low supply voltage limited by the diode dead-zone. The rectifier exhibits 6 dB gain and a 420 nW power consumption. A saturation phenomenon occurs when the rectifier input voltage is large, but this does not raise particular issues for the operation of the always-on chain. A passive low-pass filter extracts the average value of the rectified signal to avoid power consumption overhead.

To close the design process of the AO chain, this work designed an hysteresis comparator taking a decision based on the low-pass filter capacitor voltage. As it interfaces the second stage of the sensing system, hysteresis allows outputting a constant signal (bit) despite the ripple on the low-pass filter capacitor voltage. The power consumption is 66 nW for the final sizing of the comparator. Unfortunately, the hysteresis for this sizing presents a standard deviation of 1.2 mV (30% of the 4 mV expected value) when running statistical variability simulations. A drop in hysteresis could be damageable for the output bit stability as the amplitude of the ripples could exceed the hysteresis value.

Finally, the working principle of the always-on chain for a worst-case sound amplitude scenario was assessed by a transient noise analysis. It showed that the architecture toggles for a 57 dB_{SPL} sound amplitude, corresponding to a bird singing 15 away from the microphone when the background noise is quiet. The total power consumption of the AO chain is 1.02 μW, representing an improvement of factor 437 with respect to the previous AFE proposed in the project on acoustic monitoring in forests. As a result, the always-on chain aligns with state-of-the-art VAD systems, considering the higher bandwidth in this work.

Appendix A

Detailed mathematical developments

A.1 Improved Miller OTA - Transfer function

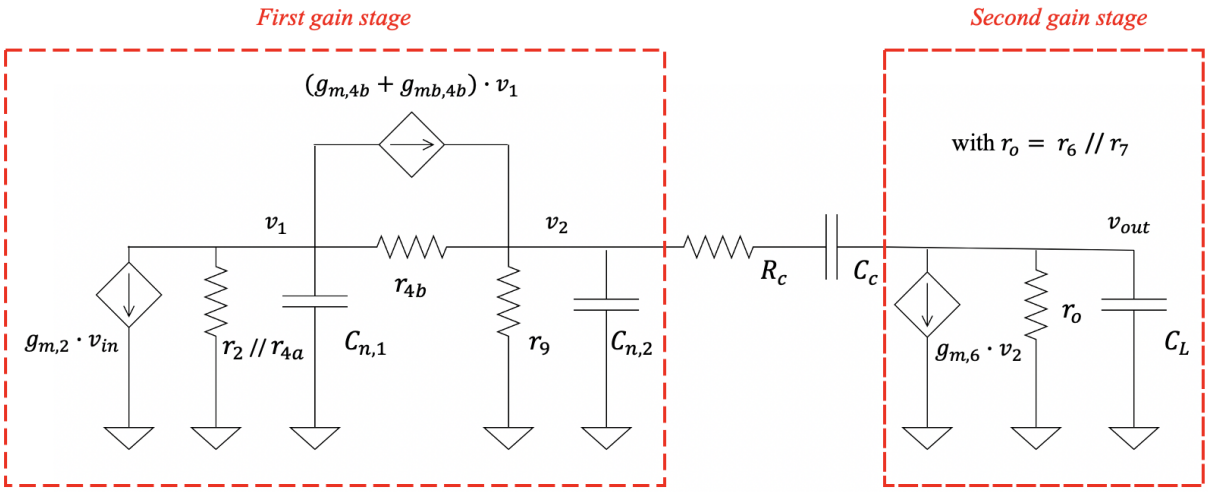


Figure A.1: AC small-signal model of the OTA

Considering Fig. A.1, we have

$$\begin{cases} g_1 = g_{d,2} + g_{d,4a} + g_{C_{n,1}} \\ g_2 = g_{d,9} + g_{C_{n,2}} \\ g_L = g_{d,6} + g_{d,7} + g_{C_L} \\ g_4 = g_{m,4b} + g_{mb,4b} \\ g_c = \frac{1}{Z_c} \end{cases} \tag{A.1}$$

From Kirchhoff current law (KCL), we can write the following system

$$\begin{cases} -g_{m,1} \cdot v_{in} = g_1 \cdot v_1 + g_4 \cdot v_1 + g_{d,4b} \cdot (v_1 - v_2) \\ g_{d,4b} \cdot (v_1 - v_2) + g_4 \cdot v_1 = g_2 \cdot v_2 + g_c \cdot (v_2 - v_{out}) \\ g_c \cdot (v_2 - v_{out}) = g_{m,6} \cdot v_2 + g_L \cdot v_{out} \end{cases} \tag{A.2}$$

The last equation is rewritten as

$$v_2 = \frac{v_{out} \cdot (g_L + g_c)}{(g_c - g_{m,6})} \ . \tag{A.3}$$

In order to write v_1 as a function of v_{out}, we substitute Eq. A.3 in Eq. A.2, yielding

$$\begin{aligned} (g_{d,4b} + g_4) \cdot v_1 &= (g_2 + g_c + g_{d,4b}) \cdot v_2 - g_c \cdot v_{out} \\ &= (g_2 + g_c + g_{d,4b}) \cdot \left[\frac{(g_L + g_c)}{(g_c - g_{m,6})} - g_c \right] \cdot v_{out} \ . \end{aligned} \tag{A.4}$$

The expression for v_1 is found as

$$v_1 = \frac{(g_2 + g_c + g_{d,4b})}{(g_{d,4b} + g_4)} \cdot \left[\frac{(g_L + g_c)}{(g_c - g_{m,6})} - g_c \right] \cdot v_{out} \tag{A.5}$$

Using the first equation of system A.2 and by substituting v_1 and v_2 we obtain

$$\begin{aligned} -g_{m,1} \cdot v_{in} &= (g_1 + g_4 + g_{d,4b}) \cdot v_1 + g_{d,4b} \cdot v_2 \\ \frac{-g_{m,1} \cdot v_{in}}{v_{out}} &= (g_1 + g_4 + g_{d,4b}) \cdot \frac{(g_2 + g_c + g_{d,4b})}{(g_{d,4b} + g_4)} \cdot \left[\frac{(g_L + g_c)}{(g_c - g_{m,6})} - g_c \right] + g_{d,4b} \cdot \frac{(g_L + g_c)}{(g_c - g_{m,6})} \ . \end{aligned} \tag{A.6}$$

By rearranging the transfer function for the OTA is obtained as

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m,1} \cdot (g_{d,4b} + g_4)}{\left[(g_2 + g_c + g_{d,4b}) \cdot (g_1 + g_4 + g_{d,4b}) - g_{d,4b} \cdot (g_{d,4b} + g_4) \right] \frac{(g_L + g_c)}{(g_c - g_{m,6})} - g_c \cdot (g_1 + g_4 g_{d,4b})} \ . \tag{A.7}$$

A.2 Composite transistor - Mathematical development

Using Eq. 2.1 it is possible to isolate the gate-to-source voltage according to

$$V_{GS} = nU_T \cdot \log \frac{I_D}{I_S \cdot \left(\frac{W}{L}\right) \cdot \left(1 - e^{\frac{-V_{DS}}{U_T}}\right)} + V_{th} \ , \tag{A.8}$$

where log stands for the natural logarithm. From the schematic presented in Fig. 5.3, Kirchhoff voltage law (KVL) yields

$$V_{DS,a} = V_{GS,a} - V_{GS,b} \tag{A.9}$$

By substituting A.8 into A.9, and assuming identical threshold voltages we write

$$V_{DS,a} = nU_T \cdot \left[\log \left(\frac{I_{D,a}}{I_{S,a} \cdot \left(\frac{W_a}{L_a}\right) \cdot \left(1 - e^{\frac{-V_{DS,a}}{U_T}}\right)} \right) - \log \left(\frac{I_{D,b}}{I_{S,b} \cdot \left(\frac{W_b}{L_b}\right) \cdot \left(1 - e^{\frac{-V_{DS,b}}{U_T}}\right)} \right) \right] . \tag{A.10}$$

According to the property of the logarithm we can rewrite the previous equation in the following form

$$V_{DS,a} = nU_T \cdot \log \left[\frac{I_{D,a}}{I_{D,b}} \cdot \frac{\frac{W_b}{L_b}}{\frac{W_a}{L_a}} \cdot \frac{I_{S,a}}{I_{S,b}} \cdot \frac{\left(1 - e^{\frac{-V_{DS,b}}{U_T}}\right)}{\left(1 - e^{\frac{-V_{DS,a}}{U_T}}\right)} \right] . \tag{A.11}$$

By assuming identical characteristic currents and neglecting the gate current (implying $I_{D,a} = I_{D,b}$), we further simplify the equation as

$$V_{DS,a} = nU_T \cdot \log \left[\frac{\frac{W_b}{L_b}}{\frac{W_a}{L_a}} \cdot \frac{\left(1 - e^{\frac{-V_{DS,b}}{U_T}}\right)}{\left(1 - e^{\frac{-V_{DS,a}}{U_T}}\right)} \right] . \tag{A.12}$$

Assuming that both transistors are saturated, Eq. A.12 finally simplifies as

$$V_{DS,a} \approx nU_T \cdot \log \left(\frac{W_b/L_b}{W_a/L_a} \right) . \tag{A.13}$$

Appendix B

Preselection and fine-tuning - Sizings

Table B.1 provides the sizing of an OTA from the Pareto front of the preselection step. This sizing has been chosen for the sake of comparison as it features approximately the same power consumption as the g_m/I_D sizing methodology. Table B.2 presents the sizing of the fully-optimized OTA after the fine-tuning step.

Stage	**Transistor**	**Aspect ratio** ($\mu m/\mu m$)
Bias stage	$M_{P,5}$	11.5/1.1
First stage	$M_{1,2}$	39.5/1.1
	$M_{3a,4a}$	9.5/1.1
	$M_{3b,4b}$	49/1.1
	$M_{8,9}$	5.75/1.1
Second stage	M_6	37.5/1.1
	M_7	57.5/1.1

Table B.1: Transistors sizes - Preselection - $C_c = 300\,fF$, $R_c = 59.5\,k\Omega$ and $I_{ref} = 120\,nA$

Stage	**Transistor**	**Aspect ratio** ($\mu m/\mu m$)
Bias stage	$M_{P,5}$	30/1
First stage	$M_{1,2}$	50/1.8
	$M_{3a,4a}$	7.5/2.4
	$M_{3b,4b}$	40/1
	$M_{8,9}$	15/3.1
Second stage	M_6	35/1
	M_7	150/1

Table B.2: Transistors sizes - Fine-tuning - $C_c = 400\,fF$, $R_c = 58\,k\Omega$ and $I_{ref} = 118\,nA$

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